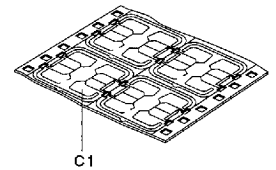
SIEMENS

Intelligent 416-Bit EEPROM with Internal PIN Check

SLE 4404

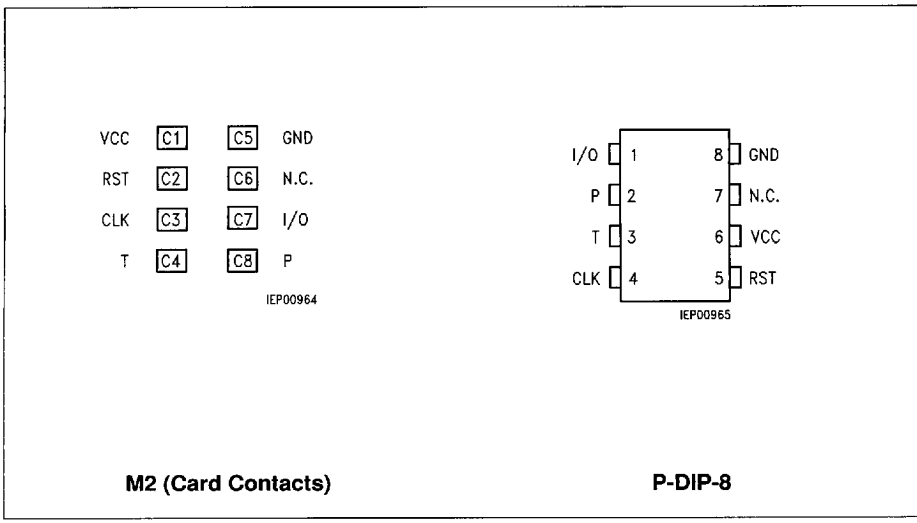
Features

- 416 x 1 bit organization
- 208-bit user memory which can be configured as ROM, PROM, read-protected PROM and read-protected ROM
- User memory protected by means of a changeable user code with non-volatile error counter (blocking state after four incorrect inputs)
- User memory reloadable and configuration changeable up to 64 times, protected by unchangeable memory code with non-volatile counter
- 7 additional memory areas with special characteristics (e.g. RAM, ROM, code data memory, counter register for security purposes)
- Minimum of 10^4 write/erase cycles
- Data retention for a minimum of 10 years
- PIN security logic and other special security features
- Contact configuration and serial interface in accordance with ISO standard 7816-3 (synchronous transmission)



M2

Type	Ordering Code	Package
SLE 4404 M2	on request	Wire-Bonded Module M2
SLE 4404 C	on request	Chip



M2 (Card Contacts) **P-DIP-8**

Pin Configuration (top view)

Pin Definitions and Functions

Pin	Card Contact	Symbol	Function
1	C7	I/O	Bi-directional data line (open drain)
2	C8	P	Control input (data change)
3	C4	T	Test input, has no effect when fused for security, not to be connected
4	C3	CLK	Clock input
5	C2	RST	Control input (reset)
6	C1	V_{CC}	Supply voltage
7	C6	N.C.	Not connected
8	C5	GND	Ground

The SLE 4404 comes out as M2 module (wire-bonded module) for embedding into plastic cards and as die for customer packaging. It is also available in a P-DIP-8 (plastic dual in-line) package for evaluation purposes.

General Description

The chip contains an EEPROM and security logic. The memory area consists of a 416 memory-cell matrix organized in 16-bit rows. Memory organization and security logic are parts of a new concept of chip card ICs which provides a high degree of security against misuse.
The security concept is based on a subdivision of the memory into different functional sections. After blowing a fusible link, the memory and security logic are irreversibly initialized. A 16-bit manufacturing code is entered by the chip supplier and cannot be altered.
The SLE 4404 is ideally suited for security applications, such as personal or transferable cards

- in all counting and calculating systems,
- in all credit and debit systems,
- as electronic key.

Functional Characteristics

The SLE 4404 represents a new kind of chip card concept with "intelligent" memory that ideally utilizes the advantages of EEPROM technology and its increased performance characteristics.

The 208-bit user memory can be reloaded up to 64 times during the life time of the chip. The user memory can be configured as ROM, PROM or read-protected ROM or PROM.

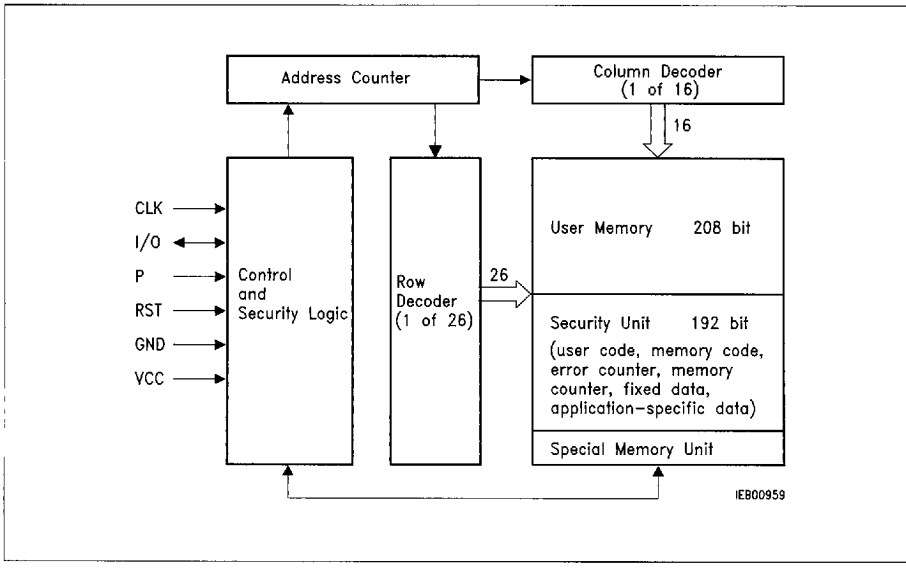


Figure 1
Block Diagram

The security unit includes the following parts with special characteristics:

- User-code for memory access. In a personal card the user may change his PIN himself. In a non-personal card this code is usually a secret one and can only be altered by the system.
- Non-volatile error counter which irreversibly blocks the chip after four successive user code input errors.
- The amount of user memory used is registered in the memory counter with a register capacity of 13 520 bit.
- Reloading of the user memory must be authorized by entering the user code and a 32-bit memory code.
- 16-bit ROM section (fixed data) for the manufacturing code (application, production lot)
- 48-bit ROM section for application-specific data.

The 16-bit scratch pad memory may be used as a note pad or currency exchange list and conveys greater application flexibility to the chip.

Table 1 - Device Operations

Code				Event dependent on the selected address	Conditions
CLK	I/O	P	RST		
x	x	x	1	Reset, address counter = 0	-
1	x	0	0	Increment address	-
0	x	0	0	Read fixed data, scratch pad memory, error counter, application-specific data, memory counter	-
0	x	0	0	Read user memory	User code o.k. addit. conditions
1	0	1	0	Write new user code	User code o.k.
1	0	1	0	Write error counter, memory counter	-
1	0	1	0	Write scratch pad memory	User code o.k.
1	0	1	0	Write user memory	User code o.k. addit. conditions
1	1	1	0	Erase user code	User code o.k.
1	1	1	0	Erase error counter	User code o.k.
1	1	1	0	Erase scratch pad memory	User code o.k.
				"New user memory"	
1	0	1	0	Write memory counter	User code,
1	1	1	0	Erase without changing the address	memory code o.k.

Address Setting (Figure 2 and Table 1)

The address counter is an upward counter which is incremented by every clock pulse as long as P and RST remain "0". It can be reset by RST = "1". Regarding the ATR procedure in ISO 7816-3 a clock pulse during RST= "1" can be supplied.

Read Operation (Figure 2 and Table 1)

For reading a certain bit, set the address counter to the corresponding address. Data at I/O are valid after the delay time t_{d2} during CLK = "0" until the falling edge of the next clock pulse is reached. For non-readable memory address (user code, memory code, read-protected user memory) I/O is permanently high.

Write Operation (Figure 3 and Table 1)

For writing a bit from "1" to "0", count the address counter up to the corresponding address. After setting P to "1" and I/O to "0" the following clock pulse, which does not increment the address counter, writes the desired bit.

Except for the error counter area, a write operation is only possible after correct input of the user code (see "Data Verification").

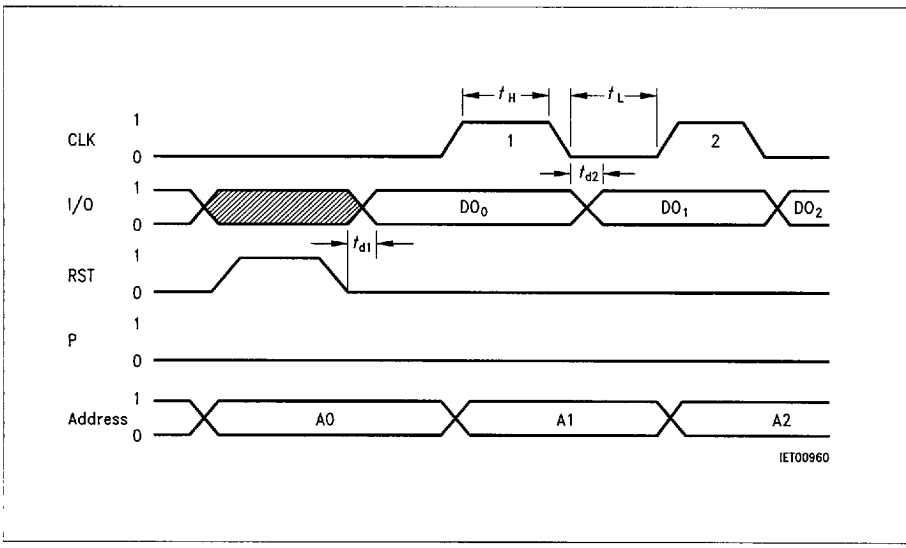


Figure 2
Address Counter Reset and Increment with Reading Data D_N

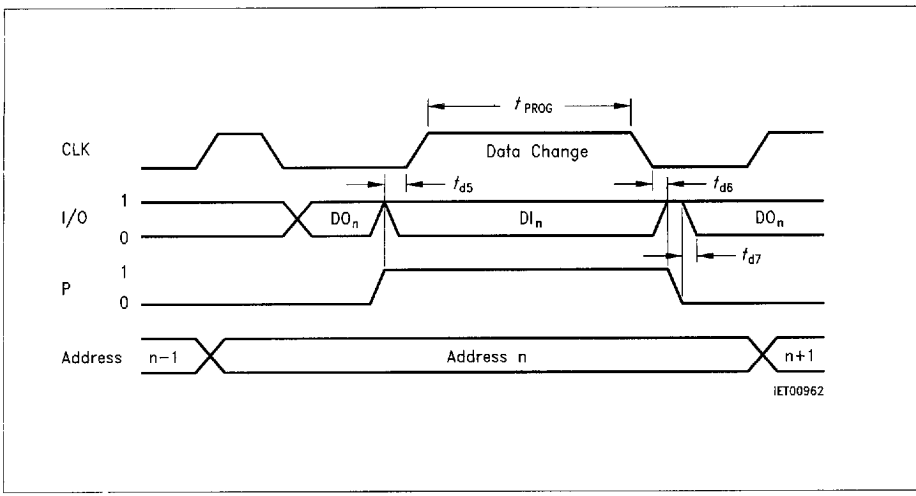


Figure 3
Write / Erase of Data

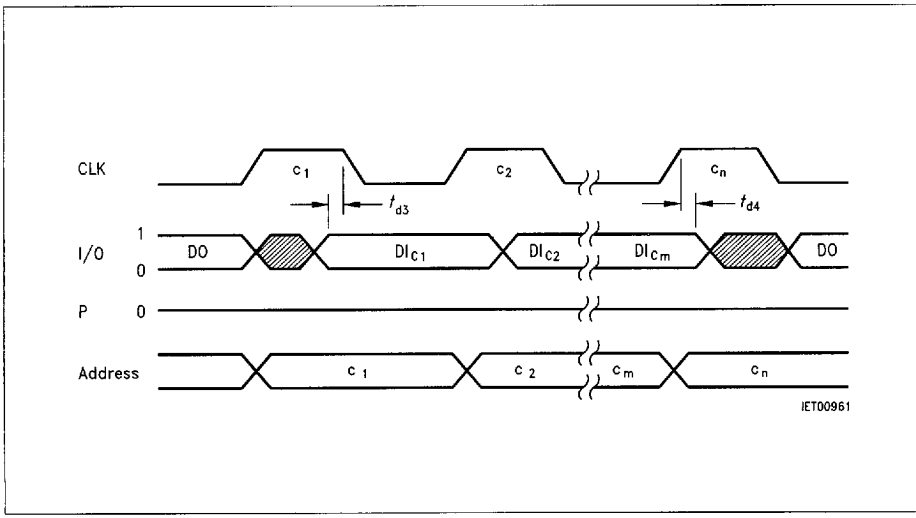


Figure 4
Counting up of Address Counter and Data Comparison with Input DI in Address Range C_1 to C_m

Erase Operation (Figure 3 and Table 1)

The erase procedure only affects the error counter with its additional 12-bit EEPROM area, the scratch pad memory and the user memory. Each area is immediately erased by one command. On principle, any erasure demands a preceding successful input of the user code. For reloading the user memory, correct input of the memory code is additionally necessary (see "Data Verification").

Regarding the first two areas, erasure is carried out by addressing any bit of an area. It is followed by the same procedure as in the write operation but with the difference that I/O = "1". Any reloading of the user memory is recorded in the memory counter. At first therefore any non-written bit of this counter has to be written to "0" immediately followed by an erase operation without incrementing the address.

Data Verification (Figure 4)

With this operation data entered at I/O are compared on-chip with the fixed reference data of the user or memory code corresponding to the selected address.

First the address counter has to be set to the last bit before the code area. At the high phase of the following clock pulses the bits (16 for user code and 32 for memory code) to be compared are entered at I/O and have to be stable during the low phase.

After the presentation of the user code the error counter must be found to have an erased bit which is written to "0". Then the error counter area may be tried to be erased. If the presentation was wrong the erasure is not possible and the attempt is recorded.

The presentation of the memory code is quite similar. This presentation is only possible under the condition of a successful user code presentation. After comparison of the last code bit an erased bit of the memory counter has to be written to " 0". Then an erase operation has to be applied without changing the address. After this procedure the user memory is erased.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Comment
		min.	max.		
Supply voltage	V_{CC}	– 0.3	6	V	-
Input voltage	V_I	– 0.3	6	V	-
Storage temperature	T_{stg}	– 40	125	° C	
Power dissipation	P_{tot}		50	mW	-

Operating Range

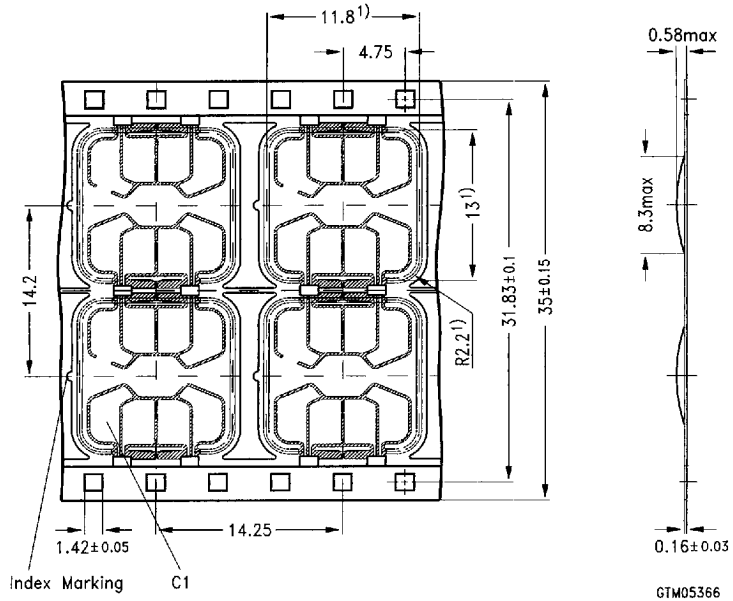
Supply voltage	V_{CC}	4.75	5.25	V	-
Ambient temperature	T_A	–35	80	°C	-

DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply						
Supply voltage	V_{CC}	4.75	5	5.25	V	-
Supply current	I_{CC}		1.8	3	mA	-
Data Input						
H-Input voltage (I/O, CLK, P, RST)	V_H	3.5	-	V_{CC}	V	-
L-Input voltage (I/O, CLK, P, RST)	V_L	0	-	0.8	V	-
H-Input voltage (Testpin C4)	V_H	3	-	V_{CC}	V	-
L-Input voltage (Testpin C4)	V_L	0	-	0.5	V	-
L-Input current (CLK, P) (V_H = 5 V, internal pull-down)	I_{IH}	-	-	100	µA	-
L-Input current (RST) (V_H = 0 V, internal pull-up)	I_{IL}	-	-	100	µA	-
Data Output						
L-Output current (V_H = 0.5 V, open drain)	I_L	-	-	0.5	mA	-
H-Output current (V_H = 5 V, open drain)	I_H	-	-	10	µA	-

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Pulse Duration						
RST	-	10	-	-	µs	-
CLK (count, H-level)	t_H	8	-	-	µs	-
CLK (count, L-level)	t_L	12	-	-	µs	-
CLK (write, H-level)	t_H	5	-	-	ms	-
CLK (erase, H-level)	t_H	5	-	-	ms	-
AC Characteristics						
Delay time (Fig. 2)	t_{d1}, t_{d2}	5	-	-	µs	-
Delay time (Fig. 4)	t_{d3}, t_{d4}	3.5	-	-	µs	-
Delay time (Fig. 3)	t_{d5},t_{d6},t_{d7}	5	-	-	µs	-



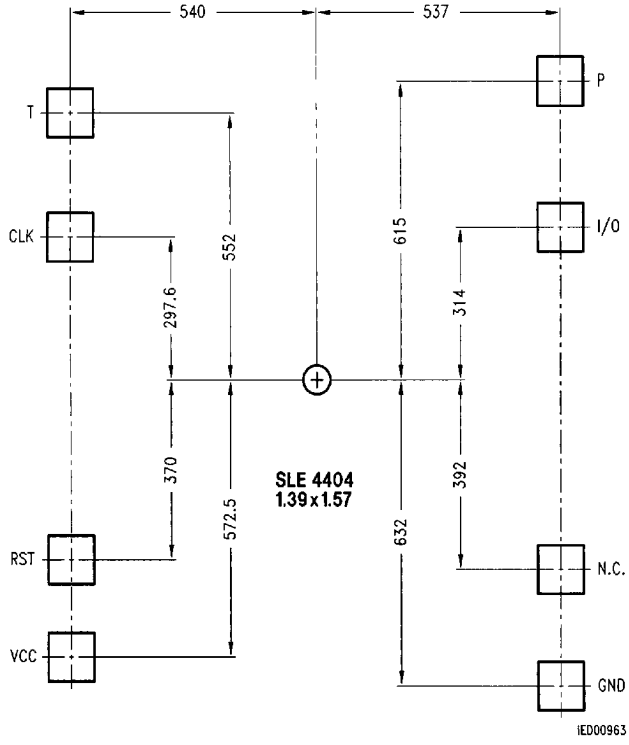
1) Recommended punching contour by customer

Dimensions in mm

Chip and Package Outlines
Wire-Bonded Module M2

Wafer Size:	5"
Stepping Size:	1390 x 1570 µm

Scribe Line:	60 µm
Pad Size:	110 x 110 µm²



Chip Dimensions

B116-H6584
G1-X-7602

8235605 0055657 986