PAGING DECODER IC(POCSAG)

The S-7038AF decoder IC is for use in the CCIR* Radio Paging Code Number 1 (POCSAG** code). It processes internally the POCSAG signals for the Tone-only pager. Furthermore, decoded data is transferred to an external microprocessor, so the S-7038AF can also be used for a Display pager. Eight kinds of call-tone cadences generated for valid calls and messages received let user know which information is received. The S-7038A has a battery saving function that drives the signal receiving circuit intermittently.

* CCIR: International Radio Consultative Committee
** POCSAG: Post Office Code Standardization Advisory Group

■ Features

- Operating voltage : 1.7 to 5.5 V (3.0 V typ.)
- Current consumption : 50 μA max.
- Data rate : 512 or 1200 bps
- User address : 2
- Four cadences per an address receivable
- External elements:
  Crystal oscillators (32 kHz/76 kHz), C_G, R_F
- Direct interface to IDROM (S-2913)
- Three outputs: Tone, LED, vibrator
- CPU direct interface
  CPU controlling output pin and CPU reference clock output pin(32 kHz at 512 bps or 76 kHz at 1200 bps)

■ Functions

- Power-on clearing
- BCH correction up to 2 bits
- Battery saving
- Battery low alert
- Memory (for Tone-only pager,
  4 channels)
- Expansion

■ Mask Options

Table 1

Item	Standard	Option
Corrected BCH errors	Random errors of up to 2 bits	Successive errors of up to 4 bits
IDROM interface	Direct interface to S-2913	Direct interface to S-2100
Tone frequency	2.7 kHz/3.2 kHz	2 kHz/4 kHz
"H" period of BS2	Goes high for 8 bits, in synchronization with BS1	Goes high 8 bits after BS1, and low in synchronization with BS1

■ Block Diagram

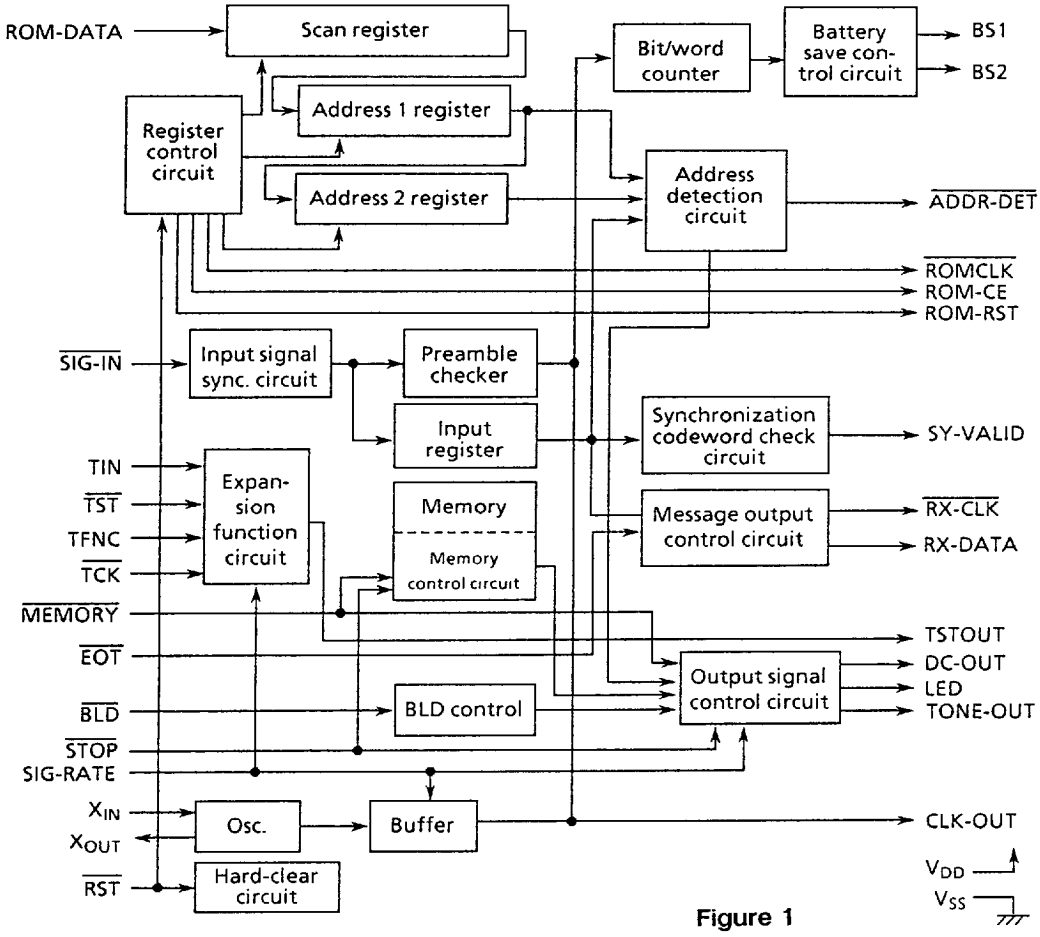
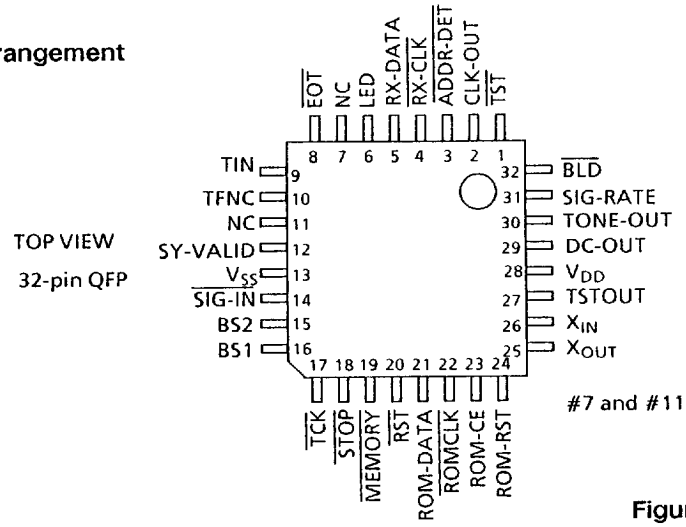


Figure 1

■ Pin Arrangement



#7 and #11 are not connected (NC).

Figure 2

Table 2

Name	I/O	Functions
V_{SS}	—	Negative power supply terminal
V_{DD}	—	Positive power supply terminal
X_{IN}	Input	Crystal connection terminal: 32.768 kHz (512 bps) or 76.8 kHz (1200 bps)
X_{OUT}	Output	Crystal connection terminal: 32.768 kHz (512 bps) or 76.8 kHz (1200 bps)
BS1	Output	Battery save signal, controls RF circuit power turns on
BS2	Output	Battery save signal, determines comparator reference voltage of RF (reception frequency) circuit
$\overline{BLD}$	Input	Battery low detection signal input terminal: Samples the signals from a voltage detector, and battery is regarded as low when low is detected twice successively
$\overline{RST}$	Input	Hardware reset terminal
$\overline{TST}$	Input	Extension mode setting terminal
TIN	Input	Extension data input
TFNC	Input	Extension mode select terminal
$\overline{TCK}$	Input	Extension clock
TSTOUT	Output	Extension mode output terminal
SIG-RATE	Input	Baud rate switchover input terminal Open or high: 512 bps Low: 1200 bps
$\overline{MEMORY}$	Input	Memory mode selection terminal Open or high: Normal mode Low: Memory mode
SY-VALID	Output	Indicates POCSAG signal is receivable
CLK-OUT	Output	System clock output terminal
$\overline{ADDR\text{-}DET}$	Output	Low continues until message output is completed when input signal address matches with that of ID-ROM
$\overline{RX\text{-}CLK}$	Output	RX-DATA (reception message) sample timing clock
RX-DATA	Output	Reception message (sequential output)
$\overline{EOT}$	Input	Completes message reception forcibly when $\overline{EOT}$ goes low
DC-OUT	Output	Vibrator output signal: In memory mode, outputs high when received call is valid
TONE-OUT	Output	Tone output signal : Outputs 2.7 kHz or composite signal of 2.7and 3.2 kHz
$\overline{STOP}$	Input	Turns off tone when $\overline{STOP}$ is low
LED	Output	LED output: 19-kHz pulse signal
$\overline{SIG\text{-}IN}$	Input	Inputs serial data reception signal from RF circuit, in negative logic
ROM-CE	Output	Enables ID-ROM chip
$\overline{ROMCLK}$	Output	ID-ROM synchronous clock
ROM-DATA	Input	ID-ROM data
ROM-RST	Output	ID-ROM reset

■ Dimensions

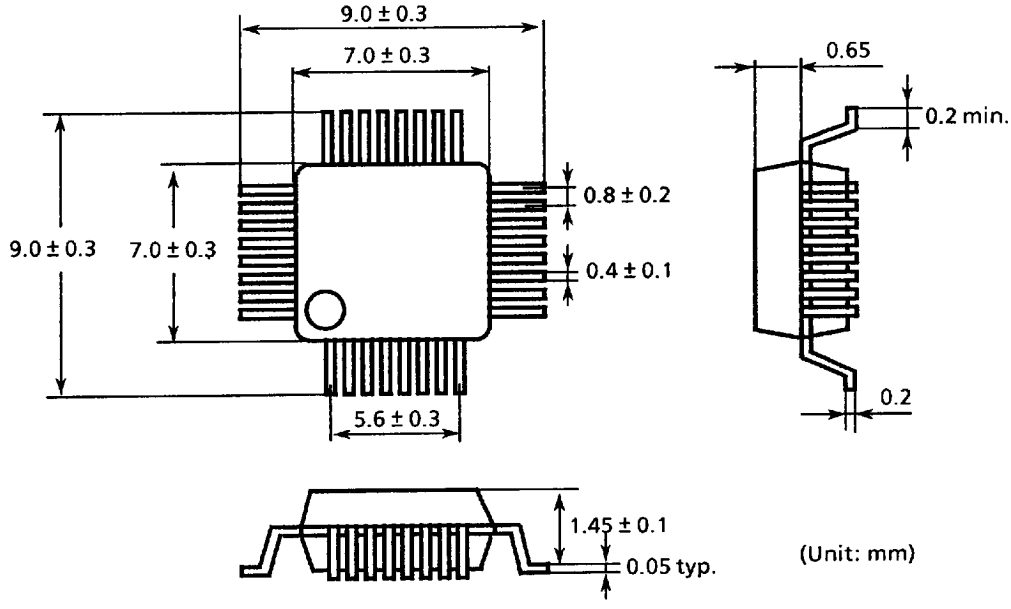


Figure 3

■ Absolute Maximum Ratings

Table 3

Item	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to 7.0	V
Input voltage	V_{IN}	V_{SS}-0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}	V_{SS} to V_{DD}	V
Storage temperature	T_{stg}	-40 to + 125	°C
Operating temperature	T_{opr}	-10 to + 70	°C

■ Electrical Characteristics

Table 4

(Unless otherwise specified: V_{DD} = 3.0 V, V_{SS} = 0 V, Ta = 25°C)

Item	Symbol	Conditions (applicable terminals)		Min	Typ	Max	Unit	Test cir	Note
Operating voltage	V_{DD}	Ta = -10°C to +70°C		1.7	3.0	5.0	V	①	1
		Ta = +10°C to +70°C		1.7	3.0	5.5	V		
Oscillation start up voltage	V_{DOB}	Ta = -10°C to +70°C		2.0	—	5.0	V	①	2
		Ta = +10°C to +70°C		2.0	—	5.5	V		
Standby average current consumption #	I_N	f_0 = 32768 Hz	V_{DD} = 1.7 V	—	8	15	μA	①	3
			V_{DD} = 3.0 V	—	20	30	μA		
		f_0 = 76800 Hz	V_{DD} = 1.7 V	—	15	30	μA		
			V_{DD} = 3.0 V	—	35	50	μA		
TONE-OUT/LED output current	I_{OH1}	V_{DD} = 1.9 V, V_{OH} = 1.6 V		—	—	-500	μA	②	4
	I_{OL1}	V_{DD} = 1.9 V, V_{OL} = 0.3 V		500	—	—	μA		
DC-OUT output current	I_{OH2}	V_{DD} = 1.9 V, V_{OH} = 1.6 V		—	—	-1000	μA	②	4
	I_{OL2}	V_{DD} = 1.9 V, V_{OL} = 0.3 V		1000	—	—	μA		
Output voltage	V_{OH}	I_{OH} = -50 μA, V_{DD} = 3.0 V (*)		2.90	—	—	V	③	—
	V_{OL}	I_{OL} = 50 μA, V_{DD} = 3.0 V (*)		—	—	0.10	V		
Input voltage	V_{IH}	V_{DD} = 1.7 to 5.5 V		0.8 × V_{DD}	—	—	V	④	—
	V_{IL}	V_{DD} = 1.7 to 5.5 V		—	—	0.2 × V_{DD}	V		
Input current	I_{IN}	V_{IN} = V_{DD} or V_{SS}		—	—	±0.1	μA	⑤	—
Pull-up current	I_{R1}	V_{IL} = 0 V (**)		-20	-10	-5	μA	⑥	—
	I_{R2}	V_{IH} = 2.8 V ($\overline{STOP}$, $\overline{MEMORY}$)		-120	-60	-30	μA		
	I_{R3}	V_{IL} = 0 V ($\overline{STOP}$, $\overline{MEMORY}$)		-20	-10	-5	μA		
	I_{R4}	V_{IH} = 2.8 V ($\overline{RST}$)		-120	-60	-30	μA		
	I_{R5}	V_{IL} = 0 V ($\overline{RST}$)		-3.75	-2	-1	μA		
	I_{R6}	V_{IL} = 0 V ($\overline{TST}$, TIN, $\overline{TCK}$)		-200	-100	-50	μA		
$\overline{RST}$ pulse width##	t_{RST1}	At power on, C (external) = 20 pF		10	—	—	μs	—	—
	t_{RST2}	At $\overline{RST}$ input		1	—	—	ms		
$\overline{STOP}$ pulse width	t_{STOP}			10	—	—	ms	—	—
$\overline{MEMORY}$ pulse width	t_{MEM}			10	—	—	ms	—	—
$\overline{EOT}$ pulse width	t_{EOT}			10	—	—	μs	—	—
Frequency IC deviation	△f/△IC			—	—	±50	ppm	—	5
Frequency voltage deviation	△f/△V			—	—	±8	ppm	—	6
Recommended equivalent resistance	CI			—	—	45	kΩ	—	—

* CLK-OUT, $\overline{ADDR\text{-}DET}$, $\overline{RX\text{-}CLK}$, RX-DATA, SY-VALID, BS1, BS2, $\overline{ROMCLK}$, ROM-CE, ROM-RST, TSTOUT

** SIG-RATE, $\overline{BLD}$, TFNC, $\overline{EOT}$

\# Average of values measured at each crystals when Ta = +80°C

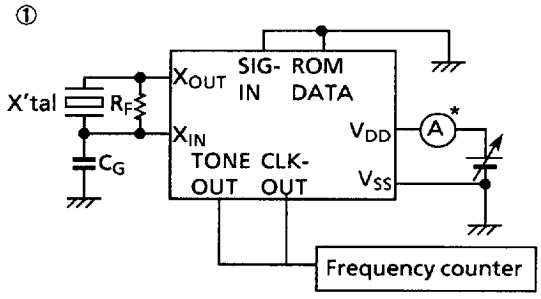
For only $\overline{RST}$ pin, latch-up strength is -90 mA

Notes:

1. Power supply voltage while frequency output from TONE-OUT is stable at $\overline{TCK}$ = low. It is recommended that 0.2 μF or more of capacitor is inserted between V_{SS} and V_{DD}.
2. Voltage value where 32 kHz or 76 kHz is output from CLK-OUT pin within 10 s after oscillation starts.
3. Excluding a pull-up current. Measured under the condition that SIG-IN and ROM-DATA are connected to V_{SS}, other pins are open and the oscillation circuit operates.
4. Suppose that a current flowing into the IC is positive.
5. $$\triangle f/\triangle IC = \frac{f(V_{DD} = 3.0\ V) - f_0}{f_0} \times 10^6\ (ppm)$$ f_0: Average frequency when V_{DD} is 3.0 V
6. $$\triangle f/\triangle V = \frac{f_1(V_{DD} = 3.0\ V) - f_2(V_{DD} = 2.9\ V)}{f_1(V_{DD} = 3.0\ V)} \times 10^6\ (ppm)$$

■ Test Circuits

①

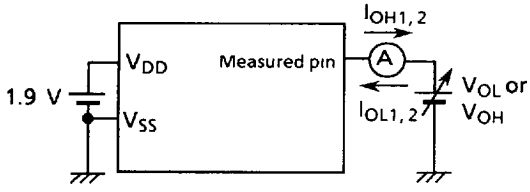


External crystal

Crystal	R_F	C_G
32768 Hz	15 MΩ	12 pF
76800 Hz	15 MΩ	

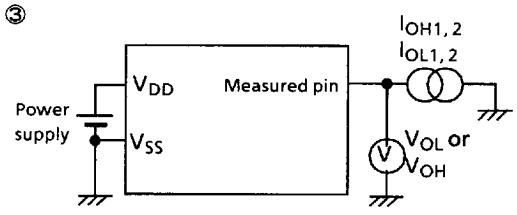
Item	Measuring method
Current consumption	Connect SIGIN and ROM-DATA to V_{SS}, and open other pins. Insert an ammeter at the position of *.
Oscillation strat voltage	Connect the frequency counter to the CLKOUT pin.
Power supply voltage	Connect the frequency counter to the TONEOUT pin.

②



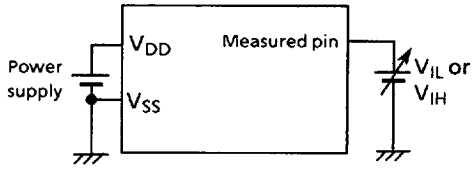
Forcible specification of output pins for the expansion function is used.

③

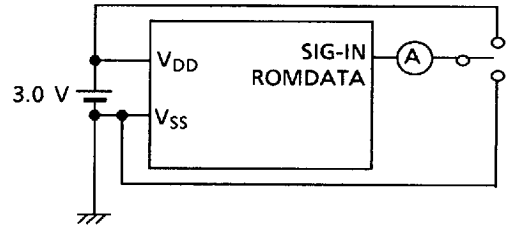


Forcible specification of output pins for the expansion function is used.

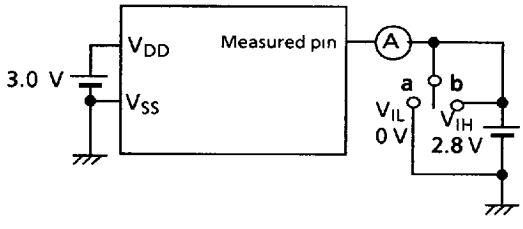
④



⑤



⑥



When I_{R1}, I_{R3}, I_{R5} or I_{R6} is measured: switch **a**
When I_{R2} or I_{R4} is measured: switch **b**

Figure 4

■ Tone-Only Pager and Display Pager

The S-7038AF is used for both the tone-only pager and the display pager, by specifying ID-ROM data. See p5-208 "Application circuit examples" for the circuit design of each pager.

1. Tone-only pager

   This pager informs the user of reception by tone when a received call signal (address data) is valid. And instead of tone, it can also store the valid call information in the memory, (see p5-198 "4. Memory function").

2. Display pager

   A microcomputer and a display unit is added for using as a display pager. The S-7038AF transmits to the CPU only the necessary information, when the received call signal (address data) and the message are valid. The CPU, then, informs the user of pager information by displaying the message, tone, vibration, and light (LED).

   The S-7038AF has two types of user addresses. Each has four kinds of tone cadence. The transmission side determines the tone cadences with a 2-bit tone selection bit.

■ POCSAG Signal Code Format

The POCSAG signal code format of the S-7038AF conforms with CCIR recommendation 584 (see Figure 5).
The transmission unit of a POCSAG signal is called a *block*. This block comprises a preamble and one or more batches following the preamble.

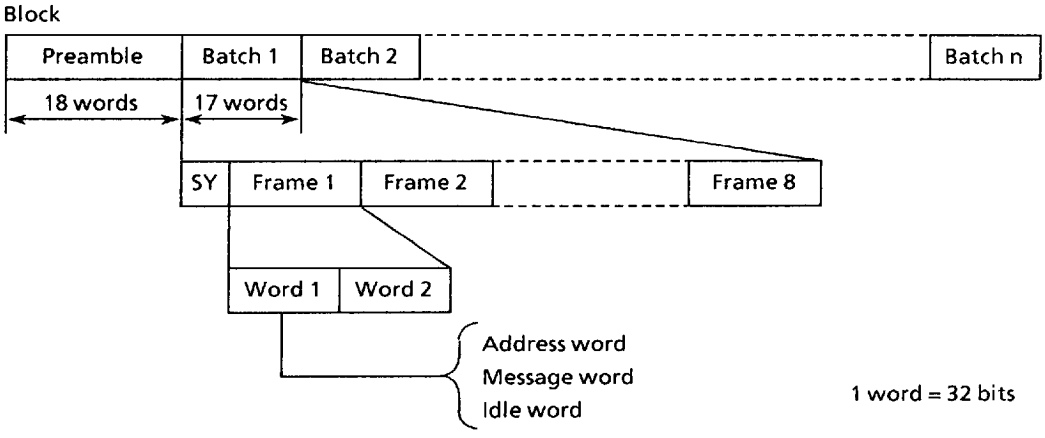


Figure 5 POCSAG code format

1. Preamble
   The preamble at the beginning of a block gives notice of a POCSAG signal sent to the S-7038AF. A preamble consists of at least 576 bits (18 words) alternate signals of 1 and 0. The S-7038AF starts to get the internal circuit and the POCSAG signal synchronized once it receives a preamble.

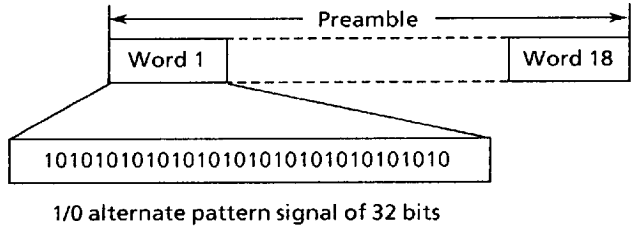


Figure 6 Preamble configuration

2. Batch

The batch contains information on the POCSAG signal, sent following a preamble. Each batch carries a synchronization codeword (SY) and eight frames.

When the S-7038AF recognizes preamble and SY as being those of POCSAG signal, it considers the following signal as a POCSAG frame data and receives it. The S-7038AF identifies the receiving frame set by ID-ROM and receives only the selected frame of one batch and BS1 pin turns high (on) only with a selected frame.

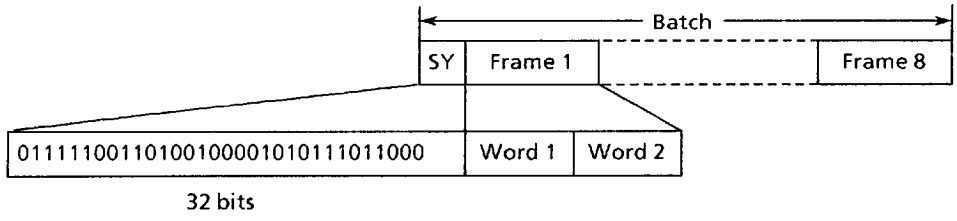


Figure 7 Batch configuration

Synchronization codeword (SY): 32-bit signal shown in Figure 7. When the SY is received after a preamble, it is considered a POCSAG code.

Frame: One frame consists of two words, each of which is 32 bits. There are three types of words: address word, message word and idle word.

3. Kinds of word

There are three types of word information, as shown in Figure 8.

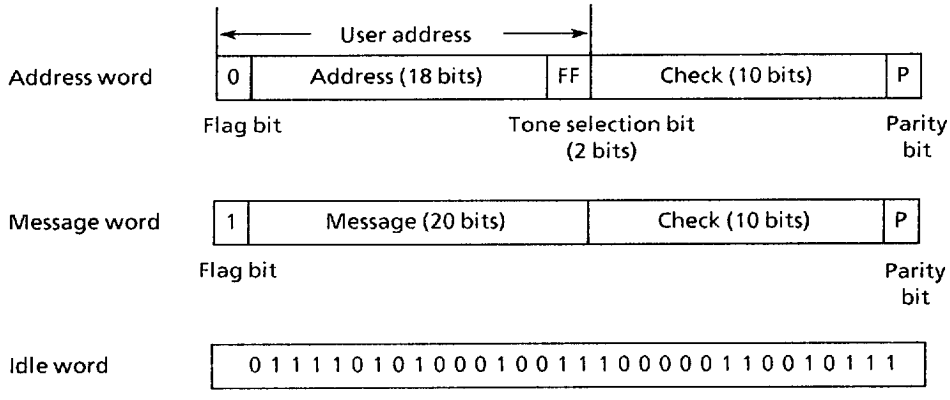


Figure 8 Kinds of words

The address word is sent first, followed by sending the message word to the address (for display pager only). Two or more message words are sent continuously. (Tone-only pagers need no messages; idle words can be used instead.) A flag bit determines whether the word is an address word or a message word. 0 means an address word, and 1 means a message word. The actual information is the address and tone selection bits (FF) in an address word, and the message in a message word.

Address word: This data indicates that the pager is called. An address is always sent with any information. Of the 21 bits in a user address, only 18 bits are used for the actual address. Two tone selection bits select the calling tone (see p5-189 "External output"). Check bits perform BCH checks (see p5-196 "BCH decode function").

Message word: Of the 32 bits in a message word, only 20 bits are used for the actual message. If a message exceeds 16 words, subsequent message words are received in the next frame until an address word is detected (a flag bit becomes 0). Multiple message words can be continuously sent. A synchronization codeword (SY) must be inserted to continue message from frame 8 (last frame of a batch) to the next batch. The S-7038A outputs these message words to the CPU.

Idle word: If a batch does not have any information to send, idle words fill the blank portion of the batch. Idle word cannot be assigned as ID codes.

■ Flow Charts

Figures 9 and 10 show flow charts of POCSAG signal reception. These flow charts indicate the operations from turning on the power to sending output signals, for tone-only pager and for display pager.

1. Tone-only pager

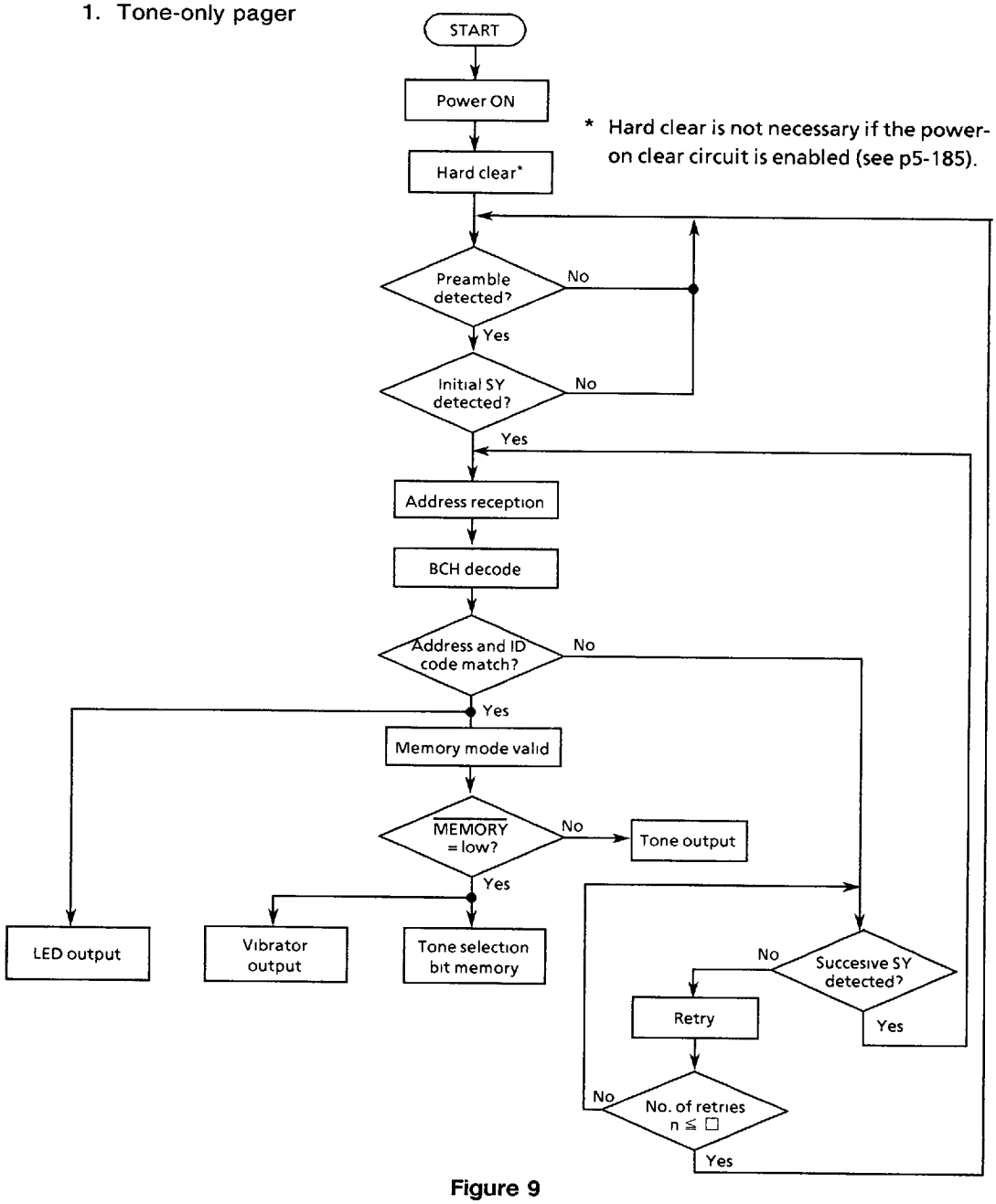


Figure 9

2. Display pager

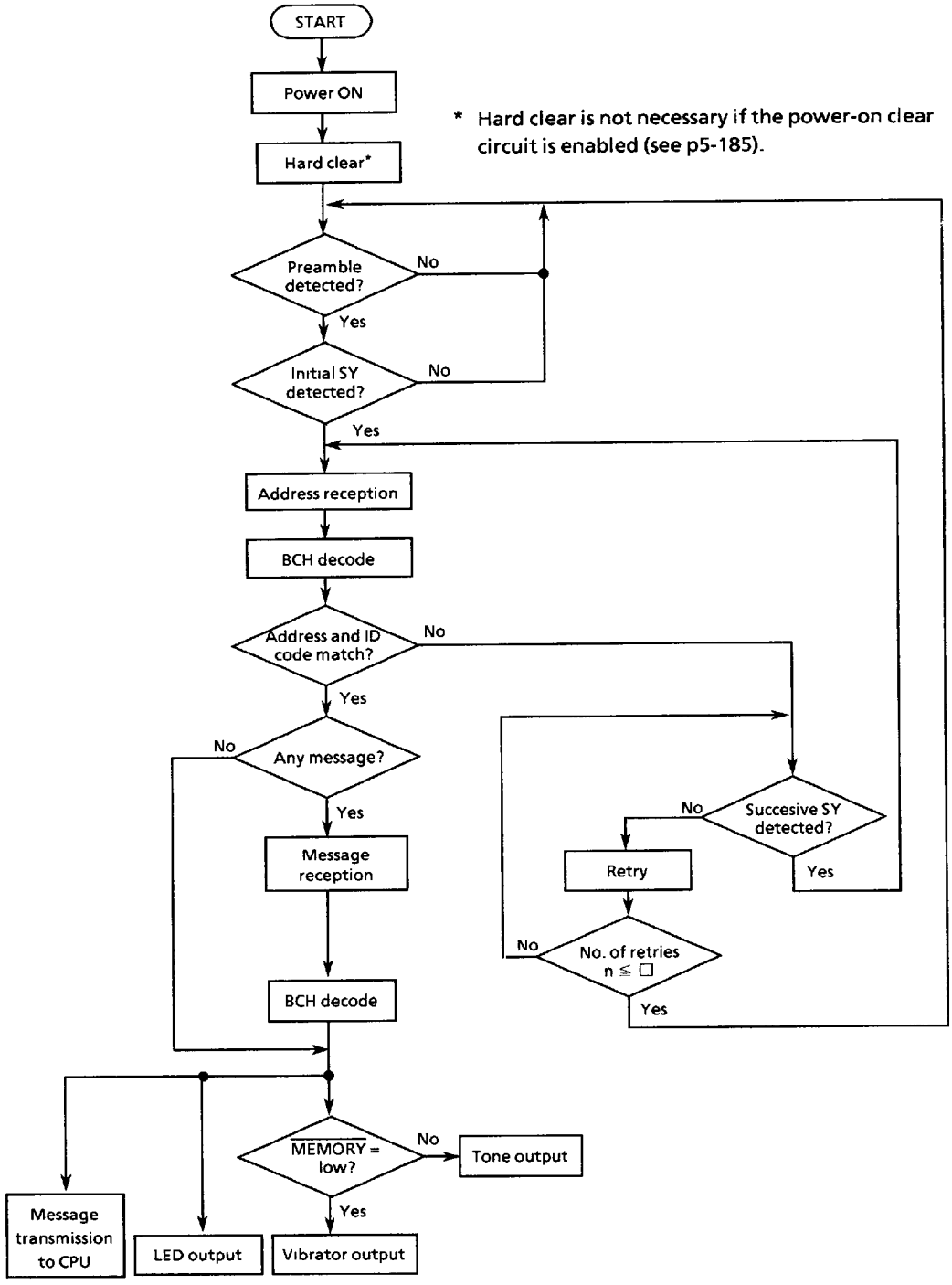


Figure 10

■ Basic Operation

1. Hard clear
   The internal circuit is initialized by setting the $\overline{RST}$ pin to low. The initial tone is output immediately after hard clear (see p5-190 for waveform). POCSAG signal cannot be received during this time. The initial tone automatically stops when the $\overline{STOP}$ pin is set to low or two seconds have passed. After the completion of initial tone, ID-ROM data is fetched in the S-7038AF.
   The internal circuit will function as a power-on clear circuit by connecting 20 pF capacitor between $\overline{RST}$ and V_{SS} pins. That is, the internal circuit is automatically initialized at power on.

2. Detecting preamble
   Preamble detection mode starts when hard clear is completed or when synchronization codeword is not detected even if detection is repeated over number of retries. During this mode, an alternate pattern of 1, 0, 1, 0 of 12 consecutive bits is regarded as a preamble.
   The S-7038AF drives the reception frequency (RF) circuit intermittently to save power consumption. When BS1 pin is high, the radio part is turned on to detect preambles. When the BS1 pin is low, preamble signals are not detected. Once a preamble is detected, the BS1 pin is set to high until a SY is detected. Figure 11 shows the timing of BS1 pin and preambles.

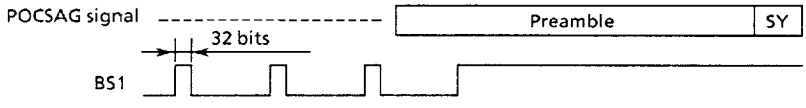


Figure 11 Timing of BS1 pin and preambles

Simultaneous detection mode of preamble and SY

In this mode, either a preamble or a synchronization codeword (SY) is detected simultaneously to receive POCSAG signals (see p5-203). This mode becomes valid when the PR bit of the ID-ROM is set to high. SY can be detected, even if no preamble is detected.

In this mode, S-7038AF detects SY according to the following procedures :

1. First, S-7038AF searches for preamble code within a time duration which has 32 bits-width time period, and cycle time of the time duration is 576 bits width period.
2. If preamble codes of 12 bits are not detected in the time duration, S-7038AF searches for BCH code word whenever input signals are sampled within a extended time duration which has 96 bits-width time period.
3. If S-7038AF finds BCH code word without error correction in the extended time duration, S-7038AF searches for SY continuously.

* In this mode, receiving period is longer than "Only preamble detection" mode (see p5-203 Table 8).
  So, power consumption increases more than the "Only preamble detection" mode. But the S-7038AF using this mode is synchronized with POCSAG signal in one batch time duration from unsynchrorous condition.

3. Detecting synchronization codeword (SY)
After detecting a preamble, the S-7038AF enters SY detection mode. The SY, first after preamble detection, is the initial SY. New SYs, sent after a batch is received, are called succesive SY.

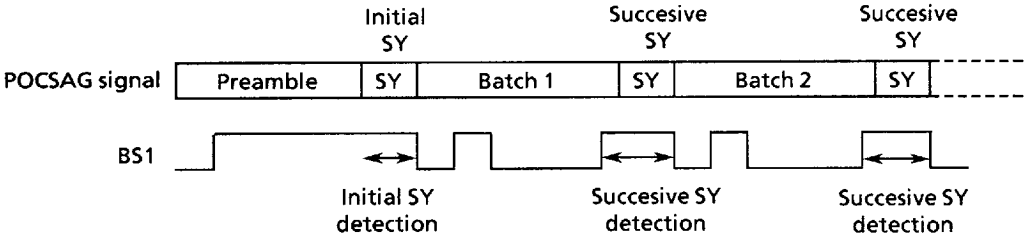


Figure 12 Initial SY and succesive SY

3.1 Initial SY detection mode
The operation which detects the initial SY following a preamble is called the initial SY detection mode. The S-7038AF compares the sent data with the SY data set in the S-7038AF (see Figure 7). After receiving one bit of data, the S-7038AF compares the 32-bit data, including that bit and those before it, with the SY. If 30 or more bits match, the SY is considered to be detected. Even if radio wave are affected by noise, SY is detected as long as there are no more than two faulty bits.

If SY is not detected after comparing 32 words (about 1K bits) in initial SY detection mode, the S-7038AF returns to preamble detection mode.

3.2 Succesive SY detection mode
After initial SY is detected, SY is sent for each batch. After receiving 8-frame (16-word) data, the S-7038AF enters automatically succesive SY detection mode. Since the signal is already in synchronization, BS1 goes high and the S-7038AF compares the sent data with the SY data set in the S-7038AF, in synchronization with the timing when 32 bits of succesive SYs are output. In the same way as in initial SY detection mode, SY is detected even when there are up to two bits of unmatching data. If SY is detected, the bit/word counter is reset, followed by processing a batch of data.

If SY is not detected, the S-7038AF retries SY detection for the number of times specified in ID-ROM plus two. If the S-7038AF fails to detect SY during these retires, it returns to preamble detection mode.

Example : When the S-2913 is used for ID-ROM

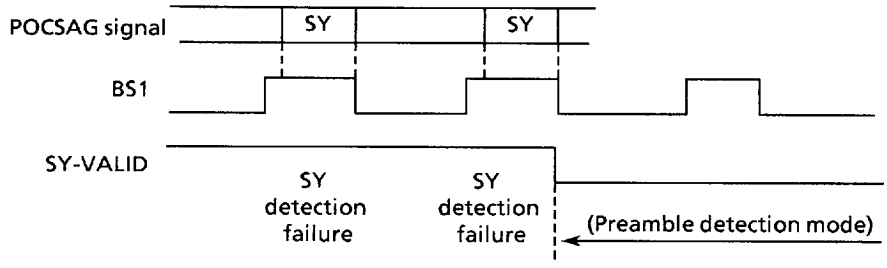
Specifies with bits R3 to R0 (see p5-203 "Interface to ID-ROM" for the bit configuration of ID-ROM).

Table 5 Setup of number of retries

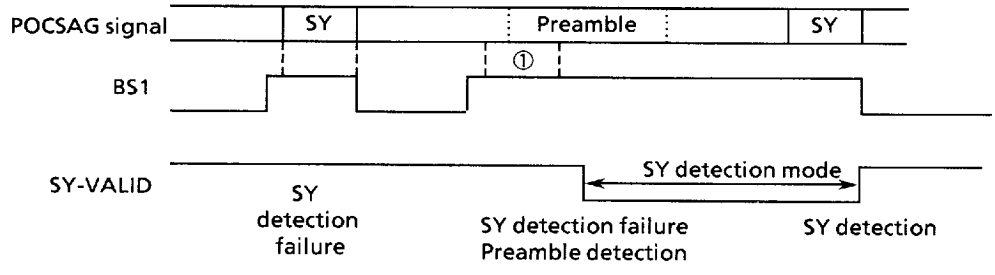
R3	R2	R1	R0	Number of retries
0	0	0	0	2
1	0	0	0	10
1	1	1	1	17

If 12 bits consecutive alternate data such as 1, 0, 1, 0 is detected during the final retry, the S-7038AF regards it as a preamble and enters the initial SY detection mode (see Figure 13).

(1) When the S-7038AF detects no SY and returns to the preamble detection mode



(2) When the S-7038AF detects a preamble in the final retry



① : Period of final retry

Figure 13 Failure to detect succesive SY

4. Detecting address
After detecting SY, the S-7038AF receives eight frames. An address word is placed at the top of a frame. As shown in Figure 14, the last 11 bits of the address word are check bits, and are used for error detection with BCH decode (see p5-196 "BCH decode function"). The S-7038AF compares the non-erroneous address words with the two addresses written in ID-ROM, and receives a message word if they match. Erroneous address words are ignored. If addresses 1 and 2 are received at the same time, address 1 is given priority. Address 2 is regarded as not being received.

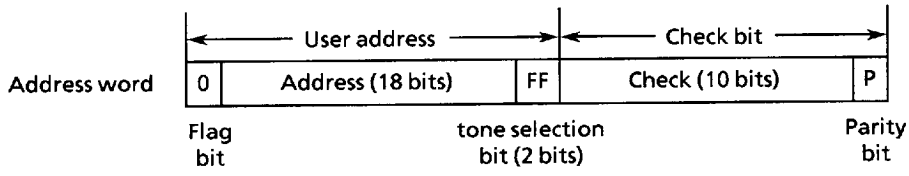


Figure 14 Address word configuration

5. Detecting message (for display pager only)
When an address word is detected, a message word is subsequently received. The S-7038AF sends the message word to CPU, and the message is then sent to the pager display. Message words are continued to detect until an address or idle word is detected.

As shown in Figure 15, the last 11 bits of the message word are also check bits, and are used for error detection with BCH decode (see p5-196 "BCH decode function"). If an error is found, the message word is sent to the CPU with the error information.

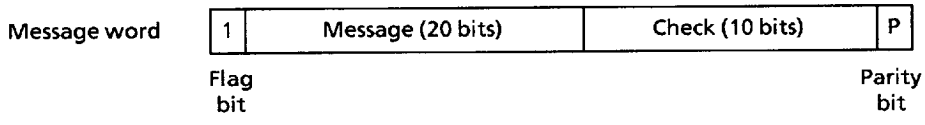


Figure 15 Message word configuration

When the S-7038AF detects SY between message words, the following message is sent to the CPU again after SY is detected. If synchronization is out of step at SY detection, message detection is terminated.

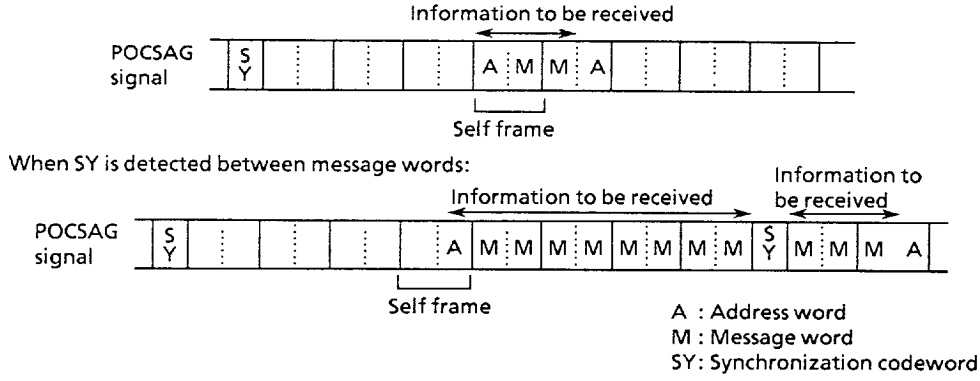


Figure 16 Information to be received

6. External Output

When detecting an address (receiving a call), the S-7038AF sends a message and notifies the operator of the reception by means of tones, lights (LED) and vibration (vibrator). They are output also at power supply voltage drop or initialization. Three pins are provided for external output signals: TONE-OUT, DC-OUT and LED.

6.1 Tone

Tone signals are output from TONE-OUT pin. They are output upon completion of pager initialization, address reception, power supply voltage drop (see p5-195 "Battery low alert function") and memory remain tone (see p5-198 "Memory function").

Upon completion of initialization: A 2.7-kHz single-tone signal is output for two seconds just after hard clear. This is called the initial tone. Setting the $\overline{\text{STOP}}$ pin to low prevents the initial tone sounding.

Upon address reception: When address reception is completed, a tone is output for 20 seconds. The waveform varies with the contents of the tone selection bits. The tone stops by setting $\overline{\text{STOP}}$ pin to low. Four types of tones are specified for an address. A single-tone of 2.7 kHz and a composite tone of 2.7 and 3.2 kHz are available. Use the TM bit of ID-ROM to specify which tone is assigned to which of the two addresses. By setting the TM bit to low, the single tone is assigned to address 1 and the composite tone is assigned to address 2 (see p5-203).
Upon address reception, a quiet sound is emitted for the first two seconds, it then increases in volume.

Upon power supply voltage drop: If $\overline{\text{BLD}}$ pin goes low, due to a power supply voltage drop, two 2.7-kHz single-tones are output every 32 seconds. This is called "BLD tone". This continues until $\overline{\text{STOP}}$ pin is set to low for 5.3 s at 512 bps or 2.3 s at 1200 bps.

Upon memory remain tone : If there is any call information remaining in memory, 125 ms of tone is output twice every 128 batches. A 2.7-kHz tone is heard from the pager.

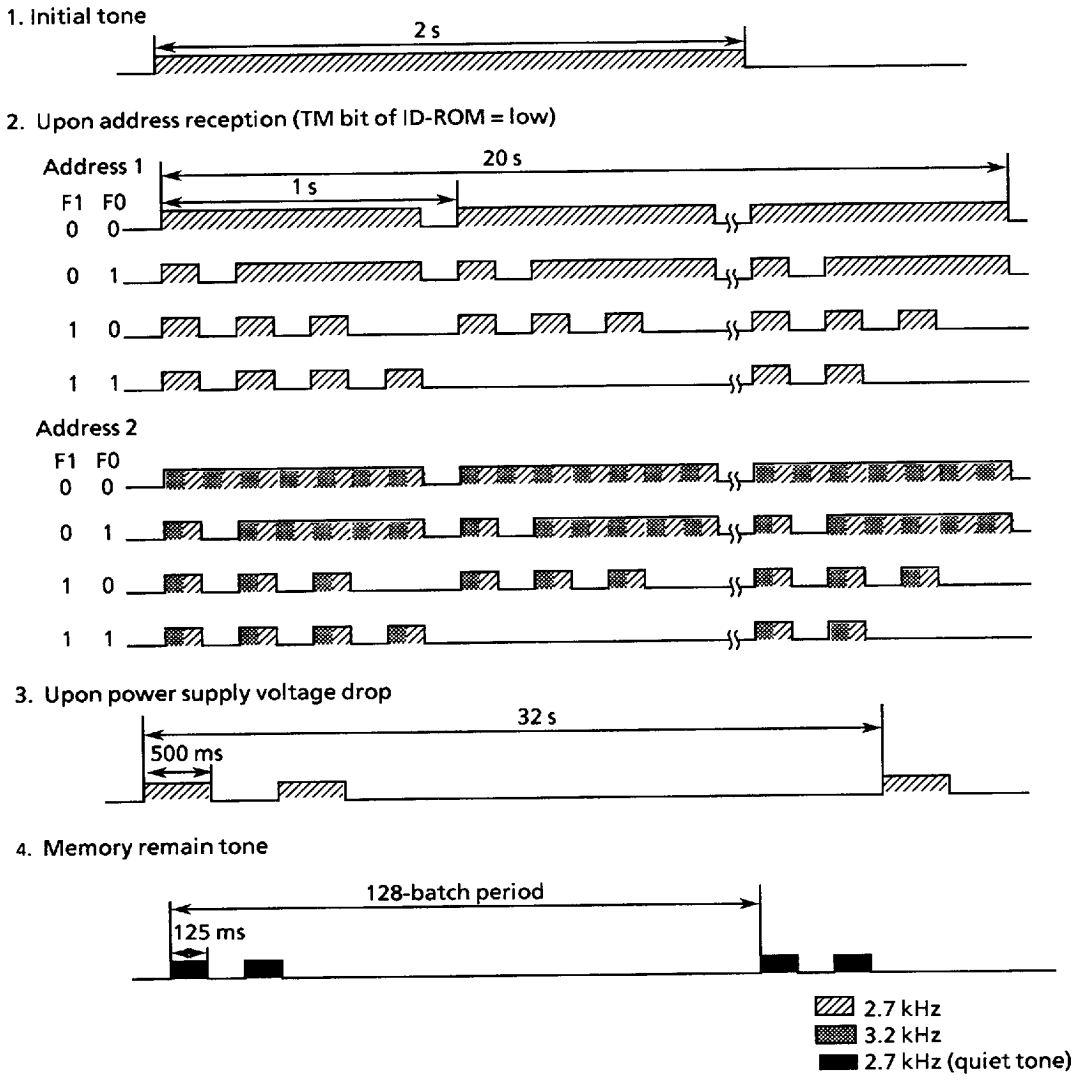


Figure 17 Output waveform of TONE-OUT

6.2 Output for LED

LED drive control signals are output from LED pin. These signals are output upon completion of pager initialization, address reception, power supply voltage drop and memory remain tone. The output waveform is a multiple signals of that of a tone output multiplexed with a 16-kHz (or 19-kHz at 1200 bps) waveform. The output signal of LED pin is output regardless of the input signal of $\overline{\text{MEMORY}}$ pin, and is prevented when $\overline{\text{STOP}}$ pin is set to low.

6.3 Output for vibrator drive control

Vibrator drive control signals are output from DC-OUT pin, upon completion of pager initialization and address reception, only when $\overline{\text{MEMORY}}$ pin is set to low. Vibrator stops to vibrate by setting $\overline{\text{STOP}}$ pin to low.

If OR bit of ID-ROM is set to high, a tone is output upon reception of adress 1 regardless of $\overline{\text{MEMORY}}$ pin (unconditional tone). DC-OUT is not output in this case.

Upon completion of initialization: The vibrator signal is output for 2 s immediately after hard clear.

Upon address reception: The vibrator signal is output, in synchronization with the LED output signal for 20 s.

		Normal mode	Memory mode
Initialization		(A)	(B)
Calling	Address 1 (TM = L, OR = L)	(C)	(E)
	Address 1 (TM = L, OR = H)	(C)	(C)
	Address 1 (TM = H, OR = L)	(D)	(E)
	Address 1 (TM = H, OR = H)	(D)	(D)
	Address 2 ($\overline{\text{TM}}$ = L)	(D)	(E)
	Address 2 (TM = H)	(C)	(E)
Power supply voltage drop		(F)	(G)
Memory remain tone		(H)	—

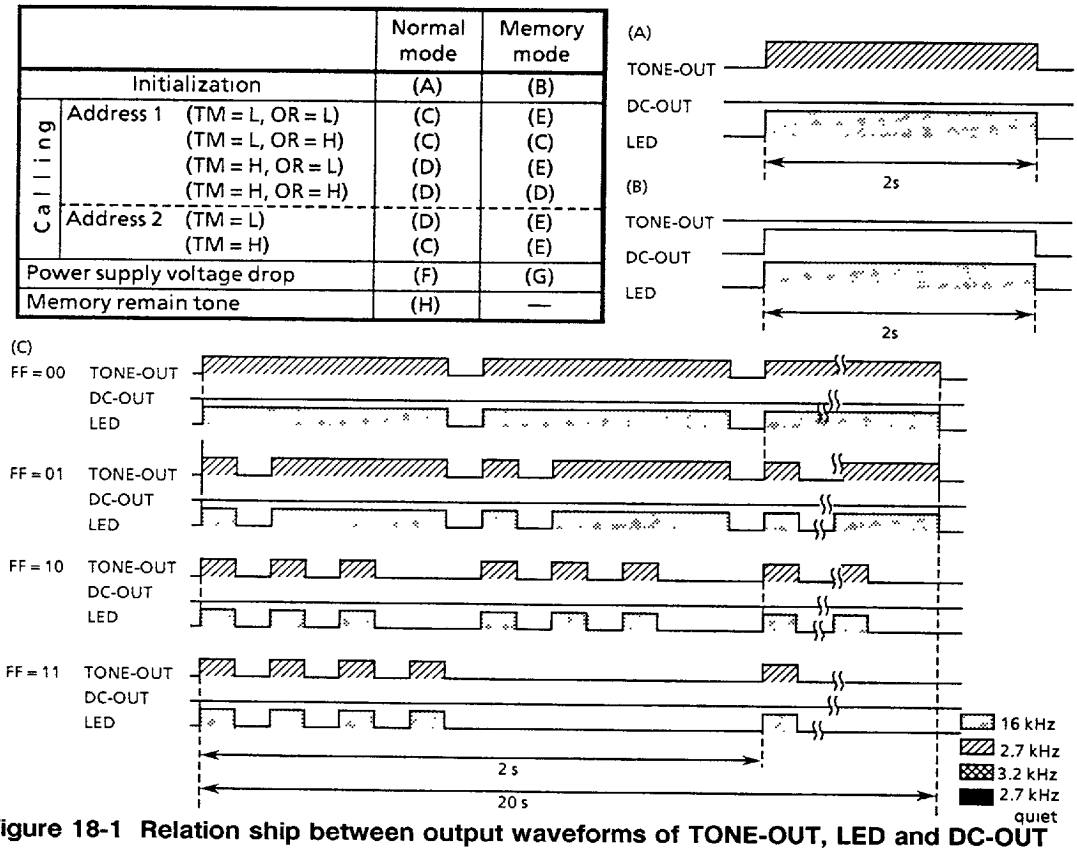


Figure 18-1 Relation ship between output waveforms of TONE-OUT, LED and DC-OUT

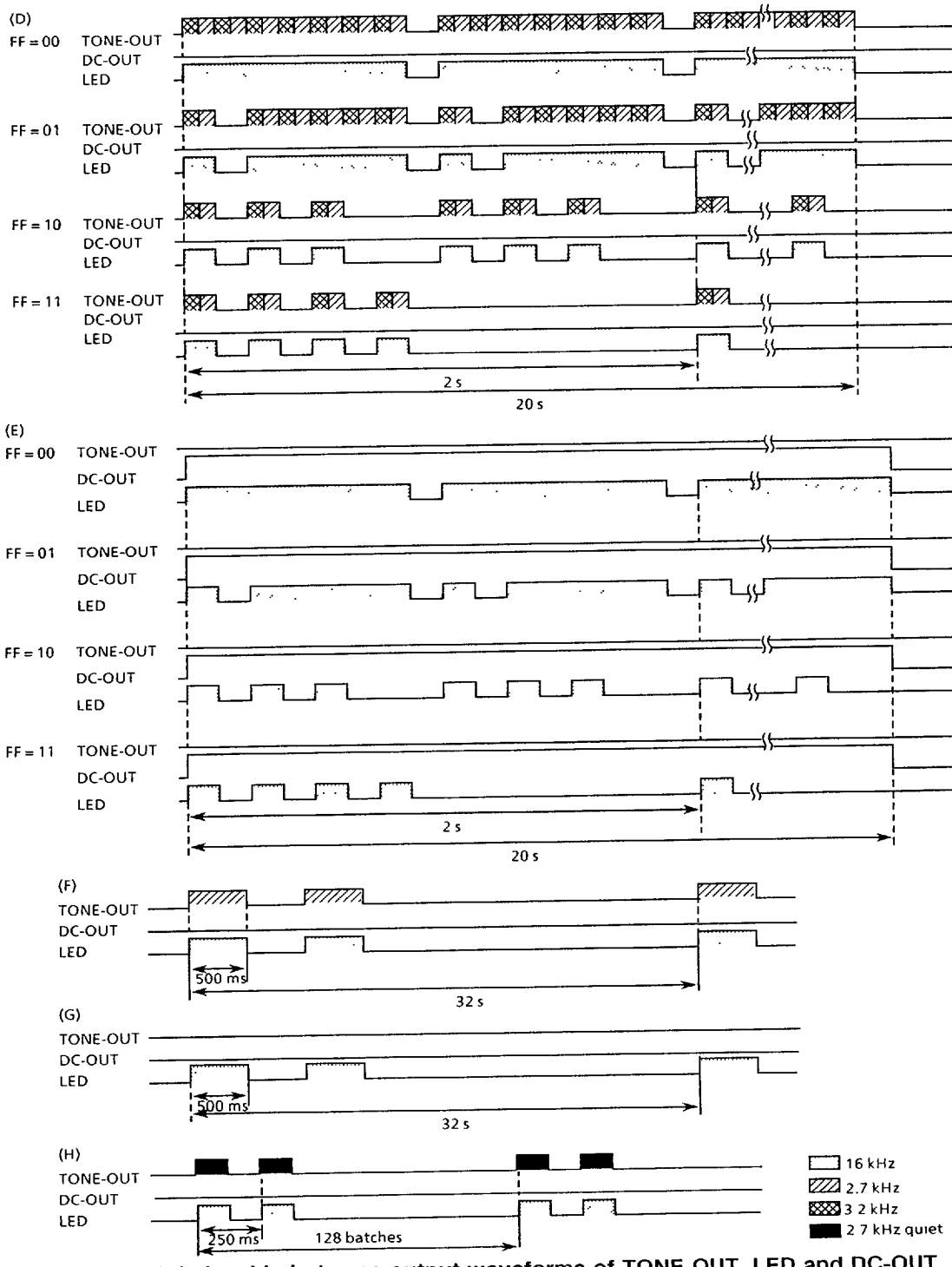


Figure 18-2 Relationship between output waveforms of TONE-OUT, LED and DC-OUT

■ Internal Functions

The S-7038AF has the following functions to support its basic operations:

- Battery save function to reduce power consumption
- Battery low alert function to notify power supply voltage drop
- BCH decode function to automatically correct address and message errors
- Memory function to store received messages in the tone-only pager
- Extension function to enable forcible output of tone

These functions are explained below:

1. Battery save function
   The battery save function turns the RF circuit on and off intermittently to reduce the power consumption of the pager. Two signals are used: BS1 and BS2. BS1 enables the RF circuit. When the BS1 signal is set to high, the RF circuit is turned on. BS2 is the timing pulse to detect preambles and synchronization codes. If BS1 is set to low, SIG-IN does not receive data and does not compensate synchronization.

1.1 BS1

Upon preamble detection: High and low are repeated for each word (32 bits). When BS1 is high, the RF circuit is turned on and preamble detection is enabled.

Upon SY detection: BS1 is set to high to receive POCSAG codes until the initial SY is detected up to 32 words, after preamble signal is detected. If no SY is detected after a period of 32 words, the S-7038AF returns to preamble detection mode. BS1 is also set to high when a consecutive SY is detected. If the S-7038AF fails to detect a consecutive SY more than a number of retries, it returns to preamble detection mode.

After SY detection: The BS1 signal is controlled by the value of the bit/word counter.
BS1 is set to high synchronized with the timing of the frame specified in ID-ROM, and is kept as high until all messages (address only for tone-only pagers) are received. BS1 is set to high 8.5 bits earlier than the specified frame. This supplied power to the RF circuit early enough to allow the RF circuit to be activated (offset time).

For the simultaneous detection mode of preambles and SYs, set the PR bit of ID-ROM to high.

1.2 BS2

Upon preamble detection: BS2 is set to high by eight bits, synchronized with BS1 being set to high.

Upon SY detection: BS2 is set to high by eight or 16 bits (selected by the OF bit of ID-ROM), synchronized with BS1 being set to low.

The following timing that BS2 goes high is available as mask option: goes high after 8 bits when BS1 goes high, until BS1 goes low or preamble is detected.

For the simultaneous detection mode of preambles and SYs, set the PR bit of ID-ROM to high.

1.3 Switching the offset time

BS1 and BS2 are set to high when the frame specified in ID-ROM and a consecutive SY arrive. They are set to high 8.5 bits earlier than the frame specified as the offset time. By setting the OF bit of ID-ROM to high, this time can be changed into 16.5 bits.

Figure 19 shows the timing of battery save operation.

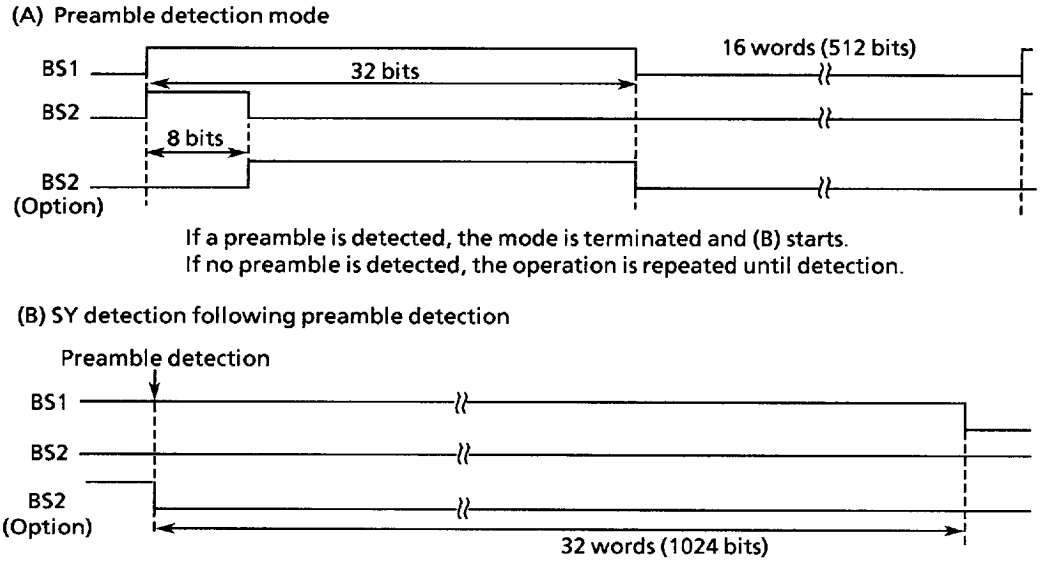


Figure 19-1 Battery saving

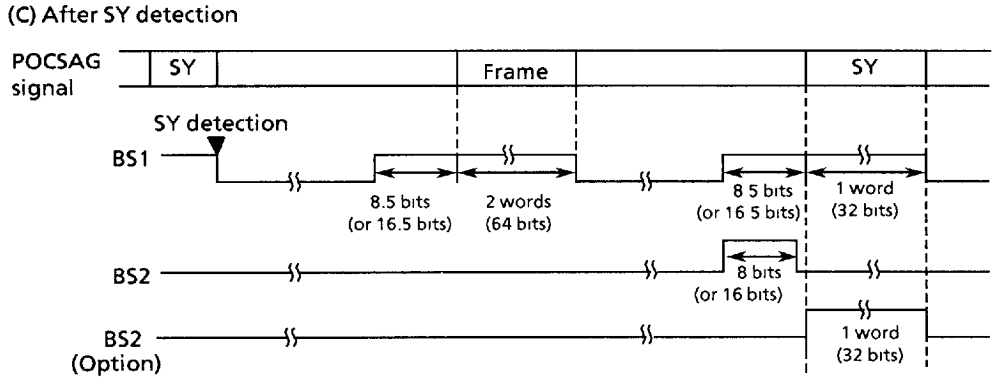


Figure 19-2 Battery saving

2. Battery low alert

Detection signals of an external voltage detector are input from $\overline{\text{BLD}}$ pin, and these levels are sampled. If BLD pin is detected low twice consecutively, the tone signal is output. This tone continues until $\overline{\text{STOP}}$ pin is set to high for 5.3 s at 512 bps or 2.3 s at 1200 bps.
If the sampling overlaps the tone output, it is not detected at that point but at the next sampling point.

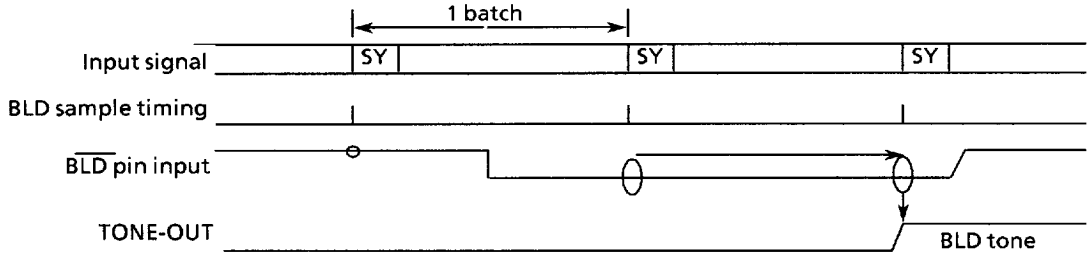


Figure 20 Sampling and detection of power supply voltage

3. BCH decode function
An address or message word consists of 21 valid data bits and 11 check bits. Valid data information is extracted and checked with the check bits. If an error is found, corrections are made according to the number of erroneous bits and 21 valid data bits is extracted. A check bit consists of 10 BCH decode bits and 1 parity bit, as shown in Figure 21.

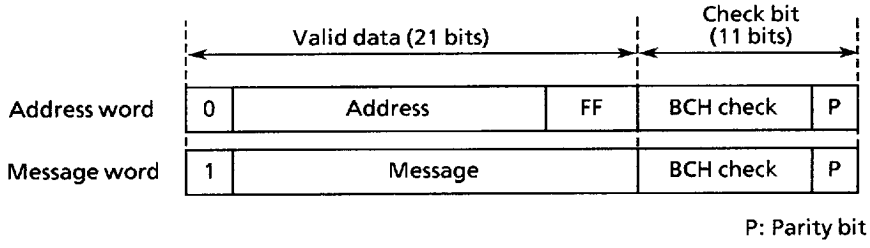


Figure 21 Address and message word configuration

3.1 Error detection based on BCH decode
BCH codes are the result value of the 21 valid data bit divided by the multiple term expression specified by the POCSAG code. By dividing the received address word or message word by the BCH code, the presence and location of error bits are checked. If divisions do not produce any remainder, there are no errors. The remainder value corresponds to the error. The value of the erroneous bits in address words or message words are corrected by the remainder value. The S-7038AF detects three error bits at random. In both address and message words, up to 2 error bits are corrected.
The mask option enables correction of four consecutive bits instead of two random bits.

3.2 Error detection based on parity
Parity bits shall be adjusted so that the total sum of the values (number of bits containing 1 as data) at every 32 bits is an even number. If the total sum is an odd number, it is detected as an error. This parity checks are performed after error correction by the BCH decode. A parity error that occurs after error correction by BCH code is processed as an error.
If an address word is erroneous, that address is ignored. If a message word is erroneous, that message is sent to the CPU with an error code.

Table 6 lists the the error processing statuses for address and message words.

Table 6 Error processing

BCH error	Correction	Parity error	Address word	Message word
0 bit		×	Receivable	Sent to CPU
0 bit			Receivable	Sent to CPU
1 bit	×		Receivable	Sent to CPU
1 bit	×	×	Ignored	Sent to CPU with an error code
2 bits	×		Receivable	Sent to CPU
2 bits	×	×	Ignored	Sent to CPU with an error code
3 bits or more		×	Ignored	Sent to CPU with an error code
3 bits or more			Ignored	Sent to CPU with an error code

4. Memory function (for tone-only pager only)
The memory function stores the received information in the built-in memory, without making a call tone. The memory can store up to four types of information of address types and tone selection bits. On display pagers, this function can be disabled by setting the MM bit of ID-ROM to low.
Besides, the memory function reads call information (scroll), notifies the user of remaining call information in memory (memory remain tone), and prevents redundant calls (block function).

4.1 Basic operation
The S-7038AF enters memory mode by setting $\overline{\text{MEMORY}}$ pin to low. In memory mode, the S-7038AF operates in the same way as in normal mode except that the tone is not output. When a call is received during memory mode, the LED and the vibrator (DC-OUT pin) work. After they stop, the address type and the tone specified by tone selection bits are stored in memory. Up to four calls of memory area are provided. For the fifth and subsequent calls, the oldest call information is erased and new information is written. If $\overline{\text{STOP}}$ pin goes low during a call, the call stops and the call information is stored in memory. At that time, if the same information as that in memory is received, the new information is not written to the memory and the old information remains.
Figure 22 shows the memory write timing. Figure 23 describes how information is stored in memory.

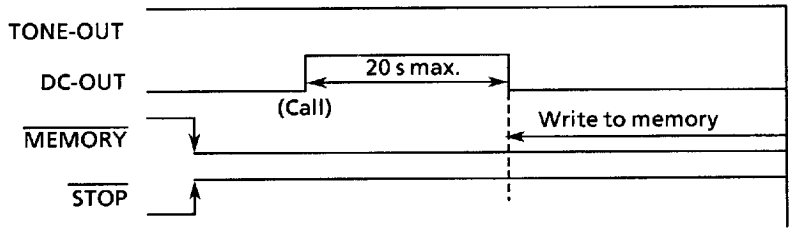


Figure 22 Memory write timing

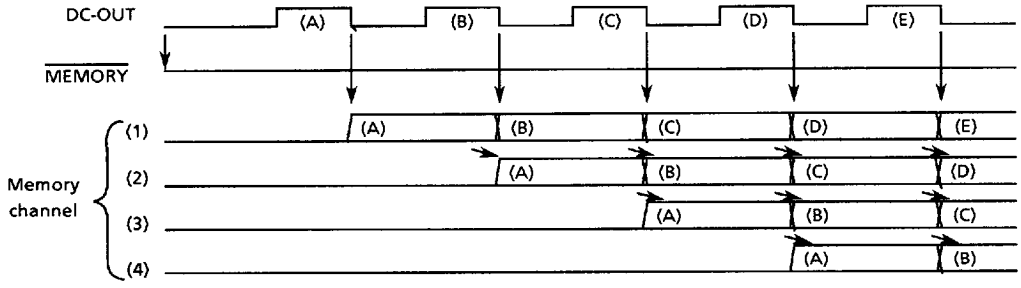


Figure 23 Storing call information in memory

4.2 Memory write in normal mode

Setting the NR bit of ID-ROM to high enables write to memory even in normal mode.

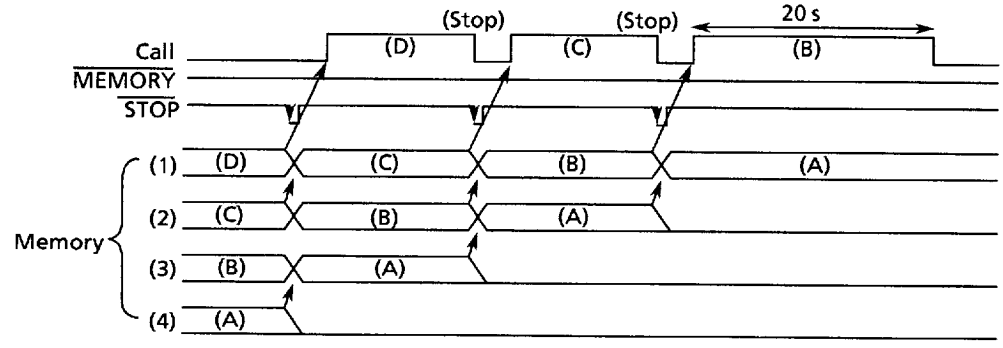
If $\overline{\text{STOP}}$ pin is not set to low during call tone output, the pager user is regarded as being absent and call information is written to memory. The specifications for memory timing are the same as those in memory mode.

4.3 Scroll

"Scroll" means reading call information remaining in memory. The read information is output to the outside by tones or LED. The tones and LED, at that time, operate in the same way as when a call is received. The scrolled information is then erased from memory.

Scroll is executed when the S-7038AF shifts from memory mode to normal mode or when $\overline{\text{STOP}}$ pin is set to low in normal mode. When a scroll starts, a tone is generated 0.5 seconds later. Setting $\overline{\text{STOP}}$ pin to low stops the tone output. If more call data remains in memory, scrolling is performed consecutively.

(1) Scroll by $\overline{\text{STOP}}$ pin



(2) Scroll by $\overline{\text{MEMORY}}$ pin

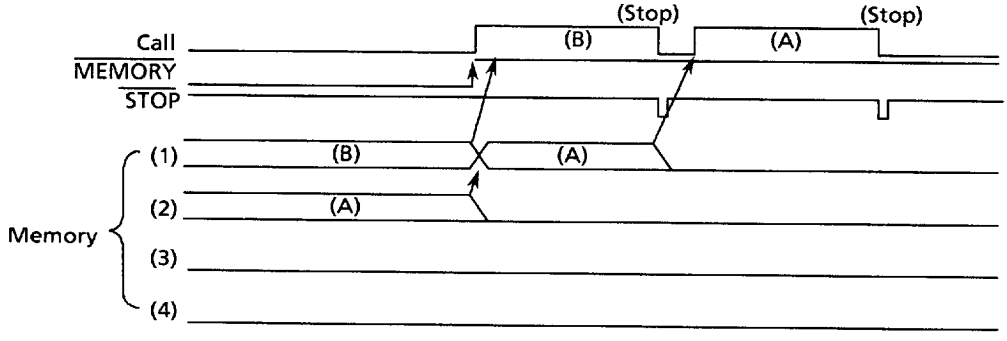


Figure 24 Scroll timing

4.4 Memory remain tone

By setting the MT bit of ID-ROM to high, the memory remain tone can be used to notify the user of the remaining call information in memory. The memory remain tone is a 2.7-kHz quiet tone, and is output when the memory function can be used (the MM bit of ID-ROM is high) and no call has been received in the first 128 batches after the last data was received. Therefore, the memory remain tone is not output in memory mode.

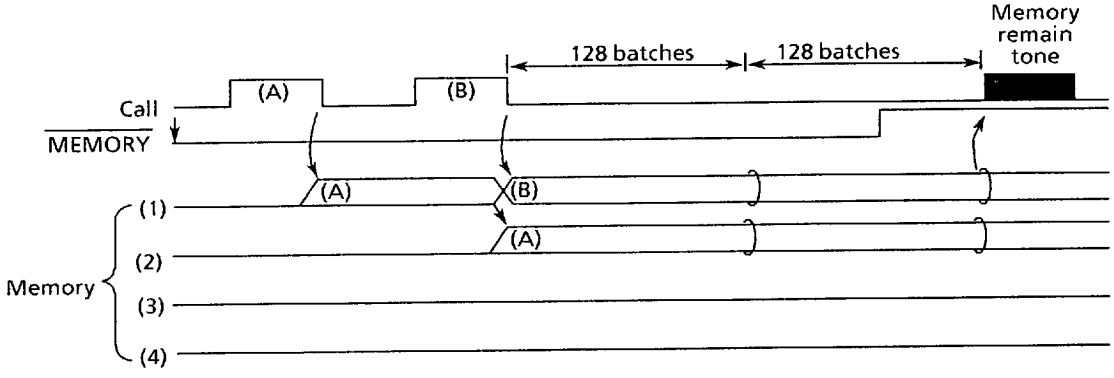


Figure 25 Memory remain tone timing

4.5 Block function

If the received address is already stored in memory, this function avoids redundant calling by ignoring the received address. This function is enabled by setting the BL bit of ID-ROM to high.

For every call, this function checks the call information in memory. If there is identical information, the newly received call is ignored. 64 previous batches, starting at the latest reception are checked.

The information of the call ignored by block function is also transferred to the CPU.

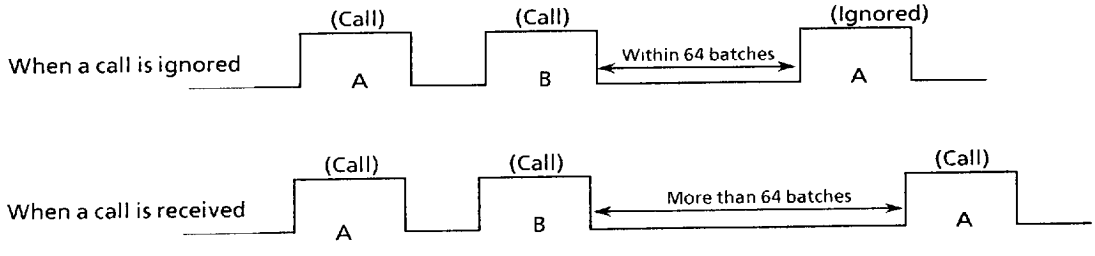


Figure 26 Block function

5. Expansion function

The S-7038AF performs the functions shown in Table 7, with using four pins such as $\overline{TST}$, $\overline{TCK}$, TFNC and TIN. These functions are controlled by the micromcomputer, regardless of IC operation.

Table 7

Input				Function
$\overline{TST}$	$\overline{TCK}$	TFNC	TIN	
×	L	×	H L	Specifies forcibly the contents of all output pins (Valid only when $\overline{RST}$ pin is low)
H	L	H	H/L	Outputs a tone forcibly 2.7 kHz is output when TIN is high, 3.2 kHz is output when TIN is low.
H	L	L	H/L	Outputs a call forcibly

5.1 Forcible specification of output pins

If $\overline{TCK}$ pin becomes low when $\overline{RST}$ pin is low, the same levels as that of TIN pin are output from all output pins but CLK-OUT pin. This function enables the synchronization test of RF circuit when BS1 pin is set to high or low. CLK-OUT pin operates same as usual.

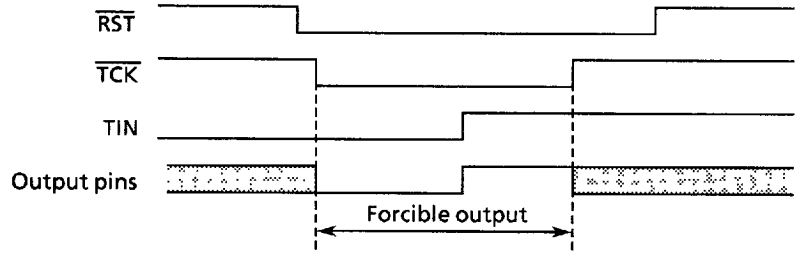


Figure 27 Timing of forcible specification of output pins

5.2 Forcible output of tone

If $\overline{TCK}$ pin becomes low during normal mode, signals are output from TONEOUT and LED, regardless of ID-ROM status. During memory mode, signals are output from DC-OUT (vibrator) and LED. The tone frequency is 2.7 kHz when TIN is high or 3.2 kHz when TIN is low.

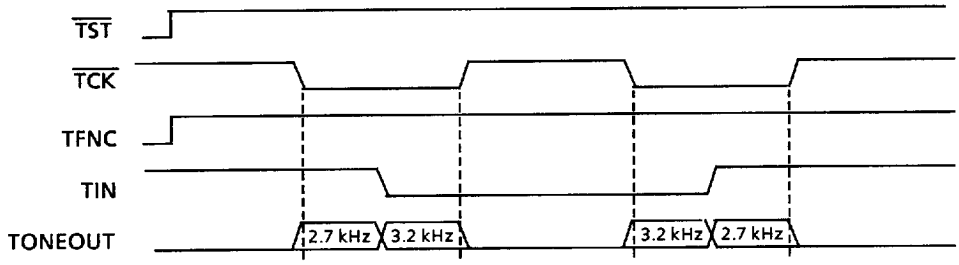


Figure 28 Tone forcible output timing

5.3 Forcible output of call

If TFNC pin becomes low during normal mode, the S-7038AF enters forcible call output mode. This mode transfers a call information to CPU, without generating a calling tone, and the information is not written in the memory. The call signals are output from TONEOUT by a CPU instruction. A calling tone is determined as follows:

1. F1 data is set to TIN pins and 1 pulse is sent to $\overline{TCK}$.
2. F0 data is set to TIN pins and 1 pulse is sent to $\overline{TCK}$.

Then address 2 tone is output when TIN is high, or address 1 tone is output when TIN is low according to Figure 17-2. TIN value must be kept until a call is completed.

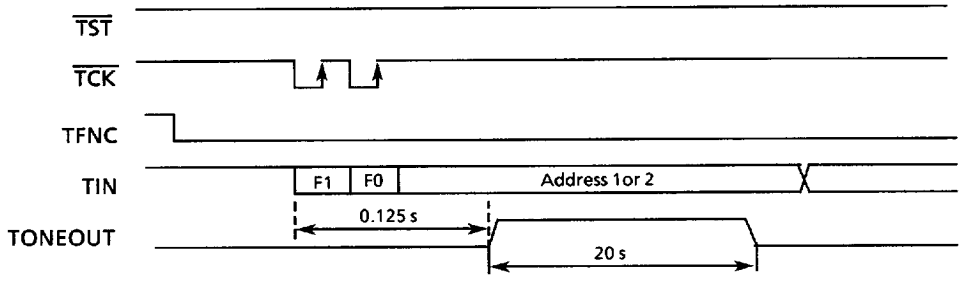


Figure 29 Call forcible output timing

■ Circuit Design

1. Interface to ID-ROM

1.1 ID-ROM assignment

Using S-2913 as an ID-ROM enables direct connection to the S-7038AF. The S-2100, with the mask option, can be used, too. Table 8 describes the ID-ROM functions, and Tables 9 and 10 describe bit allocations.

Table 8

Bit name	Functions
$\overline{UE}$*	Address 1 access enable
U17 to U0	Code setting of address 1 (U17 is MSB.)
$\overline{ME}$*	Address 2 access enable
M17 to M0	Code setting of address 2 (M17 is MSB.)
F2 to F0	Specify frame in a batch (common to addresses 1 & 2)
R3 to R0	Specify times of retrial when SC is not detected
PR	Preamble detection mode H : Simultaneous detection with SC L : Only preamble detection
BL	Block function H : Valid L : Invalid
OF	BS signal rising offset H : 16.5 bits (BS2 is 16 bits) L : 8.5 bits (BS2 is 8 bits)
MM	Memory function H : Valid L : Invalid
NR	Memory function during normal mode H : Valid L : Invalid
MT	Memory remaining alert tone H : Valid L : Invalid
TM	Address generating mixed cadences H : Address 1 L : Address 2
OR**	Unconditional tone output of address 1 H : Valid L : Invalid
TE	Tone output enable H : Valid L : Invalid
T1 to T0	Test mode setting (Don't care bit, do not use)

* When receiving information at address 1, $\overline{UE}$ must be set to low.
Also, when receiving information at address 2, $\overline{ME}$ must be set to low.

** Valid also during the memory mode.

Table 9 S-2913 bit allocation

ROM address	0	1	2	3	4	5	6	7
Bit name	UE	U17	U16	U15	U14	U13	U12	U11
	8	9	10	11	12	13	14	15
	U10	U9	U8	U7	U6	U5	U4	U3
	16	17	18	19	20	21	22	23
	U2	U1	U0	ME	M17	M16	M15	M14
	24	25	26	27	28	29	30	31
	M13	M12	M11	M10	M9	M8	M7	M6
	32	33	34	35	36	37	38	39
	M5	M4	M3	M2	M1	M0	F2	F1
	40	41	42	43	44	45	46	47
	F0	R3	R2	R1	R0	PR	BL	OF
	48	49	50	51	52	53	54	55
	MM	NR	MT	TM	OR	TE	T1	T0

Table 10 S-2100 bit allocation

ROM address	0	1	2	3	4	5	6	7
Bit name	0	UE	U17	U16	U15	U14	U13	U12
	8	9	10	11	12	13	14	15
	U11	U10	U9	U8	U7	U6	U5	U4
	16	17	18	19	20	21	22	23
	U3	U2	U1	U0	ME	M17	M16	M15
	24	25	26	27	28	29	30	31
	M14	M13	M12	M11	M10	M9	M8	M7
	32	33	34	35	36	37	38	39
	M6	M5	M4	M3	M2	M1	M0	F2
	40	41	42	43	44	45	46	47
	F1	F0	R3	R2	R1	R0	PR	BL
	48	49	50	51	52	53	54	55
	OF	MM	NR	MT	TM	OR	TE	T1
	56							
	T0							

1.2 interface

The S-7038AF calls and fetches data in ID-ROM. This operation is controlled by the ROM-CE, ROM-RST, $\overline{\text{ROMCLK}}$, and ROM-DATA pins.

ROM-CE: Chip enable signal of ID-ROM output. If this pin is set to high, the ID-ROM data is fetched.

ROM-RST: Command output. This is a reset signal when the S-2100 is used as the ID-ROM with the mask option.

$\overline{\text{ROMCLK}}$: Clock signal for reading ID-ROM data. Outputs 4 kHz (4.8 kHz for 1200 bps) clock pulses for 64 bits.

ROM-DATA : ID code data input from ID-ROM

Figure 30 shows the interface timing with the S-2913 and Figure 31 shows the interface timing with the S-2100. In the interface with the S-2913, though another 8-bit data is read from the ROM after reading ID-ROM data, the S-7038AF does not fetch it.

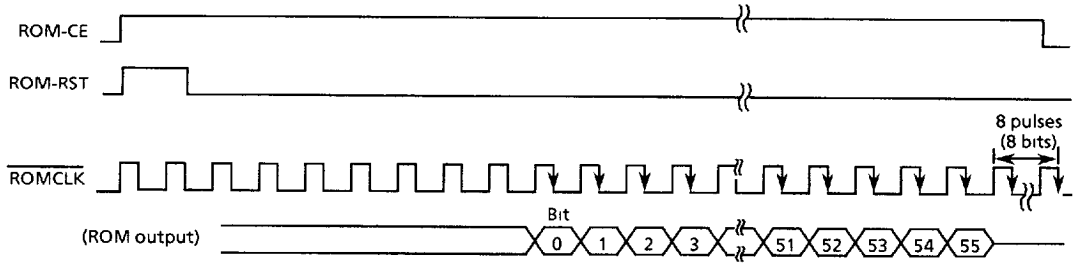


Figure 30 Standard (S-2913 compatible mode) ID-ROM interface

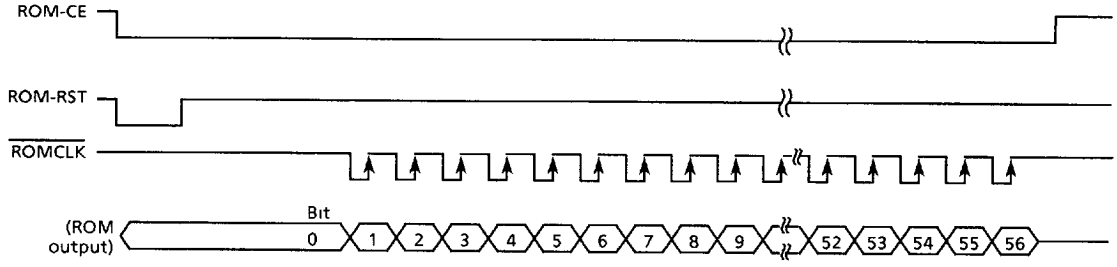


Figure 31 Mask option (S-2100 mode) ID-ROM interface

2. Interface to CPU (for display pager)
To use the S-7038AF on display pagers, a CPU must be installed between the display unit and the S-7038AF. The received data is decoded and sent to the CPU, and the CPU sends the data to the display. The S-7038AF is provided with four signal lines for these purposes.

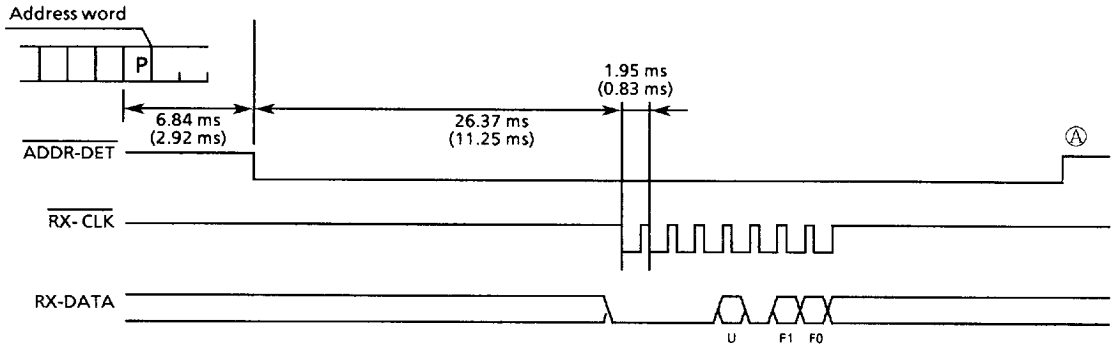
SY-VALID : Indicates that the received POCSAG signal is synchronized (the pager is in the reception area). In preamble detection mode, low is output. Upon SY detection, SY-VALID goes high. When SY-VALID is high, the bit/word counter is synchronized with the received POCSAG signal and can decode it.

$\overline{\text{ADDR-DET}}$: $\overline{\text{ADDR-DET}}$ goes low if address 1 or 2 is detected. When the reception of the message word following the address word is completed, it returns to high.
The message word reception is regarded as being completed in the following cases:
- When the next address word is detected
- When an idle word is detected
- When an SY, inserted between consecutive message words, is not detected
- When the reception of word, upon detection of low level at the $\overline{\text{EOT}}$ pin, is completed

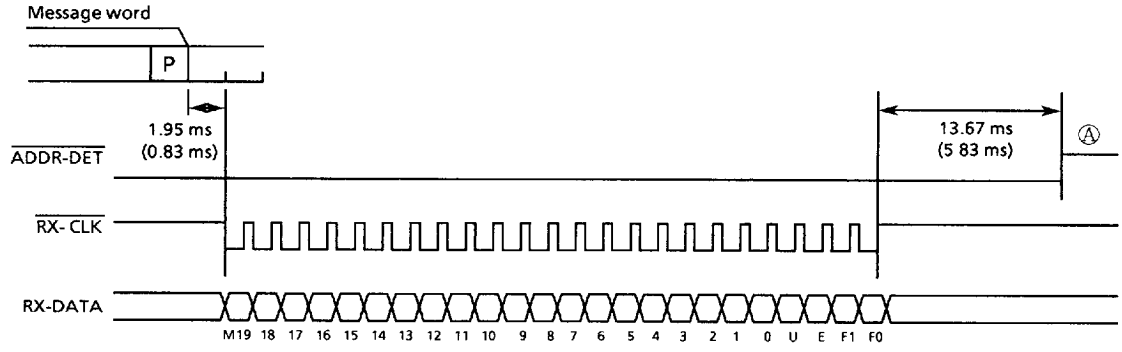
$\overline{\text{RX-CLK}}$, RX-DATA : RX-DATA outputs the received message data to the CPU. $\overline{\text{RX-CLK}}$ outputs a clock signal for sending data. The CPU samples RX-DATA at the falling edge of $\overline{\text{RX-CLK}}$, and fetches data at the rising edge. The following data is output to the CPU.
- Upon address detection, 8-bit data, containing the address type and the tone selection bits, is output.
- Upon message word reception, 24 bits of information is output per message word. The information consists of 20 message data bits, an error bit, an address type data bit, and 2 of tone selection bits.

Figure 32 shows the interface timing of each data item.

(1) Address detection



(2) Message detection



M19 to M0 : Message data
U : Address (0 : Address 1, 1 : Address 2)
E : Transmission error (0 : No error or already corrected, 1 : Error)
F1, F0 : Tone selection for call address
Upper values are for 512 bps, and lower values in parentheses are for 1200 bps.
Ⓐ $\overline{\text{ADDR-DET}}$ is kept to be low when there is a message word after this.

Figure 32 CPU interface timing

3. Application circuit example (in case of 512 bps)

3.1 Tone-only pager

Main peripheral components are ID-ROM, speaker, vibrator, LED, transistor, and crystal oscillator. No CPU is required.

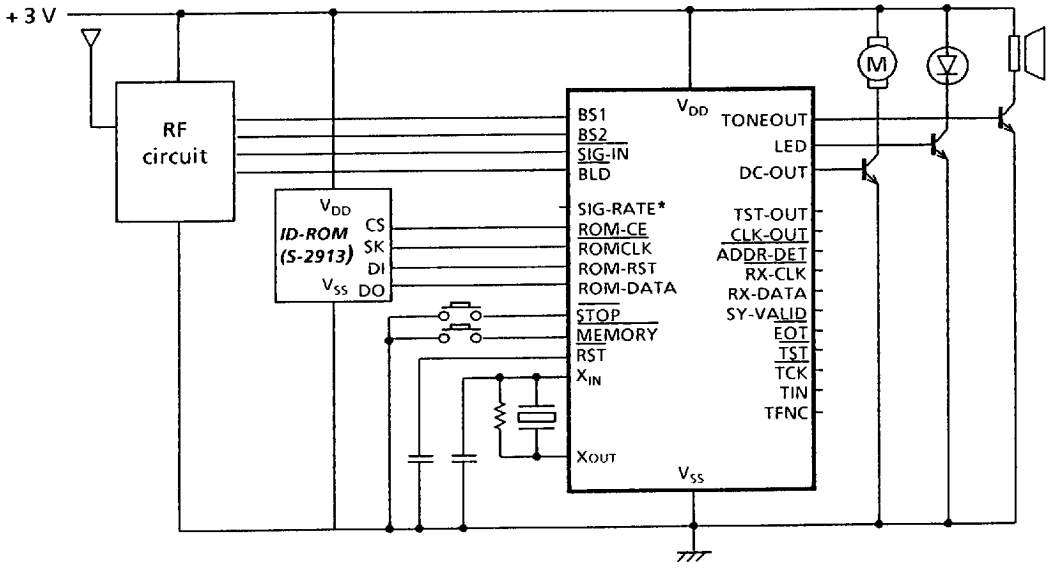


Figure 33 Application circuit example: Tone-only pager

3.2 Display pager

A CPU and a display unit are added to a tone-only pager.

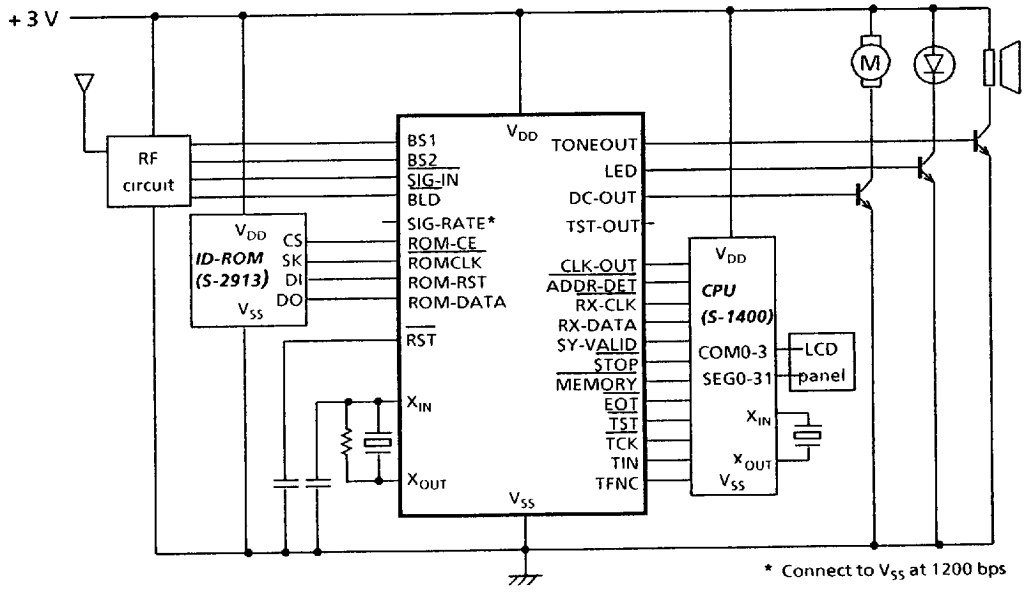


Figure 34 Application circuit example: Display pager