Q2334

DUAL DIRECT DIGITAL SYNTHESIZER

VLSI Products

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- Phase Locked Loop (PLL) Frequency Synthesizers
- DDS and PLL Evaluation Boards
- Viterbi Decoders – 256 Kbps to 25 Mbps Maximum Data Rates
- Pragmatic Trellis Modulation Codecs to 75 Mbps
- Variable Rate Vocoders

May 1995
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Q2334
DUAL DIRECT
DIGITAL SYNTHESIZER
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QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

FIGURES

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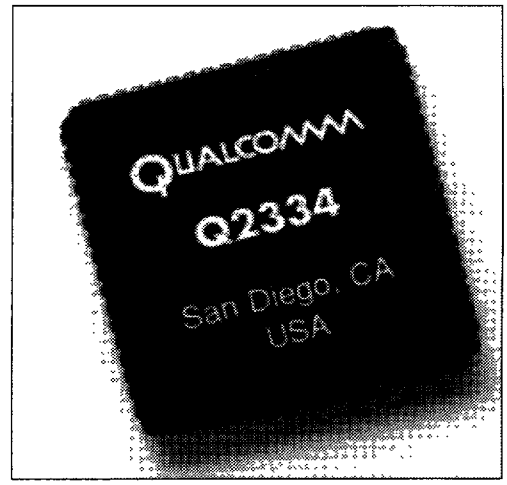
QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

FEATURES

- Two Complete Direct Digital Synthesizer Functions On-chip
- MIL-STD 883 Screened Devices Available
- Processor Interface for Control of Phase and Frequency
- Patented Algorithmic Sine Lookup Function
- Patented Noise Reduction Circuit
- Synchronous PSK and FSK Modulation Inputs
- 2 Maximum Clock Speed Versions: 20 MHz, and 50 MHz
- Phase Resolution: 0.00000008° using Processor-controlled Phase Adjustment
- Double Buffered Registers Allow Synchronous, Phase Coherent Frequency Change
- Simple External Multiplex Control for Binary Frequency Shift Keying (BFSK) Modulation
- Low Power: 267 mW maximum at 20 MHz, and 667 mW maximum at 50 MHz Clock Frequency per DDS
- Evaluation Board Available - Q0310-1
- Built-in frequency ramp function available using internal chirp mode

APPLICATIONS

- Spread Spectrum Modulators
- Quadrature Oscillators
- Programmable Frequency Synthesizers
- Satellite Receivers
- Cellular Base Stations
- Magnetic Resonance Imaging
- VXI-based ATE
- SONAR/RADAR
- Paging Systems
- High Performance Test Equipment
- Digital Radios and Modems
- HF Transceivers
- Local Oscillator Generation for VSAT, DBS, and GPS Applications



INTRODUCTION

The QUALCOMM Q2334 family of Dual Direct Digital Synthesizers (DDS) generates high resolution digitized sine wave signals using phase accumulation techniques combined with a patented on-chip sine lookup and Noise Reduction Circuit (NRC). The Q2334 contains two independent DDS functions controlled from a single microprocessor interface. This interface controls both the phase and the frequency of the generated sine waves as well as the device's operating mode. Synchronous inputs are also provided to allow for phase and frequency modulation.

The Q2334 provides greater than 76 dB rejection of phase truncation spurs and 72 dB amplitude quantization signal-to-noise ratio. Two pin compatible versions of the Q2334 DDS are available: 20 MHz and 50 MHz maximum clock speeds. This synthesizer is ideally suited for applications requiring high resolution sine wave generation, fast phase and frequency switching, and excellent phase and frequency stability.

The two independent on-chip DDS functions provide an efficient technique for implementation of full-duplex systems, quadrature oscillators, and spread spectrum systems.

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

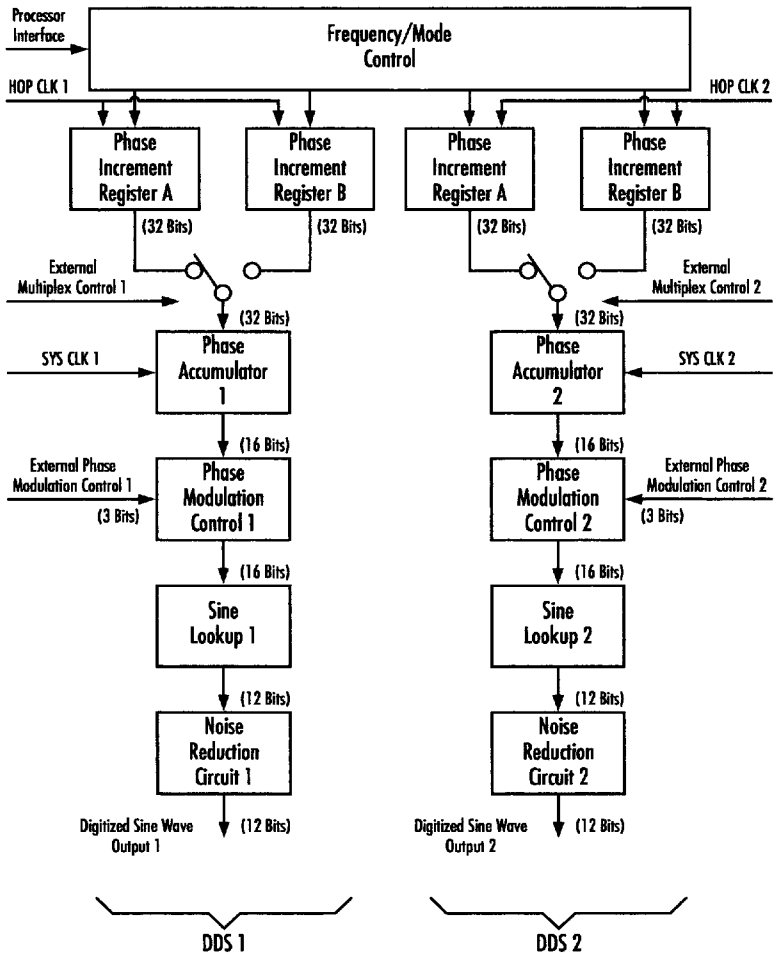
GENERAL DESCRIPTION

The Q2334 device consists of two independent DDS functions, each controlled by a common microprocessor interface, as illustrated in the figure 1 block diagram. Each DDS contains the following:

- Two Phase Increment Registers (PIR), A and B
- External Multiplex (Phase Increment Register) Control
- 32-Bit Wide Phase Accumulator
- 3-Bit External Phase Modulation Control
- Patented Sine Lookup Algorithm (see Patent Reference 1)
- Patented Noise Reduction Circuit (NRC) (see Patent Reference 2)

The processor interface controls the phase and frequency of the Q2334 DDS. The specific mode of the DDS operation is controlled by the Synchronous Mode Control (SMC) register and the Asynchronous Mode Control (AMC) register. The SMC register is double buffered. That is, values loaded into the SMC registers are synchronously enabled when the HOP CLK signal is asserted. The value loaded into the AMC registers does not require activation by any other signal.

Figure 1. Q2334 Dual DDS Block Diagram



QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

Double Buffered Registers

The SMC register and the two PIRs are double buffered. That is, these registers can be loaded at any time using the processor interface, but the values become active only when the signal HOP CLK is asserted. This makes possible the advanced synchronous phase and frequency change features of the Q2334 device which are especially important when using the device in modulation or phase-locked loop applications.

The Asynchronous Hop Clock (AHC) can also be used to activate the double-buffered settings. See the Asynchronous Hop Clock section on page 15 for more information.

Other Registers

The AMC register has an active value once the information has been written to it. This register does not require a HOP CLK signal to become active.

Q2334M-30L MILITARY VERSION DESCRIPTION

The Q2334M-30L is packaged in a 68-pin hermetically sealed ceramic leaded chip carrier (CLDCC). Device assembly is in accordance with MIL-STD-883 for Class B microcircuits. Screening and inspection of all devices is in accordance with Method 5004. Quality conformance inspection requirements of all devices are in accordance with Method 5005 of MIL-STD-883 for Class B microcircuits for Group A and Group B testing.

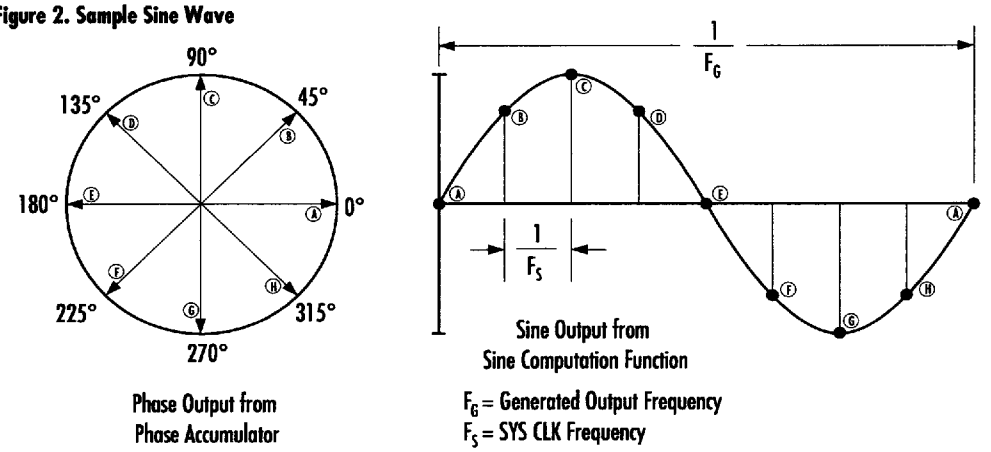
The maximum sustainable junction temperature for the device is +150°C. Based on testing, the Q2334M-30L can be safely rated for continuous operation in still, ambient air at +125°C. Higher ambient conditions may be possible if active cooling or other means to convect thermal energy away from the part is provided. It is the customer's responsibility to perform the necessary thermal calculations for operation above 125°C.

THEORY OF OPERATION

A Direct Digital Synthesizer works on the principle that a digitized waveform of a given frequency can be generated by accumulating phase changes at a higher frequency. Sampling theory requires that the generated frequency be no more than ½ of the clock frequency (Nyquist rate).

Figure 2 shows the phase accumulation of a generated sine wave whose frequency is equal to ⅛th of the clock frequency. The circle shows the phase accumulation process of ¾ at each clock cycle. The dots on the circle represent the phase value at a given time and the sine wave shows the

Figure 2. Sample Sine Wave



QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

corresponding amplitude representation. This phase to amplitude conversion occurs in the sine lookup. Note that the phase increment added during each clock period is ¾ radians, which = ⅛th of 2π.

General Q2334 DDS Operation

The block diagram in figure 1 shows the internal structure of the Q2334 DDS device. The phase value stored in PIRA or PIRB is added to the value in the phase accumulator once during each period of the system clock. The resulting phase value (from 0 to 2π) is then applied to the patented sine lookup once during each clock cycle. The lookup converts the phase information to its corresponding sine amplitude, as is illustrated in figure 2. This value is then passed through the patented NRC, which, when enabled, reduces spur heights caused by periodic repetition of the amplitude quantization error (reference the Noise Reduction Circuit section on page 16). The digital word is then output from the Q2334 DDS device.

Phase Increment Value

To output a particular frequency, the associated phase increment value must be loaded into the PIR. The generated frequency (F_G) and clock frequency (F_S) are related to the phase increment value ($\Delta\phi$) by the following equation:

$$F_G = \frac{F_S \bullet \Delta\phi}{2^N} \qquad (1)$$

where N equals the number of bits in the phase accumulator.

Using this formula, frequency resolution can be generated in exact Hz steps. For example, given a system clock of 30 MHz and a desired generated frequency of 7.5 MHz with a 32-bit phase accumulator:

$F_S = 30$ MHz
$F_G = 7.5$ MHz
$N = 32$

Using formula (1) above

$7.5 \text{ MHz} = (30 \text{ MHz} \bullet \Delta\phi)/2^{32}$
$\Delta\phi = (7.5 \text{ MHz})(2^{32})/30 \text{ MHz}$
$= 2^{30} = 40000000$ (hex)

For example, using 2^{25} Hz (33,554,432Hz) as the clock frequency, an exact decimal frequency (in Hz) can be generated:

Given: $F_S = 2^{25}$ Hz = 33,554,432 Hz
$N = 32$
Frequency Resolution = 2^{25} Hz/2^{32}
= 1 Hz/2^7
Therefore, $F_G = (1 \text{ Hz}/2^7) \bullet \Delta\phi$
if we choose $\Delta\phi = 2^7$ (80 hex),
then $F_G = 1$ Hz
if we choose $\Delta\phi = 2^8$ (100 hex),
then $F_G = 2$ Hz
if we choose $\Delta\phi = 2^7$ (200 hex),
then $F_G = 4$ Hz

Frequency Resolution

Any frequency can be generated by programming the phase change within the bit resolution of the phase accumulator (the Q2334 DDS phase accumulator registers are 32 bits wide). The frequency resolution can be determined by the following formula:

$$\text{Frequency Resolution} = F_S/2^N \qquad (2)$$

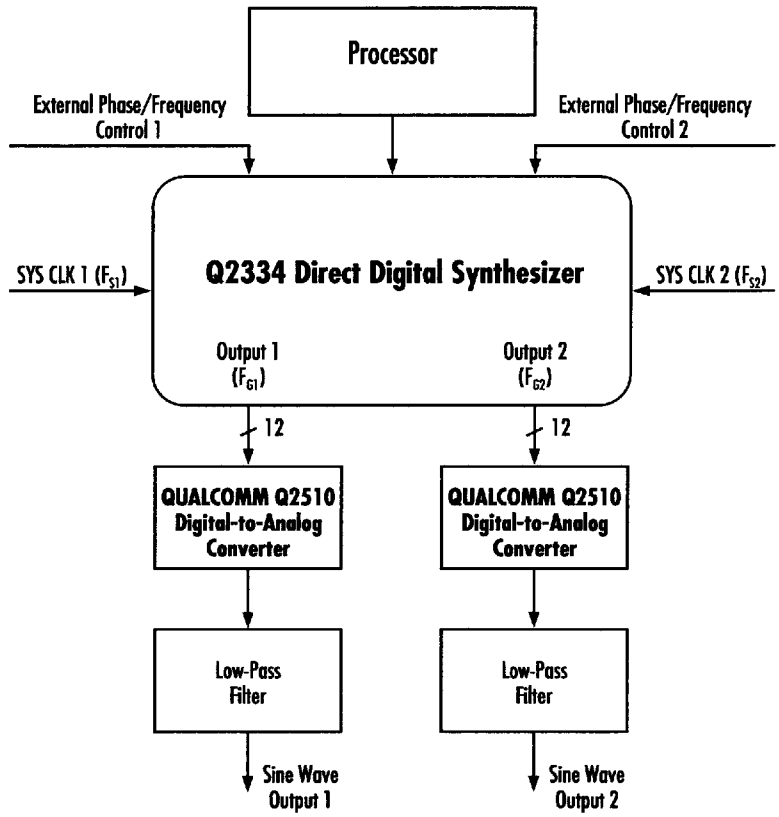
where
F_S = frequency of the system clock
N = # of bits in the phase accumulator

For example, using the Q2334I-20N where the $F_S = 20$ MHz, and N = 32:

Frequency Resolution = 20 MHz/ 2^{32}
= 0.00465 Hz

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

Figure 3. Typical Q2334 DDS Application



Typical DDS Application

Figure 3 illustrates a typical synthesizer application of the Q2334 Dual DDS. This figure shows all of the external functions required for a powerful two-channel synthesizer system. Each digitized sine wave output from the DDS device is converted to an analog waveform by a Digital-to-Analog Converter (DAC). The output of the DAC has the desired sine wave as a major component, but also includes the higher frequency image components due to the conversion of a sampled waveform. A Low Pass Filter (LPF) is used to reduce these image signals to the desired level, as shown in figure 4. The pass band of the LPF should be equal to or less than half the sample frequency.

The two DDS devices contained in the Q2334 function independently and the use of a single clock source or two independent clock sources is supported. The DDS outputs are totally independent from one another unless a relationship is established between the two.

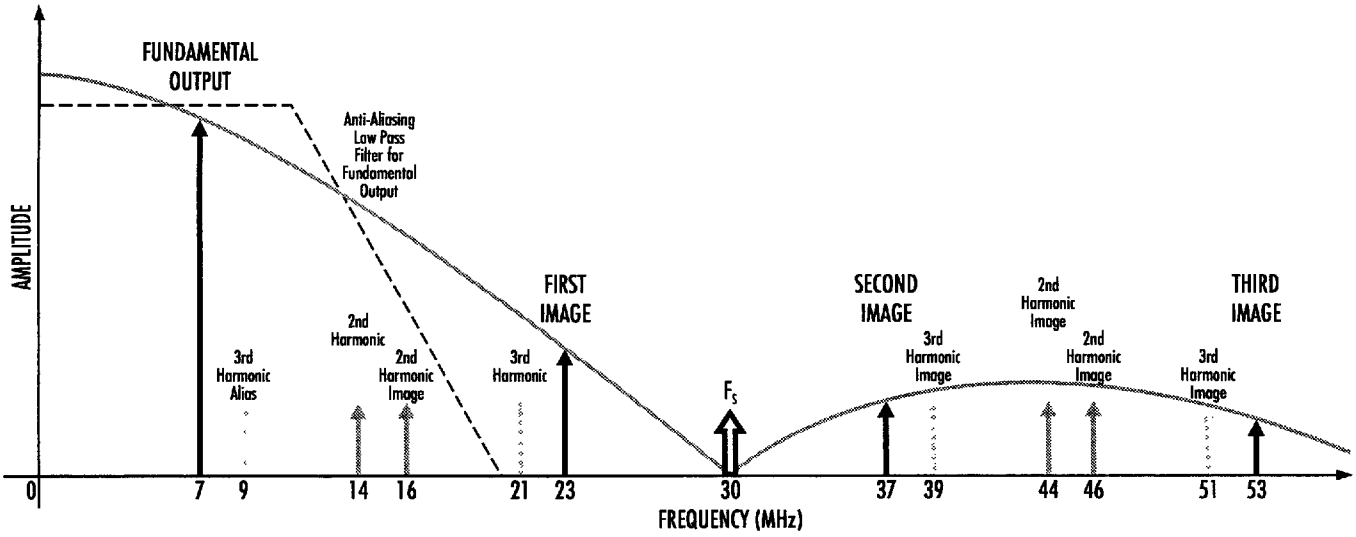
Spectral Purity

The spectral quality of a DDS system is dependent upon a number of factors, including: the phase noise of the clock source; the number of phase bits applied to the sine lookup function (i.e., phase truncation, which is an internal operation of the DDS and cannot be externally influenced); and the number of bits output from the lookup (i.e., amplitude truncation).

The specifications of the DAC, LPF design, and circuit card design also affect the quality of the converted sine wave. The linearity and glitch energy specifications of the DAC are especially important to the generation of pure sine

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

Figure 4. DDS Output Showing Effect of DAC Non-Linearities



wave signals. Careful attention to layout of the printed circuit design is important to limiting the noise of the synthesizer. Digital switching and power supply noise must be limited from coupling with clock and analog signals.

Clock Source

The clock source input to a DDS system is the major contributor to the phase noise of the system, even though its effect is reduced by the frequency division process of the DDS. The phase noise of the DDS output will show an improvement over phase noise of the clock source itself of $20 \bullet \log(F_S/F_G)$, where F_S is the system clock frequency and F_G is the generated frequency.

The frequency accuracy of the clock is propagated through the DDS. Therefore, if the sampling frequency is 1000 PPM higher than desired, the output frequency will be higher by 1000 PPM.

Phase Truncation

The Q2334 accumulates 32 bits of phase information. The 16 Most Significant Bits (MSB) are input to the sine lookup algorithm. This reduced number of phase bits input to the sine lookup function is called phase truncation. Phase Truncation is an internal operation of DDSs and cannot be externally influenced. The truncation of the 16 Least Significant Bits (LSB) is a loss of phase information and contributes errors. However, the spurs caused by phase truncation errors are below 76 dBc.

Amplitude Quantization

Amplitude quantization occurs in the sine lookup process. The lookup takes in 16 bits of phase information and converts it to the equivalent sine amplitude. Since an ideal sine representation would require an infinite number of bits for most values, the value must be truncated. The Q2334 quantizes the values and outputs the 12 MSBs as the sine amplitude representation, which is the current limit of practical high-speed DACs.

Since the sine function is a periodic function, errors associated with the quantization can become highly correlated and produce noticeable spurs. To ensure the highest possible performance, QUALCOMM developed a

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

Noise Reduction Circuit (NRC) to minimize the effects of amplitude quantization (see Patent Reference 2). Reference the Noise Reduction Circuit section on page 16 for more information.

Spurs Due To Sampling And DAC Non-Linearities

The frequencies of the discrete spurs and the amplitude of each are dependent on the ratio of the generated frequency (F_G) to the clock frequency (F_S), as well as the phase relationship of the output waveform to the sample clock. The 12-bit digitized sine output theoretically will provide a broadband signal-to-spurious ratio of 72 dB, again depending on the quality of the DAC and the LPF design as well as the printed circuit characteristics and the phase noise of the clock frequency.

The DDS device is able to generate frequencies from 0 Hz to ½ the frequency of the clock. However, limitations on the slope of the roll off of the LPF determine the practical upper limit of the output frequency to about 40% of the clock frequency. Let F_S indicate the frequency of the system clock, and F_G indicate the generated frequency. Discrete images due to sample rate aliasing will be produced at frequencies of F_S-F_G, F_S+F_G, $2F_S$-F_G, $2F_S$+F_G, and so forth, unless the LPF filters these images to acceptable levels (see figure 4).

Notice a sinc $[(\pi \bullet F_G) / F_S]$ envelope is impressed upon all of the DDS outputs in figure 4 ($\approx\Delta$ 4dB from DC up to $(F_S/2)$).

Modulation Techniques

The use of phase and frequency modulation techniques has become common for the transmission of digital bitstreams through channels ranging from telephone lines to high data rate satellite channels. The Q2334 DDS device provides features which allow the basic frequency synthesis function to be expanded and used for a variety of phase and frequency modulation schemes. Reference the Modes of Operation section beginning on page 20 for more information.

Table 1. Microprocessor Interface Register Address Map

DDS1 REGISTER ADDRESS	DDS2 REGISTER ADDRESS	FUNCTION
00H	10H	Phase Increment A (PIRA) bits 0-7 (LSB)
01H	11H	Phase Increment A (PIRA) bits 8-15
02H	12H	Phase Increment A (PIRA) bits 16-23
03H	13H	Phase Increment A (PIRA) bits 24-31 (MSB)
04H	14H	Phase Increment B (PIRB) bits 0-7 (LSB)
05H	15H	Phase Increment B (PIRB) bits 8-15
06H	16H	Phase Increment B (PIRB) bits 6-23
07H	17H	Phase Increment B (PIRB) bits 24-31 (MSB)
08H	18H	Synchronous Mode Control (SMC)
09H	19H	Reserved
0AH	1AH	Asynchronous Mode Control (AMC)
0BH	1BH	Reserved
0CH	1CH	Accumulator Reset Register (ARR)
0DH	1DH	Reserved
0EH	1EH	Asynchronous Hop Clock (AHC)
0FH	1FH	Reserved

QUALCOMM Incorporated, VLSI Products
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INTERNAL ARCHITECTURE

The Q2334 device includes two identical, independent DDS functions with a common microprocessor interface (see figure 1). Each DDS includes two double-buffered phase increment registers, two mode control registers (SMC, and AMC), a phase increment multiplexer, a phase accumulator, a phase modulation control, a sine lookup function, and a noise reduction function. These components, and the processor interface, are described in detail in the following paragraphs.

Processor Interface

The processor interface is compatible with commonly used 8-bit microprocessors. This interface includes address decoding, chip selection, and write controls to load all on-chip control and phase increment registers. Table 1 provides the register address map for the device. Each register is write-only and is decoded from the five-bit input address bus. It is important to note that the addresses listed as "Reserved" are not used and should not be written.

Phase Increment Registers (PIRs)

Two independent 32-bit phase increment registers (A and B) are provided for each DDS function in the Q2334 device. Each phase increment register is 32-bits wide. Phase Increment Register A (PIRA) of each DDS provides the phase increment for the most basic single-frequency operation. Phase Increment Register B (PIRB) provides the phase increment for a range of functions useful in various modes of operation of the DDS. The 32-bit value for each register is loaded using four 8-bit write operations. As stated previously, each PIR is double-buffered and the phase increment used by the phase accumulator is unaffected by this new stored value until a positive transition in the HOP CLK signal occurs.

Mode Control Registers

Each DDS function on the Q2334 device includes two mode control registers: a Synchronous Mode Control (SMC) register and an Asynchronous Mode Control (AMC) register. The SMC is used for operations that may change throughout the operation of the DDS. The AMC should be setup once during initialization (please note that in figures 5 and 6, the unused bits must be set to "0" for proper operation).

Synchronous Mode Control (SMC) Register

The Synchronous Mode Control (SMC) register is double buffered to update control information, which will affect the actual DDS operation only when synchronously enabled by the transition of the HOP CLK signal. Figure 5 provides the bit definition for this SMC register. Bit 0 (LSB), 4, 5, 6, and 7 are reserved and

Figure 5. Synchronous Mode Control (SMC) Register

D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	HOP CLK PHASE MOD ENABLE (HPME)	EXT MUX ENABLE (EME)	EXT PHASE MOD ENABLE (EPME)	0*

ADDRESS ×8 [hex]

* These bits must be set to 0.

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

should be set to logic "0." The remaining bits of the SMC register are the Hop Clock Phase Modulation Enable (HPME), External Multiplexer Enable (EME), and the External Phase Modulation Enable (EPME). Each of these bits is described below.

Hop Clock Phase Modulation Enable (HPME)

The HPME bit is used when operating in the Internal Phase Modulation mode. When the HPME bit is set to logic "1," the phase increment value stored in PIRB is added to the phase accumulator once each time the HOP CLK signal is asserted. If the Phase Modulation Add Enable (PMAE) bit is set to logic "0", all 32 bits of PIRB are used for the one time. However, if the PMAE bit is set to "1," the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated with the 24 LSB of PIRA.

When the HPME bit is set to a logic "1", the HOP CLK signal is internally extended to two SYS CLK cycles. The two SYS CLK cycles make it possible for the phase accumulator to add the contents from PIRB once, and then switch the process immediately back to PIRA. To disable the Internal Phase Modulation mode, as is the case when you want to reconfigure operation to the basic oscillator mode for example, the HPME bit is reset to "0". The HOP CLK is required to initiate this change and during the HPME's transition from "1" to "0", the HOP CLK is no longer internally extended to two SYS CLK cycles and therefore the accumulation process will still accumulate the contents from PIRB. In order to switch the accumulation process back to PIRA, re-load PIRA with the intended frequency value, then assert another HOP CLK (asserting a successive HOP CLK without re-loading PIRA will not switch the accumulation process from PIRB to PIRA). If desired, the contents of PIRB can be loaded with the same contents intended for PIRA concurrently with the HPME bit being disabled to "0". If this is done, then when the HPME transitions, the output will look as though only PIRA is being accumulated, although the user will want to make sure to re-load PIRA with the desired value and assert another HOP CLK so the accumulation process ends up on PIRA.

External Multiplexer Enable (EME)

The EME bit enables the External Multiplex Control. When this bit is set to logic "1," the EXT MUX signal determines whether the value stored in PIRA or PIRB will be used for the phase accumulation process. The selection on the EXT MUX signal is synchronously activated on the rising edge of the MUX CLK signal when the EME is set to logic "1." If the EME bit is set to logic "0," then the External Multiplex Control is disabled and the signal on EXT MUX is ignored. In this case, the contents of PIRA will be used for the accumulation process.

External Phase Modulation Enable (EPME)

The EPME enables the external phase modulation function. When this bit is set to "1," the PM EXT BITS are read and the corresponding phase offset is latched into the Q2334 each time the PM CLK is asserted. If external phase modulation is not used, set the EPME bit to "0" (see the External Phase Modulation section on page 22).

Asynchronous Mode Control (AMC) Register

The Asynchronous mode Control (AMC) register of each DDS function includes control bits which should only be configured during initialization of the Q2334 device. The AMC commands

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

should be activated before any other commands are asserted to the DDS in order for all commands to be received and processed properly. These control bits, as shown in figure 6, include the DAC Strobe or DAC Strobe Invert (DACSTB, DACSTB/), Phase Modulation Add Enable (PMAE), Output Format, and NRC Enable. Each of these is described below. Bits 4 and 6 of the AMC register are reserved and should be set to "0".

Figure 6. Asynchronous Mode Control (AMC) Register

D7	D6	D5	D4	D3	D2	D1	D0
DAC STB	0*	PHASE MOD ADD ENABLE (PMAE)	0*	OUTPUT FORMAT**	NRC ENABLE BITS***		

ADDRESS ×A [hex]

* These bits must be set to 0.

**Output Format	D3
Two's Complement	0
Offset Binary	1

***DAC SIZE (# OF BITS)	D2	D1	D0
6	0	0	0
7	0	0	1
8	0	1	0
9	0	1	1
10	1	0	0
11	1	0	1
12	1	1	0
DISABLE NRC	1	1	1

DAC Strobe, DAC Strobe Invert (DACSTB, DACSTB/)

The DAC Strobe is a delayed version of the system clock which is provided along with the DAC BIT outputs in order to facilitate strobing this digitized sine value into a sample-and-hold DAC or other register. A non-inverted or inverted DAC Strobe is provided so that DAC devices with different triggering requirements can be easily accommodated. The DAC Output Timing specifications must be synchronized with respect to the falling edge of SYS CLK and are therefore only guaranteed in relation to the falling edge of SYS CLK. Trying to use the DACSTB timing associated with the rising edge of SYS CLK could potentially violate DAC setup time and result in strobing erroneous DAC BIT data.

When the AMC's D7 register is set to a "0", the DAC Strobe is non-inverted in relation to the system clock. This allows the falling edge of DACSTB to be used in compliance with SYS CLK. When the D7 register is set to a "1", the sense of the DAC Strobe is inverted in relation to the system clock. This allows the rising edge of DACSTB to be used in compliance with SYS CLK.

QUALCOMM Incorporated, VLSI Products
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Phase Modulation Add Enable (PMAE)

The PMAE bit is not used unless the HPME bit is set to "1." The PMAE bit controls the way in which the value stored in PIRB is used for the one-time accumulation by the phase accumulator. When the PMAE bit is set to logic "1" and PIRB is active for accumulation, the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated. The 24 LSB of PIRA are used as the 24 LSB of the phase accumulator input value. This technique is useful for systems utilizing the Internal Phase Modulation mode of operation. By storing the synthesizer frequency in the PIRA and modifying only the most significant byte of the PIRB, a 256-state phase modulator is implemented. This feature saves computation time in the processor controlling the DDS operation when a phase modulation system with 256-state (i.e., 360°/256 = 1.41 degrees) phase resolution is adequate. Using only the 8 MSB of PIRB to control the phase modulation allows the user to establish a byte-wide Direct Memory Access (DMA) control from the processor to the DDS function phase modulation register (i.e., PIRB), thus simplifying the processor overhead required to control the DDS function in rapidly switching phase modulation systems. When the PMAE bit is set to logic "0," all 32-bits of PIRB will be accumulated in the phase accumulator when PIRB is active allowing a phase resolution of $360°/2^{32}$, i.e, 84 nano-degrees.

Output Format

The Output Format bit determines the binary coding of the DAC output bits of each DDS function. When this bit is set to logic "1," the DAC output is encoded in offset binary format. When this bit is set to logic "0," the DAC output bits are encoded in two's complement format. Table 2 shows the effect of the setting of the Output Format bit.

Table 2. DAC Output Formats

VALUE	OUTPUT FORMAT = 1 (OFFSET BINARY) MSB LSB	OUTPUT FORMAT = 0 (TWO's COMPLEMENT) MSB LSB
Maximum Value	111111111111	011111111111
...	111111111110	011111111110
...	...	...
...	...	...
Half Maximum + 1	100000000000	000000000000
Half Maximum – 1	011111111111	111111111111
...	...	...
...	...	...
...	000000000001	100000000001
Minimum Value	000000000000	100000000000

NRC Enable

When using the on-chip Noise Reduction Circuit (NRC) function, the number of significant bits to be used from the DAC Outputs must be programmed into NRC Enable bits. The DAC bit-width is encoded in three bits as shown in figure 6. When using a DAC with fewer than 12-bits resolution, the most significant DAC output bits are valid. The NRC function is disabled when the NRC Enable bits are set to 111 (binary).

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E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

The function of the NRC circuit is described in the Noise Reduction Circuit section on page 16.

Accumulator Reset Register (ARR)

Each DDS function on the Q2334 device includes an Accumulator Reset Register (ARR). By writing any value to the ARR, the accumulator reset function is armed. The next time the HOP CLK is asserted the phase accumulator is reset to zero.

Asynchronous Hop Clock (AHC)

Each DDS function includes an Asynchronous Hop Clock (AHC) register. When any value is written to this register, the previously stored values in the double-buffered PIRA, PIRB, and SMC registers are activated. This allows processor control of activation of these settings in an identical fashion as with the assertion of the HOP CLK signal. Note that the HOP CLK signal must be low when the AHC register is accessed in order to activate the new register values. Also note that the timing for the AHC is exactly the same as the HOP CLK signal. Activation of the stored settings occurs within four SYS CLK periods after writing to the AHC register.

Phase Increment Multiplexer Control

The phase increment multiplexer function selects which PIR (A or B) is used for the accumulation process. This multiplexing function provides a simple Binary Frequency Shift Keying (BFSK) interface to the DDS.

The signal EXT MUX controls the selection of the value stored in either PIRA or PIRB. For EXT MUX = 0, PIRA is selected; for EXT MUX = 1, PIRB is selected. The signal MUX CLK enables the selection made by the EXT MUX signal. The selection made by the EXT MUX signal is activated synchronously once during the low-to-high transition on the MUX CLK signal.

The MUX CLK signal is internally synchronized to the SYS CLK signal of the DDS (reference the Asynchronous Input information contained in figure 14 on page 33). The selection of the EXT MUX control may occur as frequently as once every four periods of SYS CLK (reference the External Control Timing information information contained in figure 13 on page 32).

Phase Accumulator

Two 32-bit wide phase accumulators are included in the Q2334 device, one for each DDS function. These Accumulators compute and store the sum of the previously computed phase value and the phase increment value from either PIRA or PIRB once during each period of SYS CLK.

Phase Modulation Control

Using the external phase modulation inputs, PM EXT BIT0-2, the output of the phase accumulator can be offset by phase increments of 45 degrees (from 0 degrees to 315 degrees) without affecting the operation of the phase accumulator. Table 3 shows the phase offset for the possible settings of the 3-bit external phase modulation inputs. These inputs are latched into the DDS function when the signal PM CLK is asserted. Changes in the external phase modulation are synchronized internally to the DDS function. This provides a simple 8-Phase Shift Keying (8PSK) interface to the DDS.

Reference the Modes of Operation section on page 20 for more detailed information on phase modulation.

Sine Lookup Function

The Q2334 DDS implements a patented

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

technique to generate a sine wave lookup (see Patent Reference 1). This algorithm takes the 16 MSB from the phase accumulator to generate a 12-bit sine wave value. Using this high precision lookup function the phase truncation noise of the sine wave output is kept below 76 dB. This technique differs considerably from the traditional method of using a ROM lookup function. This advanced look-up technique provides highly accurate and precise sine wave generation.

Table 3. External Phase Modulation Offset Settings

PM EXT BIT 2	PM EXT BIT 1	PM EXT BIT 0	ABSOLUTE PHASE OFFSET (degrees)
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	180
1	0	1	225
1	1	0	270
1	1	1	315

Noise Reduction Circuit (NRC)

Noise due to amplitude quantization is often assumed to be random and uniformly distributed. However, because a sine wave function is periodic, this is not always the case. At certain output frequencies, amplitude quantization errors become highly correlated, thereby causing spurs.

Spurs associated with round-off errors of the quantized sine wave outputs can be significantly reduced by enabling the on-chip Noise Reduction Circuit (NRC). This patented circuit distributes the noise energy evenly across the frequency band, thus reducing the amplitudes of peak spurious components (see Patent Reference 2).

It is important to properly set the NRC Enable bits, because the operation of the NRC is scaled to the LSB. If an incorrectly sized DAC is specified, performance will be reduced.

If the Q2334 is used to generate narrowband outputs and a low noise floor is required, the signal should be bandpass filtered and the NRC disabled. As stated above, when the NRC is enabled it distributes the noise evenly across the frequency band and raises the noise floor. When the NRC is disabled, the noise floor is slightly lower and the quantization errors show up as discrete spurious. However, since the signal is bandpass filtered, the broadband spurious will be negligible.

The output of the NRC (a 12-bit wide digitized sine wave) is normally connected to an external DAC function. This output value can be encoded in offset binary or two's complement format (see figure 6).

Figures 7 and 8 show typical spectra of the analog converted outputs from the Q2334 device with the NRC enabled and disabled. These spectra were measured with the DDS operating with a 10-bit DAC. The synthesized frequency in each of these figures is 10.8 MHz from a 30 MHz system clock frequency. The measurement frequency spans from 0 to 15 MHz, the resolution bandwidth is

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

Figure 7. Typical Spectrum with NRC Enabled (10-bit DAC)

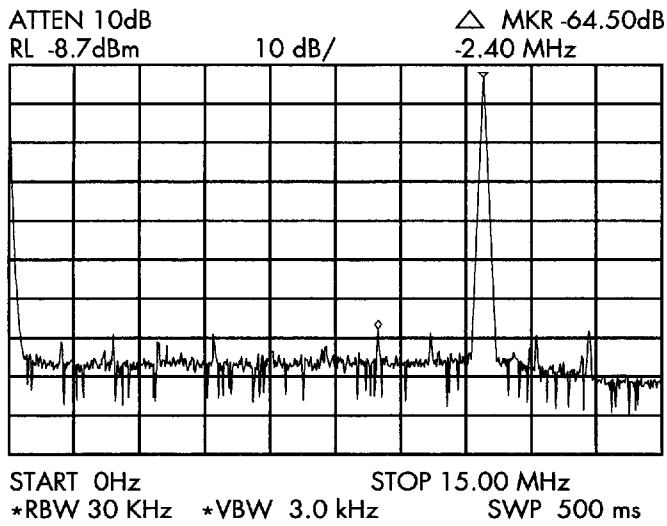


Figure 8. Typical Spectrum with NRC Disabled (10-bit DAC)

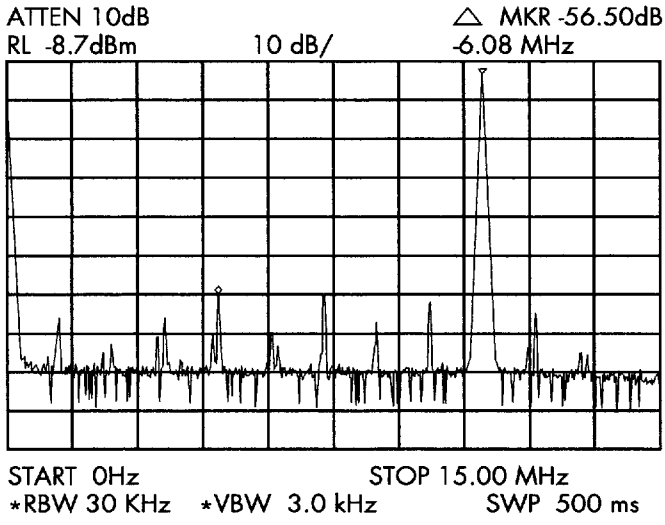
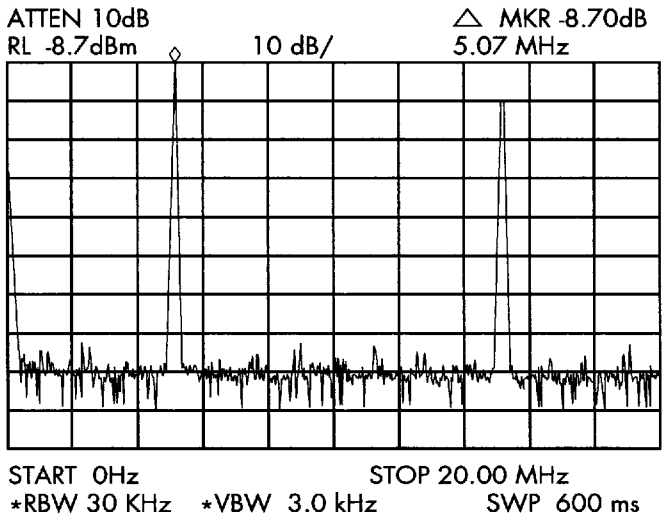


Figure 9. Typical Spectrum with LPF Disabled (10-bit DAC)

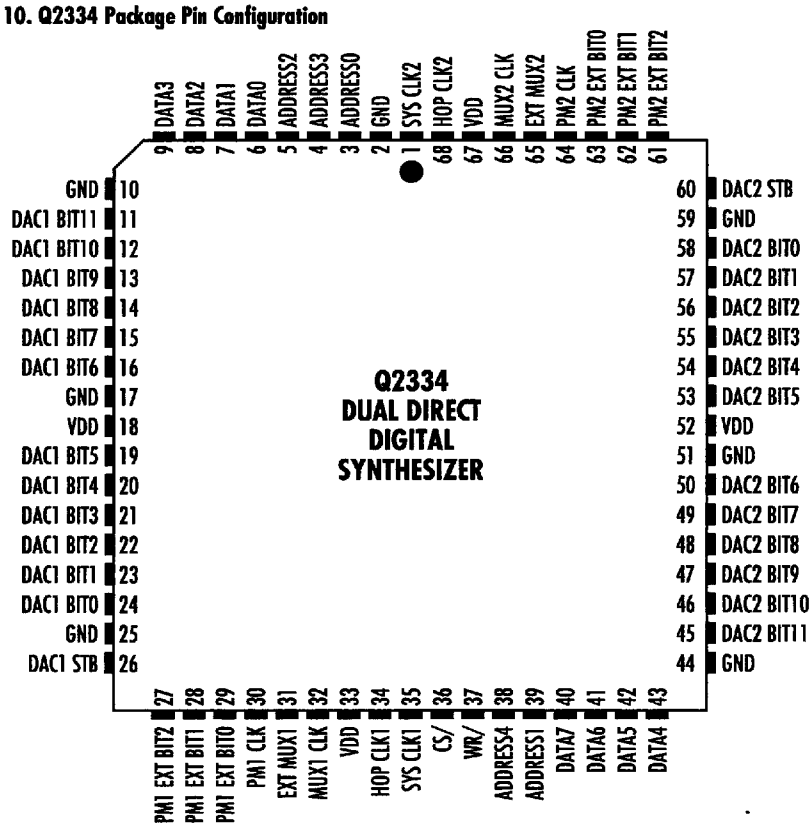


QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

30 kHz, the video bandwidth is 3 kHz, and the scale is 10 dB per vertical division.

Figure 9 shows the typical performance of the Q2334 DDS when operating with a 10-bit DAC with NRC disabled and no LPF. This figure shows a 5 MHz output generated from a 20 MHz system clock frequency and the image at 15 MHz. This 15 MHz spur results from the negative image folded around the 30 MHz clock frequency. This image would normally be filtered by a LPF at the output of the DAC.

Figure 10. Q2334 Package Pin Configuration



INPUT/OUTPUT SIGNALS

Figure 10 provides the pin configuration of the Q2334 DDS package and Table 4 provides a summary of the input/output signal pin assignments.

Signals Common for Both DDSs

The following signals are used in common for both DDS functions on the Q2334 device.

DATA0...DATA7

Inputs (6, 7, 8, 9, 43, 42, 41, 40)

8-bit data bus for writing values to the on-chip processor interface registers. This bus is used for write operations only. DATA0 is the LSB.

ADDRESS0...ADDRESS4

Inputs (3, 39, 5, 4, 38)

5-bit address bus to select the internal processor interface registers. Addresses must be held fixed during the active period of the WR/ signal. ADDRESS0 is the LSB.

CS/

Input (36)

Chip Select. Must be held low during processor write accesses to the Q2334 device. Can be held low all the time.

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

Table 4. Q2334 Input/Output Signals

PIN #	NAME	I/O TYPE	DESCRIPTION	PIN #	NAME	I/O TYPE	DESCRIPTION
1	SYS CLK2	INPUT	System clock to DDS #2	35	SYS CLK1	INPUT	System Clock to DDS#1
2	GND	INPUT	Ground Connection	36	CS/	INPUT	Chip Select - Low during processor writes
3	ADDRESS0	INPUT	Processor Interface address bus-bit 0 (LSB)	37	WR/	INPUT	Writes the value of data bus into register - Active Low
4	ADDRESS3	INPUT	Processor Interface address bus-bit 3	38	ADDRESS4	INPUT	Processor interface address bus-bit 4 (MSB)
5	ADDRESS2	INPUT	Processor Interface address bus-bit 2	39	ADDRESS1	INPUT	Processor interface address bus-bit 1
6	DATA0	INPUT	Processor Interface data bus-bit 0 (LSB)	40	DATA7	INPUT	Processor interface data bus-bit 7 (MSB)
7	DATA1	INPUT	Processor Interface data bus-bit 1	41	DATA6	INPUT	Processor interface data bus-bit 6
8	DATA2	INPUT	Processor Interface data bus-bit 2	42	DATA5	INPUT	Processor interface data bus-bit 5
9	DATA3	INPUT	Processor Interface data bus-bit 3	43	DATA4	INPUT	Processor interface data bus-bit 4
10	GND	INPUT	Ground Connection	44	GND	INPUT	Ground Connection
11	DAC1 BIT11	OUTPUT	DDS#1 Digitized sine wave output-bit 11 (MSB)	45	DAC2 BIT11	OUTPUT	DDS#2 Digitized sine wave output-bit 11 (MSB)
12	DAC1 BIT10	OUTPUT	DDS#1 Digitized sine wave output-bit 10	46	DAC2 BIT10	OUTPUT	DDS#2 Digitized sine wave output-bit 10
13	DAC1 BIT9	OUTPUT	DDS#1 Digitized sine wave output-bit 9	47	DAC2 BIT9	OUTPUT	DDS#2 Digitized sine wave output-bit 9
14	DAC1 BIT8	OUTPUT	DDS#1 Digitized sine wave output-bit 8	48	DAC2 BIT8	OUTPUT	DDS#2 Digitized sine wave output-bit 8
15	DAC1 BIT7	OUTPUT	DDS#1 Digitized sine wave output-bit 7	49	DAC2 BIT7	OUTPUT	DDS#2 Digitized sine wave output-bit 7
16	DAC1 BIT6	OUTPUT	DDS#1 Digitized sine wave output-bit 6	50	DAC2 BIT6	OUTPUT	DDS#2 Digitized sine wave output-bit 6
17	GND	INPUT	Ground Connection	51	GND	INPUT	Ground Connection
18	V_{DD}	INPUT	+5V power supply connection	52	V_{DD}	INPUT	+5V power supply connection
19	DAC1 BIT5	OUTPUT	DDS#1 Digitized sine wave output-bit 5	53	DAC2 BIT5	OUTPUT	DDS#2 Digitized sine wave output-bit 5
20	DAC1 BIT4	OUTPUT	DDS#1 Digitized sine wave output-bit 4	54	DAC2 BIT4	OUTPUT	DDS#2 Digitized sine wave output-bit 4
21	DAC1 BIT3	OUTPUT	DDS#1 Digitized sine wave output-bit 3	55	DAC2 BIT3	OUTPUT	DDS#2 Digitized sine wave output-bit 3
22	DAC1 BIT2	OUTPUT	DDS#1 Digitized sine wave output-bit 2	56	DAC2 BIT2	OUTPUT	DDS#2 Digitized sine wave output-bit 2
23	DAC1 BIT1	OUTPUT	DDS#1 Digitized sine wave output-bit 1	57	DAC2 BIT1	OUTPUT	DDS#2 Digitized sine wave output-bit 1
24	DAC1 BIT0	OUTPUT	DDS#1 Digitized sine wave output-bit 0 (LSB)	58	DAC2 BIT0	OUTPUT	DDS#2 Digitized sine wave output-bit 0 (LSB)
25	GND	INPUT	Ground connection	59	GND	INPUT	Ground connection
26	DAC1 STB	OUTPUT	DDS#1 Synchronous strobe to facilitate clocking the DAC BITs into a DAC	60	DAC2 STB	OUTPUT	DDS#2 Synchronous strobe to facilitate clocking the DAC BITs into a DAC
27	PM1 EXT BIT2	INPUT	DDS#1 Controls the external PM value-bit 2	61	PM2 EXT BIT2	INPUT	DDS#2 Controls the external PM value-bit 2
28	PM1 EXT BIT1	INPUT	DDS#1 Controls the external PM value-bit 1	62	PM2 EXT BIT1	INPUT	DDS#2 Controls the external PM value-bit 1
29	PM1 EXT BIT0	INPUT	DDS#1 Controls the external PM value-bit 0	63	PM2 EXT BIT0	INPUT	DDS#2 Controls the external PM value-bit 0
30	PM1 CLK	INPUT	DDS#1 Enables the values in PM EXT BITs	64	PM2 CLK	INPUT	DDS#2 Enables the values in PM EXT BITs
31	EXT MUX1	INPUT	DDS#1 Controls which PIR is being accumulated	65	EXT MUX2	INPUT	DDS#2 Controls which PIR is being accumulated
32	MUX1 CLK	INPUT	DDS#1 Enables the value on EXT MUX1	66	MUX2 CLK	INPUT	DDS#2 Enables the value on EXT MUX2
33	V_{DD}	INPUT	+5V power supply connection	67	V_{DD}	INPUT	+5V power supply connection
34	HOP CLK1	INPUT	Hop Clock to DDS#1	68	HOP CLK2	INPUT	Hop Clock to DDS#2

WR/

Input (37)

When low while CS/ is low, writes the value of the Data Bus to the register determined by the Address Bus.

V_{DD}

Input (18, 33, 52, 67)

Provides power to all Q2334 circuitry.

GND

Input (2,10,17, 25, 44, 51, 59)

Provides electrical ground reference for signal and power inputs.

Signals Independent for each DDS

The following signals pertain to a specific DDS function (1 or 2) on the Q2334 device.

SYS CLK1, SYS CLK2

Input (35, 1)

Provides the fundamental clock frequency of the synthesized sine waveform. Internal operations of the phase accumulator, external phase

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

modulation, and phase increment registers are synchronized to this clock signal.

HOP CLK1, HOP CLK2

Input (34, 68)

The HOP CLK signal controls the activation of the selection of the double buffered registers. HOP CLK must be active (high) for at least one SYS CLK period and can be asserted once every ten SYS CLK periods.

EXT MUX1, EXT MUX2

Input (31, 65)

When latched into the DDS with the signal MUX1 CLK (or MUX2 CLK) this signal determines which PIR (A or B) will be used for the incremental phase accumulator input value. When the EXT MUX signal is set to "1," the value stored in PIRB will be used by the phase accumulator. When the EXT MUX signal is set to "0," the value stored in PIRA will be used.

MUX1 CLK, MUX2 CLK

Input (32, 66)

The rising edge of this signal latches and enables the value on the EXT MUX inputs. This signal must be held high for a minimum of three SYS CLK periods. Activation of the EXT MUX inputs is synchronized internally to SYS CLK.

PM1 EXT BIT0...PM1 EXT BIT2, PM2 EXT BIT0...PM2 EXT BIT2

Inputs (29, 28, 27, 63, 62, 61)

External phase modulation inputs which control 45 degree phase offsets in the phase accumulated values in accordance with the settings provided in Table 3. PM EXT BITs are active when the signal PM CLK is asserted and are synchronized internally to the DDS function to SYS CLK.

PM1 CLK, PM2 CLK

Input (30, 64)

The rising edge of this signal latches and enables the value on the PM EXT BIT inputs. This signal must be held high for a minimum of three SYS CLK periods. The PM EXT BIT inputs are synchronized internally to SYS CLK.

DAC1 BIT0...DAC1 BIT11, DAC2 BIT0...DAC2 BIT11

Outputs (24, 23, 22, 21, 20, 19, 16, 15, 14, 13, 12, 11, 58, 57, 56, 55, 54, 53, 50, 49, 48, 47, 46, 45)

Digitized sine wave outputs encoded in offset binary or two's complement format, depending on settings in the AMC Registers. One sample is generated during each period of SYS CLK. DAC BIT 0 is the LSB.

DAC1 STB, DAC2 STB

Output (26, 60)

Provides a synchronous strobe to facilitate clocking of the DAC BIT outputs into an external register or sampled DAC. One DAC STB is generated during each period of SYS CLK. Essentially, the DAC STB (or DAC STB/) is a delayed version of SYS CLK.

MODES OF OPERATION

Each DDS can be independently set to perform a wide range of expanded functions of the basic operation, as described in the following paragraphs.

Basic Synthesizer Mode

In its most basic operational mode each DDS on the Q2334 device can provide a fixed frequency digitized sine wave output. The frequency of this sine output is determined by the frequency of the clock input and the value stored in the PIRs (see formula (1) in the Phase Increment Value section on page 7).

To set the Q2334 up in a single frequency output mode, the SMC should

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

be set to "00" (hex). The AMC should be set according to the size of the DAC selected and the desired output format. The PMAE bit should also be set to "0" (reference the *Simple Oscillator Mode* example section on page 24).

Phase Modulation Mode

The Q2334 provides two means to implement phase modulation of a basic frequency output, referred to as Internal Phase Modulation and External Phase Modulation.

Internal Phase Modulation provides extremely fine resolution up to 0.00000008° of the phase adjustment (2^{32} - state phase resolution), while External Phase Modulation is designed for 45° increment phase shifts.

Internal Phase Modulation

Internal Phase Modulation operates as a differential phase adjustment technique and requires use of the processor interface. The Internal Phase Modulation mode is activated by loading PIRA with the correct phase increment for the basic frequency without phase modulation. PIRB is then loaded with the phase increment value equal to the phase increment value stored in PIRA plus the value of the desired phase offset. The phase accumulator uses PIRA for most phase accumulations.

Setting the HPME bit in the SMC register to logic "1" arms the DDS to use the 32-bit value in PIRB for one phase accumulation cycle when the signal HOP CLK is asserted. Since the phase increment value in PIRB is only used once for each HOP CLK assertion, the net effect is to cause a phase change to the generated sine wave.

When the PMAE bit is set to logic "1," the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated with the 24 LSB of PIRA. This 32-bit value is used for one-time accumulation. If PMAE is "0," all 32 units of PIRB will be used for the accumulation.

The one-time phase shift occurs every time the HOP CLK signal is asserted. The phase shift can occur as often as the HOP CLK signal can be asserted (see Processor Interface Timing shown in figure 11 on page 30).

If it is desired to change the phase offset value, PIRB must be reloaded before the HOP CLK cycle with the new phase offset for the next HOP CLK period. The HPME bit will remain set to "1" until reset by the processor (reference the Hop Clock Phase Modulation Enable section on page 12).

External Phase Modulation

External Phase Modulation operates as an absolute phase adjustment technique and utilizes special synchronous inputs separate from the processor interface. When using the External Phase Modulation mode, the phase increment value for the unmodulated input is written into PIRA. PIRB is not used in the External Phase Modulation mode.

The External Phase Modulation Enable (EPME) bit in the SMC register is set to logic "1" to enable the External Phase Modulation mode. When the EPME bit is set to "1," the phase offset determined by the PM EXT BITs are latched into the DDS function each time the signal PM CLK is asserted. This PM EXT BIT setting causes a phase offset in 45° increments as indicated in table 3. This mode of operation allows very simple control of the DDS as a binary, quartenary, or 8-ary phase shift keyed (8PSK) modulator.

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

Binary Frequency Shift Keying (BFSK) Modulation Mode

Two PIRs are provided for each DDS function allowing for Binary Frequency Shift Keyed (BFSK) modulation without any additional hardware. The Q2334 provides signals allowing this switch to occur synchronously.

BFSK Modulation is achieved by setting the phase increment value in PIRA to generate the first frequency and the value in the PIRB to generate the second frequency. The EME bit is then set to logic "1" to enable the external multiplexer controls.

If the EXT MUX signal is set to logic "1," when the MUX CLK signal is asserted the phase accumulator will choose the phase increment value from PIRB. If the EXT MUX signal is set to logic "0," when the MUX CLK is asserted the phase accumulator will choose the phase increment value from PIRA. Changing the value of the EXT MUX input causes the alternation between the frequency controlled by PIRA and the frequency controlled by PIRB.

After the BFSK mode is set up and the PIRA and PIRB contents are active, the EXT MUX signal can be changed as fast as the MUX CLK can be asserted (see External Control Timing shown in figure 13 on page 32). The MUX CLK timing is the only restriction on how fast the accumulation can be switched from PIRA to PIRB.

One of the major advantages of DDS techniques over traditional frequency synthesis methods is this ability to instantaneously switch frequencies while maintaining phase continuity.

Minimum Shift Keying (MSK) Modulation Mode

The Minimum Shift Keying (MSK) Modulation mode is a subset of the BFSK mode described above. The operation is the same, but the two frequencies are selected at a known mathematically determined rate. The MSK Modulation mode is linear MSK and can be generated by setting the frequency shift rate equal to the separation between the two frequencies. This is where MSK got its name, since it is the minimum spacing between the two frequencies that can be accomplished while still recovering the signal with a given shift rate. If the frequency spacing is closer than the frequency shift rate, the information cannot be recovered. If the spacing is too far apart, the information can be retrieved using FSK demodulation techniques, although MSK will not be generated from the resultant spectra. To produce the two MSK frequencies, the values in PIRA and PIRB correspond to incrementing and decrementing phase values (respectively) that must change through ±90 degrees for each symbol time of the frequency shift rate. This is obtained by loading PIRA and PIRB with frequency values such that the mid-point value between them is separated by ± FSK rate/2. This must occur without any phase discontinuities but since the DDS changes frequencies in a phase continuous fashion, this is not a problem. The overall result due to the slow phase transitions between the frequencies is a reduction in the high-frequency spectral content, thus attenuating the sidelobes. The spectrum is said to be more efficient since more power is contained in the main lobe and less in the sidelobes. The EME bit of the SMC register is set to logic "1," as in the BFSK mode, and the EXT MUX and MUX CLK signals control the shift between the values of PIRA and PIRB.

Frequency Hopping Mode

Simple frequency hopping can be enabled

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

by writing a new phase increment value of the desired frequency in PIRA. Since PIRA is a double buffered register, this value will be activated at the next assertion of the HOP CLK signal.

Assuming each frequency to be generated requires all 32 bits to be changed, then four 8-bit writes to PIRA would be needed (see Processor Interface Timing shown in figure 11 on page 30). After PIRA has been loaded, the assertion of the HOP CLK will activate these settings and the resulting frequency will be output from the Q2334 within 31 clock cycles. The frequency value can be changed as fast as the new phase increment value can be written to PIRA and a HOP CLK signal asserted (also see figure 11 on page 30). Once all 32 bits have been activated, the contents will remain until the register is written again. Subsets within the register may also be written. This allows for the changing of an existing register value using a single 8-bit write as opposed to four 8-bit writes.

PIPELINE DELAY

The output of the Q2334 DDS will reflect the change in status activated by the HOP CLK within 30 to 31 SYS CLK periods. When the EXT MUX signal is enabled, the associated PIR will affect the output in 29 to 30 SYS CLK periods after the MUX CLK has been asserted. If External Phase Modulation is implemented, the phase shift will occur 28 to 29 SYS CLK periods after the rising of the PM CLK.

The one SYS CLK ambiguity occurs because the MUX CLK, PM CLK, and HOP CLK signals are allowed to be asynchronous in relation to the SYS CLK. To keep the internal operation of the Q2334 synchronous, the signals are input to synchronizing circuitry which resolves the signal to within one clock period.

To guarantee the synchronous operation with a fixed delay, follow the setup and hold times given with the Synchronous Specifications for Asynchronous Inputs shown in figure 14 on page 33.

TYPICAL EXAMPLES AND INITIAL SETUP OPERATIONS

The Q2334 offers many flexible and powerful operational modes, each of which requires a slightly varying setup to implement. These examples are intended to assist the designer in understanding the "flow" of these setup procedures.

During the following examples, it is assumed that the DDS 1 function will be used. If the DDS 2 function is to be used, all address references should set the most significant digit to "1" instead of "0" as shown for DDS 1. It is also assumed that the NRC circuit is to be used and that these applications are implementing a 10-bit wide D/A converter using offset binary notation. If your application differs from the above specifications, please make the appropriate changes. Some specific configuration steps and additional setup comments, which are common to all the modes of operation, are listed below to alleviate their redundancy in the accompanying examples.

1.) Set the configuration of the D/A converter into the Asynchronous Mode Control (AMC) register, address "0A" (hex). This is accomplished by writing a value of "0C" (hex) to address "0A" using a write procedure which complies with the timing requirements shown in figure 11 on page 30. This sets the AMC register value to operate with an Offset Binary notation D/A converter which is 10-bits wide.

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

2.) The DDS accumulator may be set to be reset to the zero-phase output by "arming" the Asynchronous Reset Register (ARR). This step is performed by writing any data value to address "0C" (hex) . This step is optional. This reset function will become active at the next HOP CLK signal and essentially gives the output signal a zero-phase starting point.

3.) None of the settings written to the Q2334 DDS device will be activated until the assertion of a Hop Clock signal. This may be performed by pulsing the HOP CLK signal to an active high level according to the timing requirements shown in figure 11 on page 30 and figure 13 on page 32. Alternatively, this assertion of the Hop Clock signal may be performed by writing any data value to the Asynchronous Hop Clock (AHC) register (address "0E" (hex)). The change is instantaneous, there is no settling time associated with DDS because it is a digital device. The change is also phase coherent.

Simple Oscillator Mode

When using the Simple Oscillator mode, the Q2334 DDS outputs a digitized sine wave at a fixed frequency ranging from essentially D.C. to one-half the frequency of SYS CLK. Practical limitations on anti-alias filtering will limit the range of frequencies to a maximum of approximately 40% of the SYS CLK frequency.

During the following example the desired output frequency is ¼ of the SYS CLK frequency. That is, if the SYS CLK frequency is 30MHz, the desired output frequency is 7.5MHz. The following steps should be followed:

1.) Set the mode of the device to be the "simple oscillator" mode. It is not necessary to reset the device prior to this first step. Setting the operation mode is accomplished by disabling all modes in the "Synchronous Mode Control" (SMC) register, address 08(hex). In this case, the value of "00" (hex) should be loaded into this device. This is performed by setting the address bus (ADDRESS0 through ADDRESS4) to "08" and the data bus (DATA0 through DATA7) to "00". Set the Chip Select signal (CS/) to active "0" and pulse the Write Strobe (WR/) low according to the timing requirements shown in figure 11 on page 30. The PMAE bit D5 of the AMC register is set to "0" because the internal phase modulation operation is disabled.

2.) The actual phase increment value (32-bits) is next loaded into the Phase Increment Register A (PIRA), addresses "00" through "03" (hex). The least significant byte of the 4-byte value is written into address "00" and the most significant byte is written into address "03". The write operations are performed using the process described in Step 1 and four such operations are required to load all four byte-wide PIRA register addresses. For this example of a desired output frequency which is ¼ of the SYS CLK frequency, the 32-bit value to be written to PIRA is "40000000" (hex) using formula (1) in the Phase Increment Value section on page 7.
In this case, the registers at address "00", "01", and "02" are written with a data value of "00" while address "03" is written with a data value of "40" (hex).

3.) The assertion of a Hop Clock signal will cause the Q2334 device to begin synthesizing an unmodulated sine

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wave at a frequency equal to ¼ the frequency of the SYS CLK input.

Binary Frequency Shift Keying (BFSK) Mode

The following procedure will initialize the Q2334 device to operate in the BFSK mode. For this example, the desired frequencies to be generated are ¼ and ⅛ of the SYS CLK frequency. That is, if the SYS CLK frequency is 30MHz, the desired output frequencies are 7.5 MHz, and 3.75 MHz respectively.

It is assumed that the phase increment value associated with generating 7.5 MHz will be stored in PIRA and 3.75 MHz will be stored in PIRB. The following steps should be followed:

1.) It is not necessary to reset the device prior to this step. Setting up the BFSK mode is accomplished by disabling all modes in the "Synchronous Mode Control" (SMC) register, address "08" (hex) except EXT MUX ENABLE (EME) bit D2. The EME bit should be set to logic "1." In this case, the value of "04" (hex) should be loaded into this device. This is performed by setting the address bus (ADDRESS0 through ADDRESS4) to "08" (hex) and the data bus (DATA0 through DATA7) to "04" (hex). Set the Chip Select signal (CS/) to active "0" and pulse the Write Strobe (WR/) low according to the timing requirements shown figure 11 on page 30. The PMAE bit D5 of the AMC register is set to "0" because the internal phase modulation operation is disabled.

2.) The actual phase increment values (32-bits) are loaded into their respective Phase Increment Register. For PIRA, use addresses "00" through "03" (hex) and for PIRB use addresses "04" through "07" (hex). The least significant byte (LSB) of the 4-byte value is written into address "00" (PIRA) or "04" (PIRB) and the most significant byte (MSB) is written into address "03" (PIRA) or "07" (PIRB). The write operations are performed using the process described in Step 1. Since the phase increment registers are 32-bits wide, four such operations are required to load all four byte-wide PIRA and PIRB register addresses. For this example, the 32-bit phase increment value to be written to PIRA is "40000000" (hex) using formula (1) shown on page 7. In this case, the registers at address "00", "01", and "02" are written with a data value of "00" while address "03" is written with a data value of "40" (hex). The 32-bit phase increment value to be written to PIRB is "2000000" (hex) using formula (1) shown on page 7. In this case, the registers at address "04", "05", and "06" are written with a data value of "00" while address "07" is written with a data value of "20" (hex).

3.) The EME bit is set to logic "1" to enable the external multiplexer controls. This will make the settings at the EXT MUX1 pin (pin 31) select which PIR to use for accumulation purposes. If EXT MUX1 is set to logic "1" then PIRB will be accumulated, if it is set to logic "0" then the contents of PIRA will be accumulated.

External Phase Modulation Mode

When using the External Phase Modulation mode, the Q2334 DDS has the capability to shift its output signal in 45° increments from 45° to 315°. Since the Q2334 is a dual device, it is ideal to use as a quadrature oscillator because it requires only one Q2334 device; this is further described in the *Application Examples and Frequently Asked*

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6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
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Questions section under the *Quadrature Signal Generation with the Q2334* subsection.

The following procedure will initialize the Q2334 device to operate in the External Phase Modulation mode. The desired phase shift will be 90° for this example (see Table 3 on page 16 for other phase settings) and the frequency to be generated is ¼ of the SYS CLK frequency. That is, if the SYS CLK frequency is 30 MHz, the desired output frequency is 7.5 MHz. The following steps should be followed:

1.) It is not necessary to reset the device prior to this step. Setting the operation mode is accomplished by disabling all modes in the "Synchronous Mode Control" (SMC) register, address 08(hex) except EXT PHASE MOD ENABLE (EPME) bit D1. The EPME bit should be set to logic "1". In this case, the value of "02" (hex) should be loaded into this device. This is performed by setting the address bus (ADDRESS0 through ADDRESS4) to "08" and the data bus (DATA0 through DATA7) to "02". Set the Chip Select signal (CS/) to active "0" and pulse the Write Strobe (WR/) low according to the timing requirements shown in figure 11 on page 30. The PMAE bit D5 of the AMC register is set to "0" because the internal phase modulation operation is disabled.

2.) The actual phase increment value (32-bits) is loaded into the Phase Increment Register A (PIRA), addresses "00" through "03" (hex). The least significant byte (LSB) of the 4-byte value is written into address "00" and the most significant byte (MSB) is written into address "03". The write operations are performed using the process described in Step 1. Four such operations are required to load all four byte-wide PIRA register addresses. The desired output frequency is ¼ of the SYS CLK frequency; the 32-bit value to be written to PIRA is "40000000" (hex) using formula (1) shown on page 7. In this case, the registers at address "00", "01", and "02" are written with a data value of "00" while address "03" is written with a data value of "40" (hex).

3.) To effect the 90° phase shift, set PM1 EXT BIT2, PM1 EXT BIT1, PM1 EXT BIT0 to 0 1 0 respectively. (See Table 3 on page 16 for the settings.) These inputs are latched into the DDS by pulsing the signal PM1 CLK high according to the timing specifications in figure 13 on page 32.

Frequency Hopping Mode

The example of frequencies to be hopped between are 1/16, ⅛ and ¼ of the SYS CLK frequency. That is, if the SYS CLK frequency is 30MHz, the desired frequencies are 1.875 MHz, 3.75 MHz, and 7.5 MHz respectively.

It is assumed that the first frequency to be generated will be 1.875 MHz, then 3.75 MHz and last 7.5 MHz. The user can hop between as many different frequencies as they wish however for example purposes we will limit the number to three. The following steps should be followed:

1.) It is not necessary to reset the device prior to this step. Setting the operation mode is accomplished by disabling all modes in the "Synchronous Mode Control" (SMC) register, address 08(hex). In this case, the value of "00" (hex) should be loaded into this device. This is performed by setting the address bus (ADDRESS0 through ADDRESS4) to "08" and the data bus

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6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

(DATA0 through DATA7) to "00". Set the Chip Select signal (CS/) to active "0" and pulse the Write Strobe (WR/) low according to the timing requirements shown in figure 11 on page 30. The PMAE bit D5 of the AMC register is set to "0" because the internal phase modulation operation is disabled.

2.) The actual phase increment value (32-bits) is loaded into the Phase Increment Register A (PIRA), addresses "00" through "03" (hex). The least significant byte (LSB) of the 4-byte value is written into address "00" and the most significant byte (MSB) is written into address "03". The write operations are performed using the process described in Step 1. Four such operations are required to load all four byte-wide PIRA register addresses.
For this example, three frequencies are to be generated in succesion. The first 32-bit value to be written to PIRA is "10000000" (hex) using formula (1) shown on page 7. The second 32-bit value to be written to PIRA is "20000000" (hex) and the third is "40000000".
Note, that in this case the last 24-bits in each three phase increment value are the same. Once the first 32-bit value has been written to the PIRA,all you have to do is change the 8 MSB to generate the three designated frequencies. (The 24 LSB will remain the same until they are re-written and activated by the HOP CLK signal.)
In this case, initially registers at address "00", "01", and "02" are written with a data value of "00" while address "03" is written with a data value of "10" (hex). To hop from 1/16 to 1/8 of the SYS CLK, address "03" is written with a data value of "20" (hex). The same operation is followed to hop between 1/8 and 1/4 of the SYS CLK frequency: address "03" is written with a data value of "40" (hex). If the hopping frequencies did not have any bits in common, then all 32-bits of PIRA would need to be re-written according to the instructions above.

Internal Phase Modulation Mode

When using the Internal Phase Modulation mode, the Q2334 DDS has the capability to shift its output signal in 84 nano-degree increments ($360°/2^{32}$) throughout the complete 360° range. The phase shift can occur as often as the HOP CLK signal can be asserted which is as much as one-tenth of the system clock.

The following procedure will initialize the Q2334 device to operate in the Internal Phase Modulation mode to output a synchronous preset frequency and phase. The intended starting phase offset will be 5° for this example and the frequency to be generated is 19.14 MHz. The following steps should be followed:

1.) It is not necessary to reset the device prior to this step. Setting the operation mode is accomplished by disabling all modes in the "Synchronous Mode Control" (SMC) register, address 08 (hex) except HOP CLK PHASE MOD ENABLE (HPME) bit D3. The HPME bit should be set to logic "1". In this case, the value of "08" (hex) should be loaded into this device. This is performed be setting the address bus (ADDESS0 through ADDRESS4) to "08" and the data bus (DATA0 through DATA7) to "08". Set the Chip Select signal (CS/) to active "0" and pulse the Write Strobe (WR/) low according to the timing requirements shown in figure 11 on page 30.

2.) The actual phase increment values

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

(32-bits) are loaded into their respective Phase Increment Register. For PIRA, use addresses "00" through "03" (hex) and for PIRB use addresses "04" through "07" (hex). The least significant byte (LSB) of the 4-byte value is written into address "00" (PIRA) or "04" (PIRB) and the most significant byte (MSB) is written into address "03" (PIRA) or "07" (PIRB). The write operations are performed using the process described in Step 1. Since the phase increment registers are 32-bits wide, four such operations are required to load all four byte-wide PIRA and PIRB register addresses. For this example, the 32-bit phase increment value to be written to PIRA is "61FEF9A0" (hex) using formula (1) shown on page 7. In this case, the registers at address "00", "01", "02", and "03" are written with a data value of "A0", "F9", "FE", and "61" (hex), respectively. The 32-bit phase increment value to be written to PIRB is "658D3284" (hex) according to the Internal Phase Modulation description under the *Modes of Operation* section on page 22. In this case, the registers at address "04", "05", "06", and "07" are written with a data value of "84", "32", "8D", and "65" (hex), respectively.

3.) The DDS accumulator should be cleared to cause the intended starting phase offset to begin with respect to a zero-phase reference position. This is performed by writing any data value to address "0C" (hex).

4.) The PMAE bit D5 of the AMC register is set to "0" because the internal phase modulation operation will be utilizing all 32 bits of PIRB for the accumulation. If only 8-bit phase resolution is required (i.e., 256-state, 1.41° resolution minimum), then PMAE is set to "1" to utilize only the most significant byte of the PIRB.

DESIGN CONSIDERATIONS WITH THE Q2334

Maintaining low noise and ripple on power supplies and ground is critical for obtaining optimum results with the Q2334, especially as you get closer to the DDS's maximum operating frequency. Make sure to map out the power, ground, and decoupling at the very beginning when starting a new printed circuit board layout. It is possible that power supply switching noise could couple into some of the asynchronous inputs such as WR/, HOP CLK, MUX CLK etc. and cause a false writing of an asynchronous register on the DDS or a false HOP CLK. Such an event can cause the data stream coming out of a single DACBIT to appear erratic or inconsistent. The Data Bus Inputs can also be susceptible in this way. It is therefore desirable to isolate the digital microprocessor bus from other logic circuitry that may be very noisy because it is usually switching all the time. One way to mitigate this digital noise affect is to put high-frequency bypass capacitors, such as 100 pF value, right at the DDS control interface pins in question. Unused DDS input pins can be tied to ground. In this way, maximizing the noise immunity will help in achieving optimum reliability. Additionally, when it comes to the use of decoupling caps, careful attention should be paid to use appropriate values to get the highest degree of RF bypassing of both the power supply switching noise and the Q2334's clock frequency. This is done with a combination of capacitors positioned as close as possible to the V_{DD} terminals of the device, with values ranging down to 0.01 µF for up to 30 MHz clock rates and 0.001 µF for clock rates up to 50 MHz.

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

TECHNICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 5 shows the absolute maximum ratings of the Q2334 devices. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

		Q2334I-20N		Q2334C-50N		Q2334M-30L			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
Storage Temperature	T_S	-55	+85	-55	+85	-65	+150	°C	
Operating Temperature	T_A	-40	+85	0	+70	-55	+125	°C	
Junction Temperature	T_J		+150		+150		+150	°C	1
Voltage on any Input Pin		-0.3	V_{DD} + 0.3	-0.3	V_{DD} + 0.3	-0.3	V_{DD} + 0.3	V	
Voltage on V_{DD} & any Output Pin		-0.3	+7.0	-0.3	+7.0	-0.3	+7.0	V	
DC Input Current	I_{IN}	-10	+10	-10	+10	-10	+10	µA	

Note:

1. For thermal management consideration, the Junction to Case Thermal Resistance, Θ_{JC}, given for the 68-pin PLCC package only, is 10.7°C/W typical.

DC Electrical Characteristics

Table 6 shows the DC electrical characteristics for the Q2334 devices.

Table 6. DC Electrical Characteristics

		Q2334I-20N Q2334M-30L		Q2334C-50N			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	4.5	5.5	4.75	5.25	V	
High-level Input Voltage	V_{IH}	2.0	V_{DD} + 0.3	2.0	V_{DD} + 0.3	V	
Low-level Input Voltage	V_{IL}	-0.3	0.8	-0.3	0.8	V	
Input Leakage Current	I_L		1.0		1.0	µA	
High-level Output Voltage	V_{OH}	2.4		2.4		V	1
Low-level Output Voltage	V_{OL}		0.4		0.4	V	2
Output Short Circuit Current	I_{OS}	100	300	100	300	mA	3
Output Capacitance	C_{OUT}		10		10	pF	
Power Dissipation @ maximum SYS CLK	P_D		.267 @ 20MHz		0.67 @50 MHz	W	4

Notes:

1. I_{OH} = - 1.6 mA.
2. I_{OL} = 1.6 mA.
3. Not more than one output shortened at a time (for less than 1 second).
4. Clocking the DDS at the maximum clock frequency, and only one DDS is operating. If both sides are active the power will be doubled. For other clock frequencies, Power = (13.33 mW/MHz)(Clock Frequency); Current = (2.66 mA/MHz)(Clock Frequency).

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E-mail: vlsi-products@qualcomm.com
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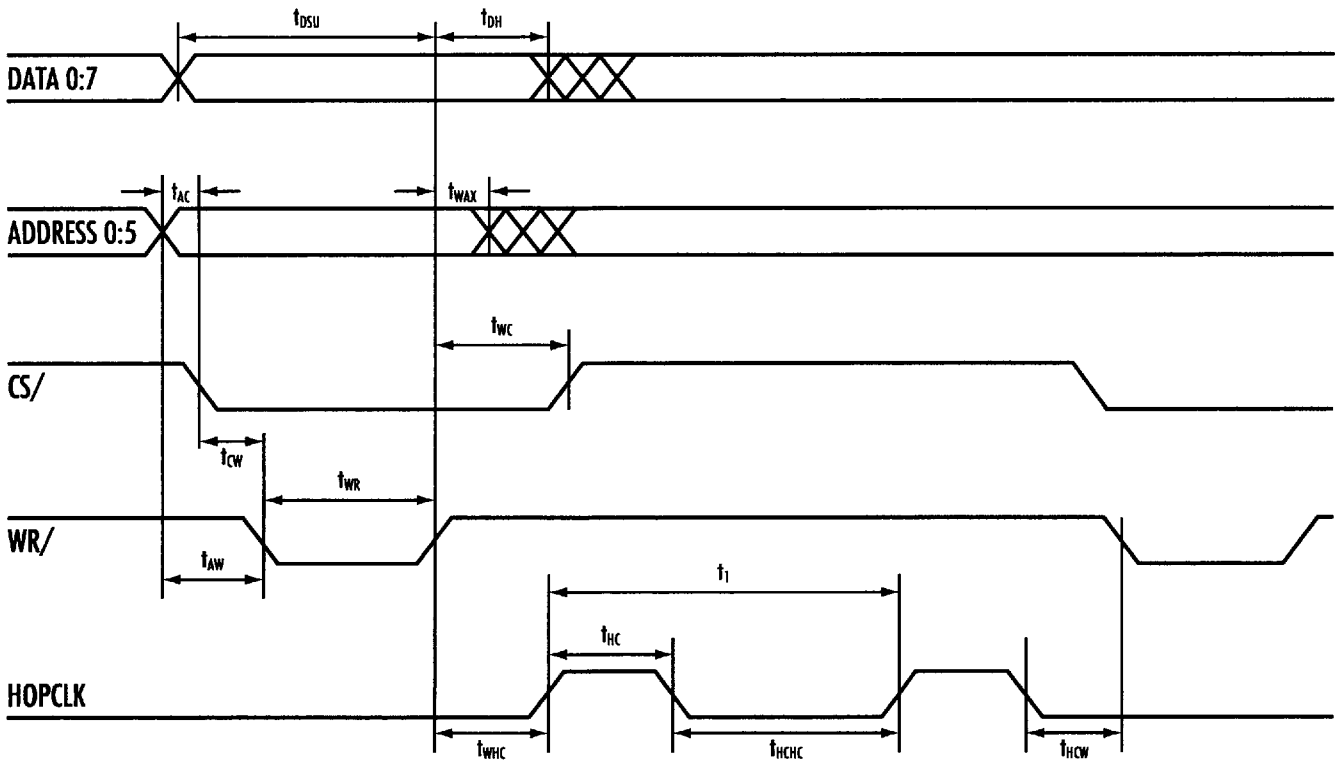
Timing Specifications

Figures 11 through 14 show the timing specifications of the Q2334 devices

Figure 11. Processor Interface Timing



PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Data Setup to WR/ rising	t_{DSU}	10	—	ns	
Data hold after WR/ rising	t_{DH}	5	—	ns	
Address valid to CS/ falling	t_{AC}	0	—	ns	
Address hold after WR/ rising	t_{WAX}	5	—	ns	
CS/ setup to WR/ falling	t_{CW}	0	—	ns	
CS/ hold after WR/ rising	t_{WC}	0	—	ns	
WR/ rising to HOP CLK rising	t_{WHC}	10	—	ns	1
HOP CLK pulse width	t_{HC}	t_{CYC}	—	ns	2
HOP CLK falling edge to HOP CLK rising edge	t_{HCHC}	$4 * t_{CYC}$	—	ns	2
HOP CLK falling edge to WR/	t_{HCW}	$10 * t_{CYC}$	—	ns	1
Address valid to WR/ falling	t_{AW}	15	—	ns	
WR/ period	t_{WR}	40	—	ns	
Time between HOP CLK	t_I	$10 * t_{CYC}$	—	ns	2

Notes:

1. When CS/ is active low.
2. t_{CYC} is the system clock period.
3. Processor interface timing is identical for all versions of the Q2334.

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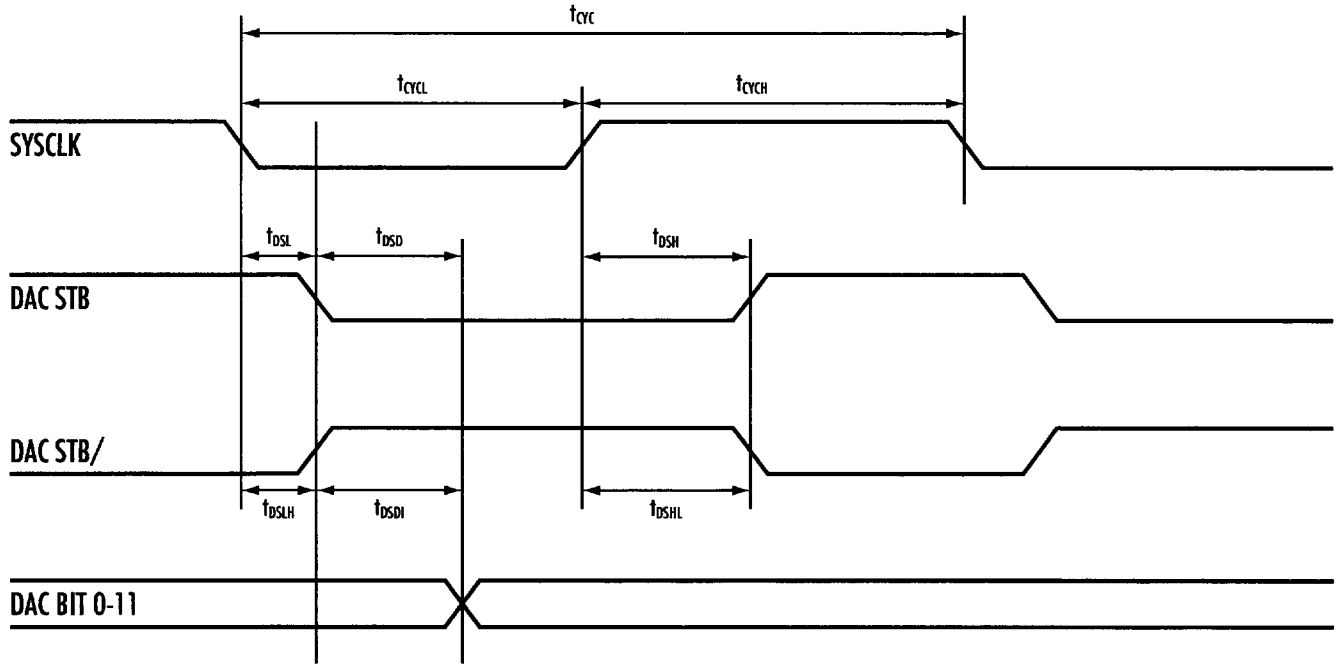
Figure 12. DAC Output Timing



PARAMETER	SYMBOL	Q2334I-20N (20MHz max clock) MIN	Q2334I-20N (20MHz max clock) MAX	Q2334C-50N Q2334M-30L (30MHz max clock) MIN	Q2334C-50N Q2334M-30L (30MHz max clock) MAX	Q2334C-50N (40MHz max clock) MIN	Q2334C-50N (40MHz max clock) MAX	Q2334C-50N (50MHz max clock) MIN	Q2334C-50N (50MHz max clock) MAX	UNITS	NOTES
SYS CLK cycle period	t_{CYC}	50	500	33	500	25	500	20	500	ns	1, 2, 3
SYS CLK low period	t_{CYCL}	22	478	15	485	11.25	488.75	8.5	491.5	ns	
SYS CLK high period	t_{CYCH}	22	478	15	485	11.25	488.75	8.5	491.5	ns	
SYS CLK low to DAC STB low	t_{DSL}	–	10	–	10	–	10	–	10	ns	4
SYS CLK low to DAC STB/ high	t_{DSLH}	–	10	–	10	–	10	–	10	ns	4
SYS CLK high to DAC STB high	t_{DSH}	–	10	–	10	–	10	–	10	ns	4
SYS CLK high to DAC STB/ low	t_{DSHL}	–	10	–	10	–	10	–	10	ns	4
DAC STB low to DAC BIT output	t_{DSD}	4	20	4	17	4	17.5	4	14	ns	4
DAC STB/ high to DAC BIT output	t_{DSDI}	4	20	4	17	4	17.5	4	14	ns	4

Notes:

1. The Q2334C-50N will operate up to 30 MHz maximum clock with $-55 \le T \le 125°C$ and $4.5 \le V_{DD} \le 5.5$ V.
2. The Q2334C-50N will operate up to 40 MHz maximum clock with $-40 \le T \le 85°C$ and $4.5 \le V_{DD} \le 5.5$ V.
3. The Q2334 contains dynamic Logic. Minimum SYS CLK frequency is 2.0 MHz.
4. Assumes a 25pF capacitive loading.

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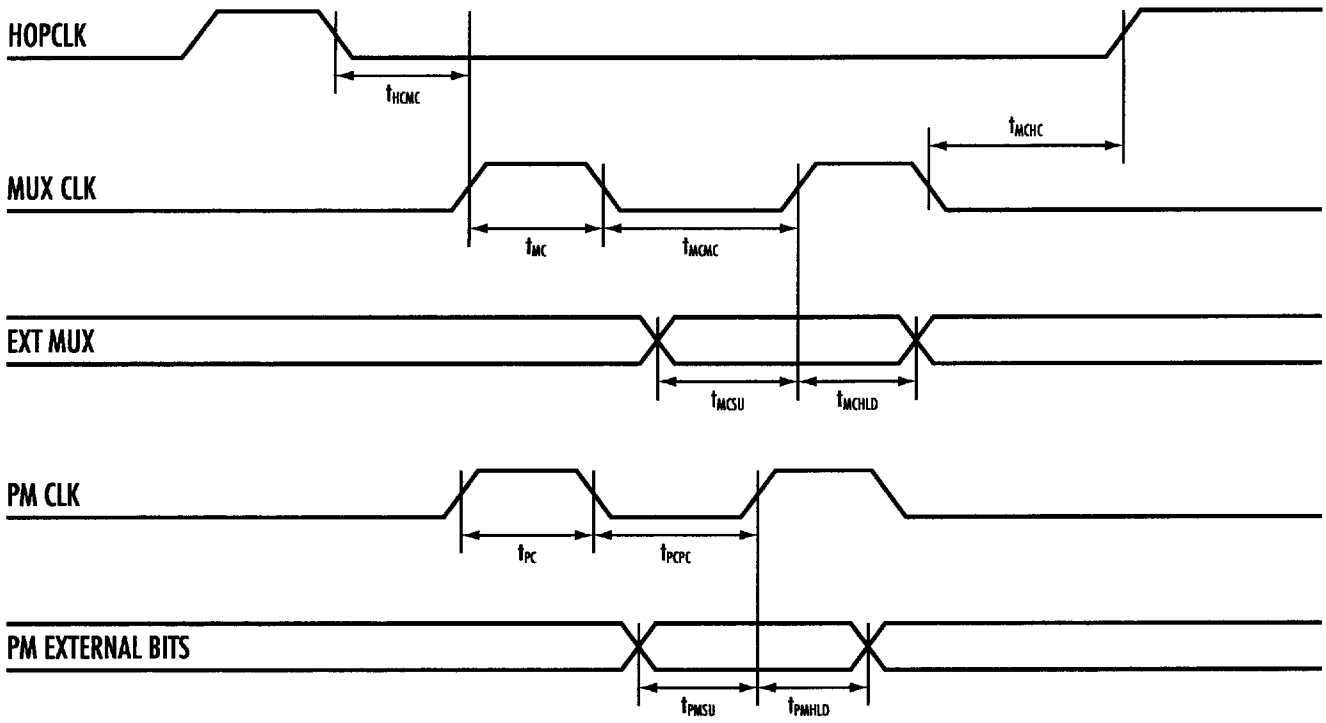
Figure 13. External Control Timing



PARAMETER	SYMBOL	MIN	MIN	MAX	UNITS
HOP CLK falling to MUX CLK rising	t_{HCMC}	t_{CYC}	—	—	ns
MUX CLK high period	t_{MC}	$3 * t_{CYC}$	—	—	ns
MUX CLK low period	t_{MCMC}	t_{CYC}	—	—	ns
MUX CLK falling to HOP CLK rising	t_{MCHC}	$10 * t_{CYC}$	—	—	ns
EXT MUX setup to MUX CLK	t_{MCSU}	10	15	—	ns
EXT MUX hold after MUX CLK	t_{MCHLD}	10	15	—	ns
PM CLK high period	t_{PC}	$3 * t_{CYC}$	—	—	ns
PM CLK low period	t_{PCPC}	t_{CYC}	—	—	ns
PM data setup to PM CLK	t_{PMSU}	10	15	—	ns
PM data hold after PM CLK	t_{PMHLD}	10	15	—	ns

Notes:

1. External control timing is identical for all versions of the Q2334.
2. t_{CYC} is the system clock period.

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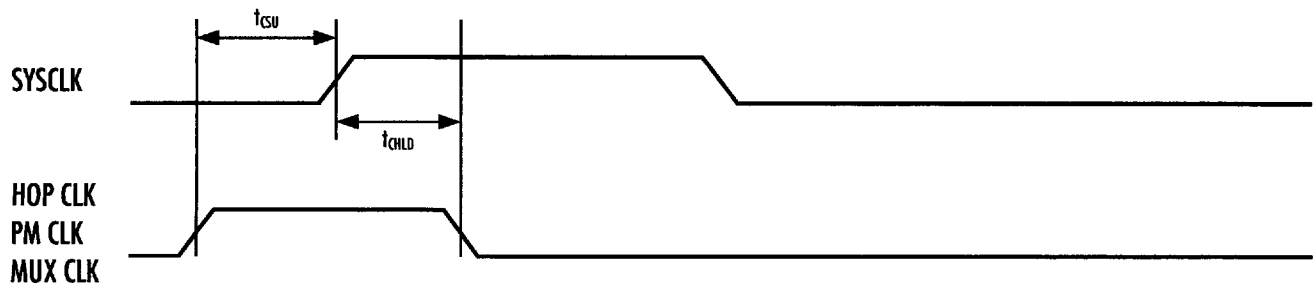
Figure 14. Synchronous Specifications for Asynchronous Inputs



PARAMETER	SYMBOL	MIN	MAX	UNITS
Asynchronous rising to SYS CLK rising	t_{CSU}	5	—	ns
Asynchronous falling to SYS CLK rising	t_{CHLD}	8	—	ns

Note:

Synchronous specifications for asynchronous inputs are identical for all versions of the Q2334.

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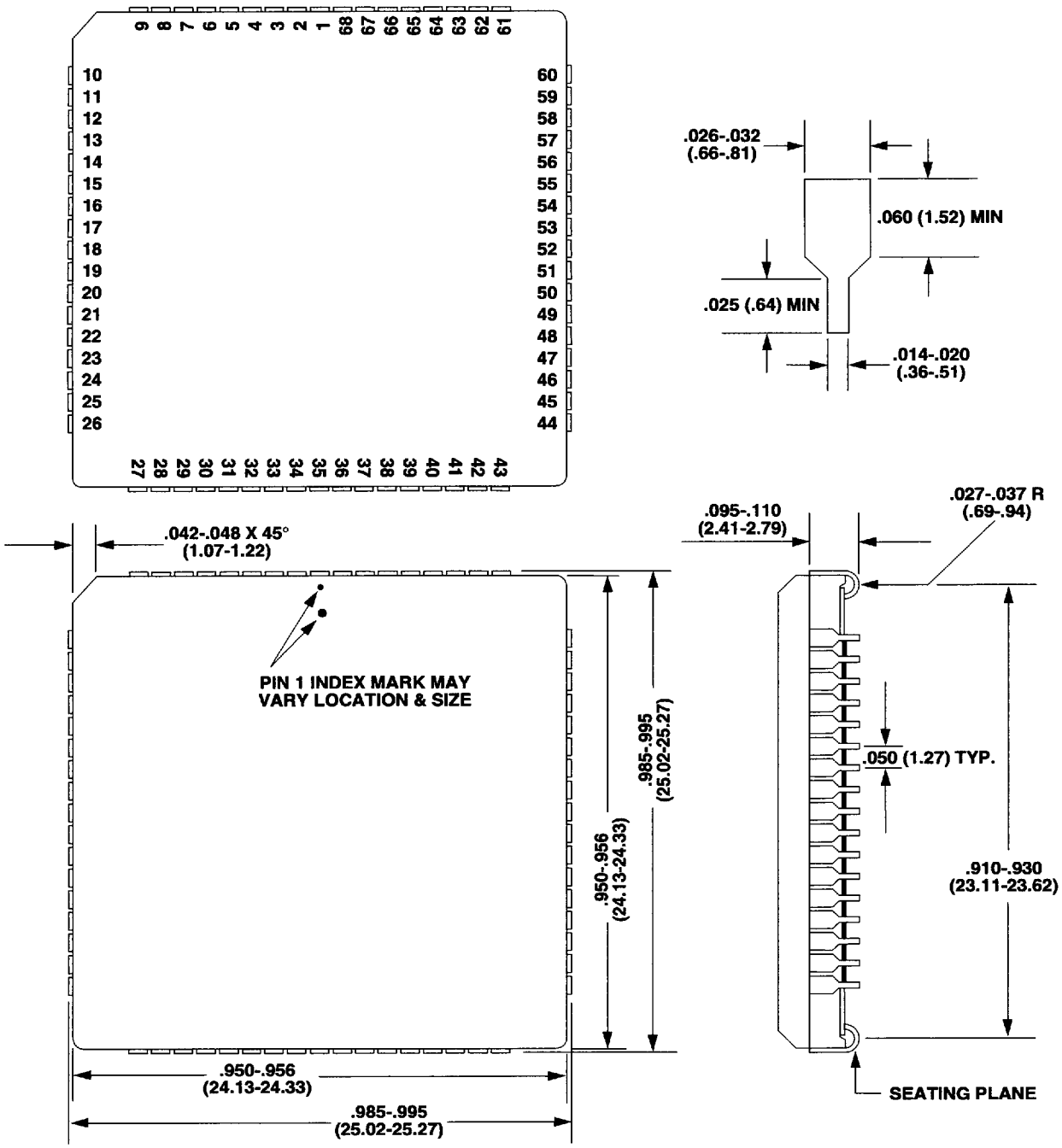
PLCC PACKAGING
(Q2334I-20N, Q2334C-50N)

The Q2334I-20N and the Q2334C-50N are packaged in the 68-pin plastic leaded chip carrier (PLCC) shown in figure 15. The dimensions are given in inches and (mm).

Figure 15. PLCC Packaging



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6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

CLDCC PACKAGING
(Q2334M-30L)

The Q2334M-30L is packaged in the 68-pin ceramic leaded chip carrier (CLDCC) shown in figure 16. The dimensions are given in inches and (mm).

Figure 16. CLDCC Packaging

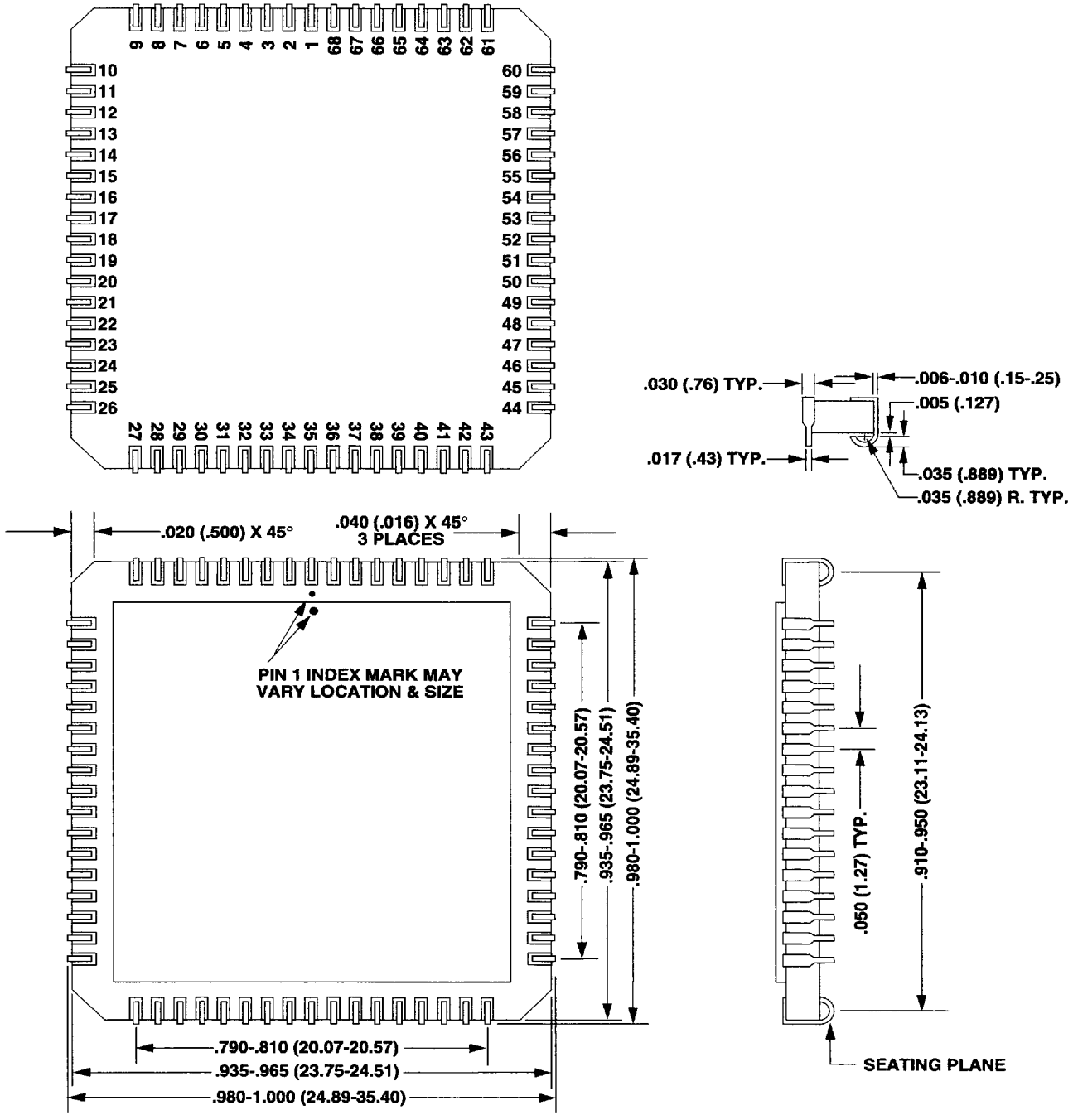

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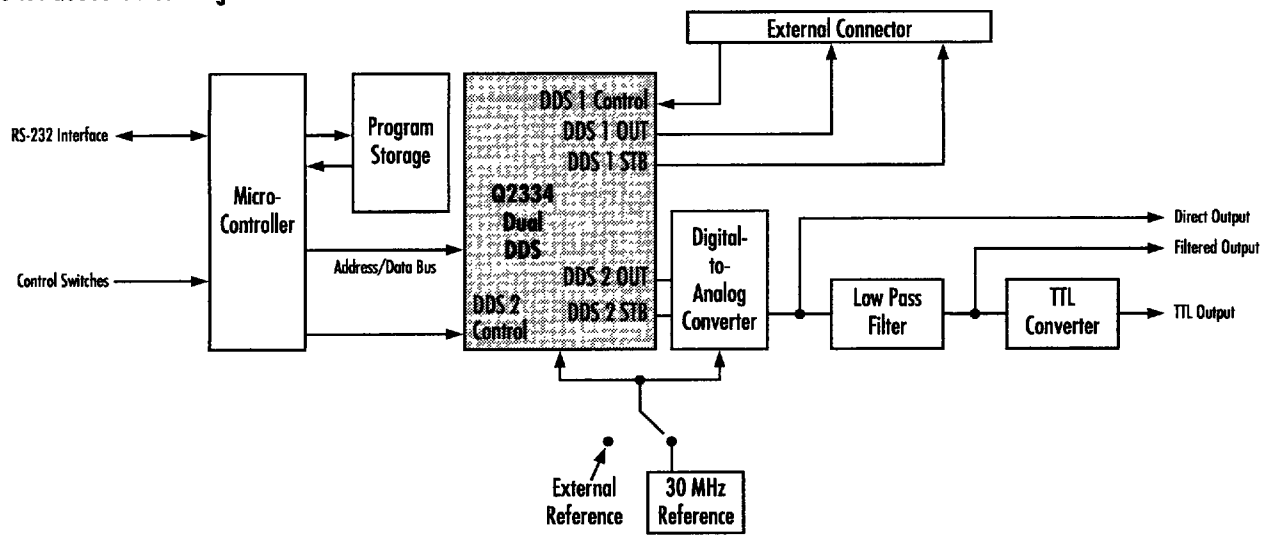
Figure 17. Q0310-1 Block Diagram



Q0310-1 DDS EVALUATION BOARD

The Q0310-1 is an evaluation board for the Q2334 DDS. The Q0310-1 is a complete DDS System that includes a Q2334I-30N, Pre-programmed microcontroller, 10-bit DAC, and Low Pass Filter all designed onto an 8" x 4" x 1.5" printed circuit card that is fully assembled and tested. An 8031 microcontroller controls the DDS device using a monitor program contained in the on-board EPROM. This program interacts through the switches on the board for stand-alone operation or through the RS-232 port for remote mode. A block diagram of this particular configuration is shown in figure 17. The menu-driven monitor program can exercise all of the following modes of operation:

- Basic Oscillator
- Frequency Sweep (Fast or Slow)
- Frequency Hop
- 8-PSK Modulator
- 256-PSK Modulator
- MSK Modulator

A Q0310-1 User's Guide with complete documentation including schematics, parts list, and microcontroller code (available in floppy disk) is included.

RECOMMENDED SOCKETS

For PLCC Package Type:

Methode Electronics 213-052-602 Low Profile Surface Mount 68-pin carrier socket; AMP 821574-1 thru-hole 68-pin carrier socket.

For CLDCC Package Type:

AMP 641749-2 thru-hole 68-pin carrier socket, or AMP 641345-2 surface mount 68-pin carrier socket.

RECOMMENDED DACS

Since the DAC is generally the limiting factor for spurious performance, DDS manufacturers are able to do two things: (1) guarantee the noise (spur) levels of the digitized sine wave or (2) offer applications assistance and predict the noise level of the analog sine wave. The latter can be difficult to do for DDS manufacturers since the DDS can be used with any DAC and thus, predicted performance only becomes meaningful if the DDS manufacturer has direct experience in empirically qualifying a particular type DAC with a given DDS. After extensive testing, it is our recommendation in applications using

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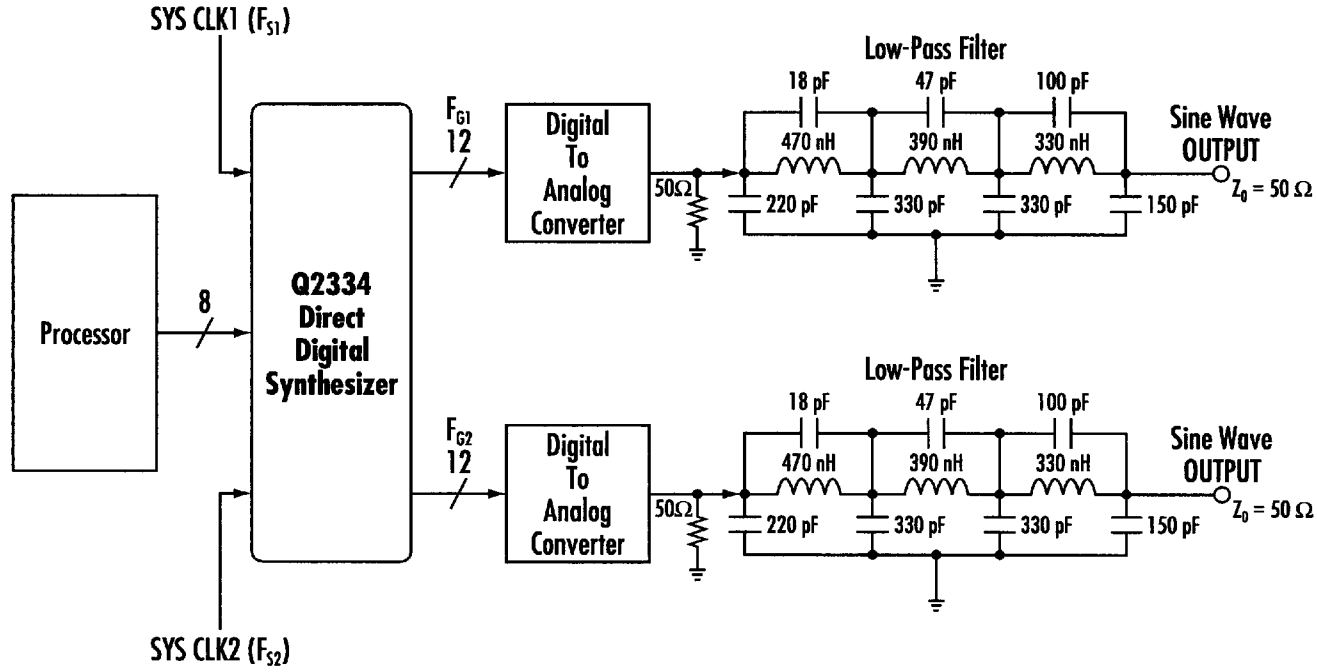
Clock rates below 20 Msps and output frequencies below 5 MHz, that the best Spurious-Free-Dynamic-Range performance can be achieved with 12-bit resolution DACs; these may not necessarily be suited for higher frequency AC performance, however, since DAC non-linearities are the dominant effect at low frequencies, these kinds of applications will benefit from the higher-bit resolution. In applications where faster Clock rates or higher output frequencies are applied, the best SFDR performance will be achieved with DACs having ultra low switching transients (glitch energy) and very fast settling time, although the practical tradeoff for total integrated noise performance generally means using a DAC of at least 10-bits of resolution. Different DACs may be appropriate for a specific system but it seems the only real way to compare DACs and validate performance is to build test circuits using them.

Figure 18. Q2334 DDS System



APPLICATION EXAMPLES AND FREQUENTLY ASKED QUESTIONS

DDS System Diagram

Figure 18 provides a basic diagram of a Q2334 DDS system. Note the LPF used is a seven pole elliptical filter designed for operation with a 50 MHz clocked DDS, which rolls off at approximately 20 MHz. This is the filter topology used in the Q0310-1 Evaluation Board. Each system has different specifications, and the design of the LPF should take the system requirements into account.

Quadrature Signal Generation with the Q2334

Quadrature (sine and cosine) outputs are generated by setting each DDS to the same frequency, but 90° apart in phase.

Implementation:

1.) You must tie the clocks together, thus allowing no drift between the 2 DDSs

2.) Using the external phase modulation mode, you can easily set the two DDSs to be exactly 90° apart by setting the 3 bits to 0 1 0. Two possible methods are shown in figure 19 a and b.

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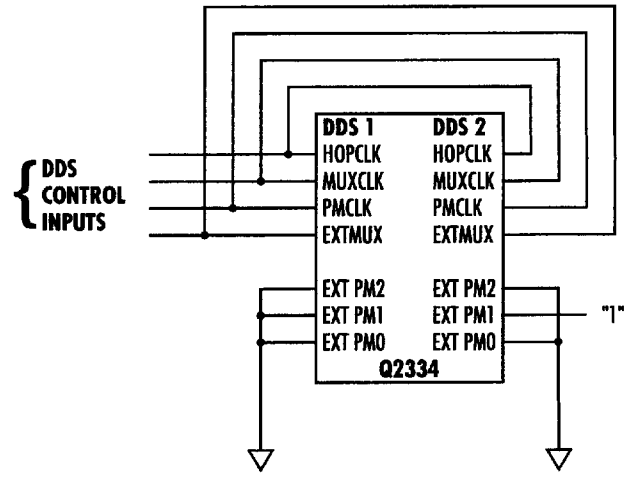
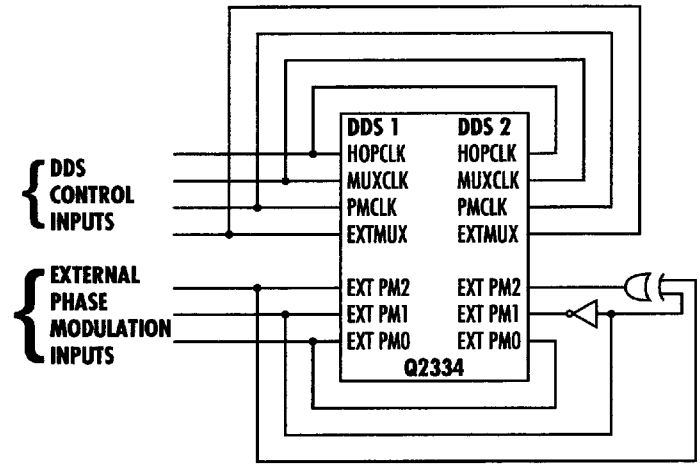
Figure 19. Quadrature Signal Implementation



a.) Quadrature Oscillator Using Q2334 DDS



b.) Phase Modulated Quadrature Oscillator Using Q2334 DDS

As per figure 19a, all external control lines for both DDS functions (HOP CLK, MUX CLK, PM CLK, and EXT MUX) are tied together and the external PM inputs of one DDS are set to 90°. As per figure 19b, two external logic gates permit the use of the external PM control bits if phase modulation of the quadrature outputs is also required. In this case, the DDS2 output waveform will always be 90° advanced in phase with respect to DDS1.

DDS-generated quadrature signals have the advantage of precise phase and amplitude balance over the entire DDS bandwidth since it does not rely on analog components with their associated frequency response, tolerances, and aging effects. Using the "Internal Phase Modulation" mode, the Q2334 can produce outputs which differ in phase from 90° with a minimum resolution of $360°/2^{32}$. Since a microprocessor-controlled system can store open-loop compensation data vs. frequency, phase compensation can be made as an adjustment during equipment calibration. Alternatively, a closed-loop system can

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Figure 20. Translated DDS with Improved Phase Noise and Spurious

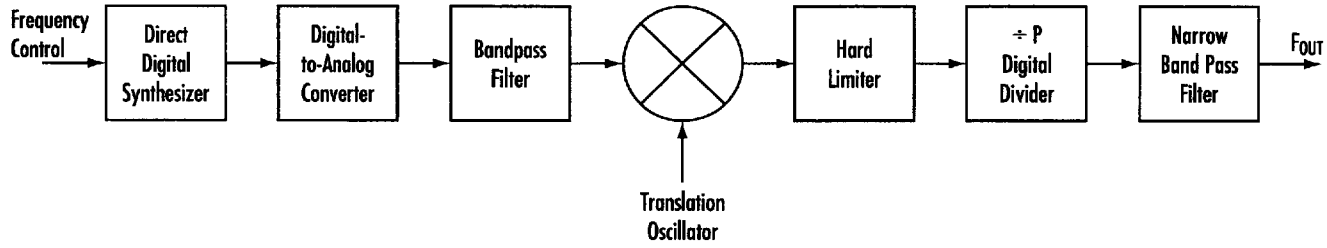
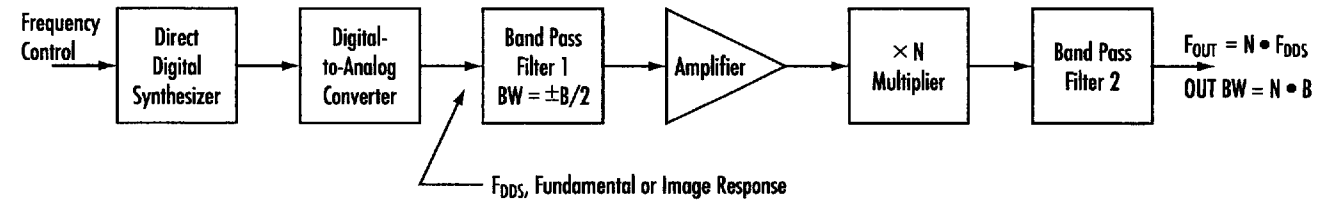


Figure 21. Multiplied DDS for Higher Frequency and Greater Output Bandwidth



be constructed, given a suitable detector, which will allow feedback control of fine resolution offsets from quadrature for compensation of phase errors elsewhere in the system.

Divided/Multiplied/Translated DDS

Fundamental or Image

One of the limitations surrounding DDS for L.O. generation is the fact that the fundamental frequency that can be achieved is restricted to ≈ 40% of the clock frequency capability. This limitation can frequently be sidestepped by taking advantage of the image responses that are automatically generated as a byproduct of the sampling techniques that occur within the DDS architecture. The images will occur at multiples of the clock frequency ± the generated fundamental output frequency, as shown in Figure 4. In other words,

DDS Image Responses = $N \bullet F_{CLK} \pm F_{OUT}$
where N = 0,1,2,3...

There are certain things to note when trying to utilize DDS image responses. First, whether we're referring to a fundamental output or an imaged output, the DAC's nonlinearities or "glitches" may contribute harmonics of the fundamental output which may fold into the desired passband. Secondly, the Sin(x)/x amplitude envelope impressed upon all DDS fundamental and image outputs, will inherently create lower amplitude image signals compared to the fundamental. This results in a lower spurious-free-dynamic-range for the image output but can be improved by using a DAC with excellent linearity and perhaps D/A de-glitching techniques. It's important to note, however, that the actual phase noise performance at the image response will be the same as that of the fundamental output frequency. The kinds of applications best-suited for utilizing an image signal involve generating a narrowband L.O. or I.F. frequency using the first or second image response. If there are any output tuning requirements, they should be constrained to a very narrowband range so as to allow

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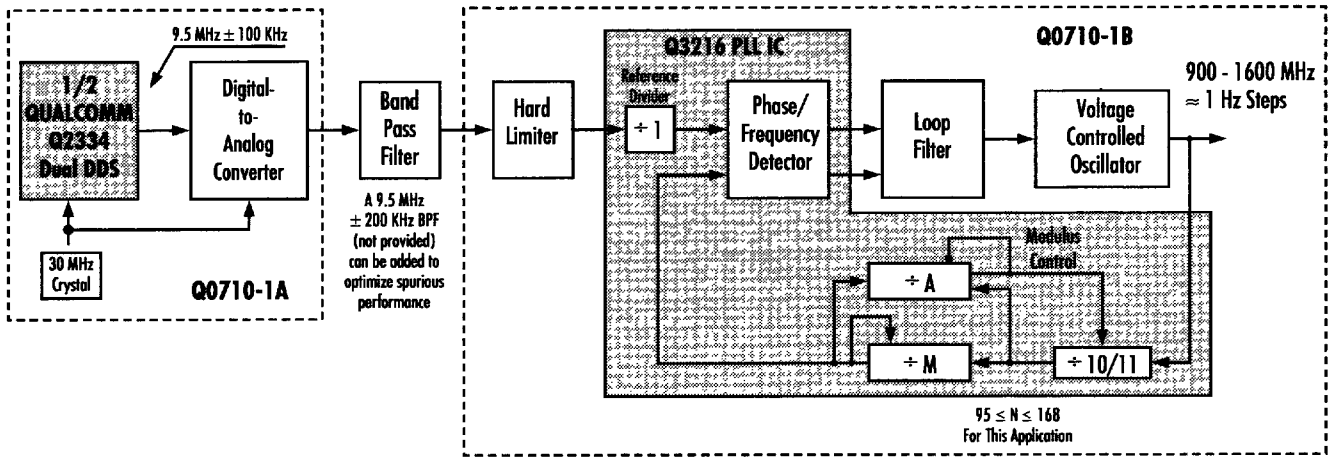
for the use of a very selective bandpass filter to attenuate all unwanted spurious outputs.

Various "tricks" can be applied to any fundamental or image response to both maximize spectral purity, and achieve a higher range of final output frequencies. One such method is to upconvert the output of the DDS/DAC and then cascade with a digital divider to get the desired frequency, as shown in Figure 20. The limiter will suppress any AM spurs, and the divider can be used to divide the DDS output to provide an appropriate center frequency for a particular filter technology (such as a crystal filter, where the range of center frequencies may be limited), or simply to improve its phase noise and spurious performance (20 LOG[P] dB improvement, ideally). Another such method to achieve both a higher frequency and a widened tuning bandwidth is to cascade the output of the DDS/DAC with a multiplier and associated filtering, as shown in Figure 21. The first bandpass filter keeps the DDS-generated spurious tones and noise confined to the filter bandwidth of ± B/2. After frequency multiplication by N, the noise and spurious tones will be degraded by 20 LOG[N] dB, but only within ± B/2 of the output frequency. That is to say, the output spectrum is a clean tone surrounded by a pedestal of noise and spurs. The pedestal width is equal to B, with noise and spurs falling off rapidly beyond this point. The final output frequency is $F_{OUT} = N \bullet F_{DDS}$, and the output tuning bandwidth is N • B. In essence, bandpass filter 1 serves as a tuneable high-frequency tracking filter, but is actually a fixed, low-frequency design. The amplifier provides sufficient drive level into the passive multiplier, and bandpass filter 2 pre-selects the desired harmonic and suppresses other harmonic spurious. Any AM spurious components from the DDS are no larger at the output of a multiplier than at the input, so these can be suppressed by a limiter before or after frequency multiplication, if desired.

Figure 22. Q0710-1 DDS-Driven PLL Block Diagram



DDS-Driven Phase Locked Loop (PLL)

The combination of DDS and PLL frequency synthesis can make a powerful hybrid synthesizer. For example, the use of a PLL synthesizer driven by a Direct Digital Synthesizer (such as the QUALCOMM Q0710-1 DDS-Driven PLL Frequency Synthesizer) can produce a synthesizer which operates between 900 and 1600 MHz. This hybrid synthesizer

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has a frequency resolution of ≈1 Hz (it varies between 0.63 Hz and 1.2 Hz across the band). The DDS output frequency is 9.5 MHz, and the "N" in the PLL varies between 95 and 168. A block diagram of the Q0710-1 DDS-Driven PLL Frequency Synthesizer is shown in figure 22.

This approach combines the high frequency, low noise features of a PLL design with the fine frequency resolution and rapid switching times of the DDS (reference QUALCOMM Application Note #AN2334-4, Hybrid PLL/DDS Frequency Synthesizers).

Common Questions about the Q2334 DDS

1.) Question: What should I expect at power up?
Answer: The Q2334 powers up in a random state. To put the Q2334 in a known state, set the ARR to clear everything in the phase accumulator, HOP Clock. Then set all your frequencies and modulation modes and Hop Clock.

2.) Question: How long does it take for my input to the DDS to produce the effected output?
Answer: It takes 31 clock cycles for the DDS to process the new input and generate a new output.

3.) Question: What is the frequency stability of the Q2334?
Answer: The output frequency of the Q2334 has a stability which is directly proportional to the stability of the Clock Reference used. For instance, for a DDS operating at a set clock frequency, the frequency accuracy of the clock is propagated through the DDS. Therefore, if the sampling frequency is 100 PPM higher than desired, the DDS output frequency will be higher by 100 PPM. This doesn't change the frequency resolution but it does affect the overall frequency accuracy.

4.) Question: What is the maximum rate of change of frequency possible under microprocessor control with the Q2334?
Answer: Assuming you can write data at the maximum rate, this comes out to a 2 MHz frequency change rate for the Q2334C-50N.

5a.) Question: How do I use the Asynchronous Hop Clock?
Answer: You just write anything to that port.

5.b) Question: What's the difference between the Hop Clock and the Asynchronous Hop Clock?
Answer: There is no difference between the functions that they perform. They can be thought of as exactly the same thing, however, their implementation does differ. The Hop Clock is an external control line which is applied to the HOP CLK input pin and the Asynchronous Hop Clock is processsor controlled via software.

6.) Question: I'm seeing spurs larger than 60dBc on my prototype board. I thought I was guaranteed better than -60dBc spurs?
Answer: We can only guarantee the performance from the DDS. The -60dBc spurs you are seeing are coming from the DAC or possibly layout related. We can only tell you what is typically expected when using these DACs.

7.) Question: Can you use the rising edge of DACSTB to clock the DACBIT data into the DAC?
Answer: It is inadvisable. The DACSTB must be synchronized with respect to the falling edge of SYS CLK or set-up and hold time

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requirements for the DAC may be violated, causing DAC errors. If you must use a rising edge triggered DACSTB, then set the D7 address of the Asynchronous Mode Control register to a "1" in order to generate a DACSTB/ which maintains compliance with respect to the SYS CLK falling edge.

8.) Question: Can I use the most significant bit (MSB) of the digitized sine wave outputs as a programmable clock source directly?

Answer: Yes, as long as the associated jitter component of the MSB is acceptable for your clock source requirements. The worst case jitter that the MSB will have for any given output frequency is $1/(2F_S)$. A DAC will basically interpolate this out which is why it is not a factor when this is used. It is also recommended that the Noise Reduction Circuit (NRC) be disabled when the MSB output is used directly so as to not include any undesirable frequency dithering components from this circuit.

9.) Question: Can I use my PC with the Q0310 Evaluation Board?

Answer: Yes, all you need is to use a dumb terminal emulation package. There are many available, such as Kermit or Vterm.

GLOSSARY

AHC	Asynchronous Hop Clock
AMC	Asynchronous Mode Control
ARR	Accumulator Reset Register
BFSK	Binary Frequency Shift Keying
CLDCC	Ceramic Leaded Chip Carrier
CS	Chip Select
DAC	Digital to Analog Converter
DDS	Direct Digital Synthesizer
EME	External Multiplexer Enable
EPME	External Phase Modulation Enable
EXT MUX	External Multiplexer
F_G	Generated Frequency
F_S	System Clock Frequency
HOP CLK	Hop Clock
HPME	Hop Clock Phase Modulation Enable
LSB	Least Significant Bit
MSB	Most Significant Bit
MSK	Minimum Shift Keying
MUX CLK	Multiplexer Clock
LPF	Low Pass Filter
NRC	Noise Reduction Circuit
PIR	Phase Increment Register
PLCC	Plastic Leaded Chip Carrier
PMAE	Phase Modulation Add Enable
PSK	Phase Shift Keying
SMC	Synchronous Mode Control
SNR	Signal to Noise Ratio

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RELATED QUALCOMM LITERATURE

AN2334-1 "Complex Waveform Generation Using Direct Digital Synthesizer Techniques"

AN2334-3 "Direct Digital Synthesis, 21 Questions & Answers for RF Engineers"

AN2334-4 "Hybrid PLL/DDS Frequency Synthesizers"

"PLL, DDS, VCO Synthesizer Boards" Technical Data Sheet"

PATENT REFERENCES

1.) U.S. Patent No. 4,905,177 - "High Resolution Phase to Sine Amplitude Conversion," QUALCOMM, Feb. 27, 1990.

2.) U.S. Patent No. 4,901,265 - "Pseudorandom Dither for Frequency Synthesis Noise," QUALCOMM, Feb. 13, 1990.

3.) U.S. Patent No. 4,965,533 - "Direct Digital Synthesizer Drive Phase Lock Loop Frequency Synthesizer," QUALCOMM, Oct. 23, 1990.

ORDERING INFORMATION

Table 7. Q2334 Ordering Information

PART NUMBER	MAXIMUM CLOCK SPEED	PACKAGE	TEMPERATURE RANGE	V_{DD} INPUT	NOTES
Q2334I-20N	20 MHz	68-Pin PLCC	−40°C to +85°C	4.5 V to 5.5 V	
Q2334M-30L	30 MHz	68-Pin CLDCC	−55°C to +125°C	4.5 V to 5.5 V	1
Q2334C-50N	50 MHz	68-Pin PLCC	0°C to +70°C	4.75 V to 5.25 V	2, 3
Q0310-1	Evaluation Board for the Q2334 Dual Direct Digital Synthesizer				4

Notes:

1. For more information, reference the "Q2334M-30L Military Version Description" section on Page 6 of this data sheet.
2. The Q2334C-50N will operate up to 30 MHz maximum clock with $-55 \le T \le 125°C$ and $4.5 \le V_{DD} \le 5.5$ V. Reference the "DAC Output Timing" specifications on Page 31 of this data sheet.
3. The Q2334C-50N will operate up to 40 MHz maximum clock with $-40 \le T \le 85°C$ and $4.5 \le V_{DD} \le 5.5$ V. Reference the "DAC Output Timing" specifications on Page 31 of this data sheet.
4. For more information, reference the "Q0310-1 DDS Evaluation Board" section on Page 36 of this data sheet, and the "PLL, DDS, VCO Synthesizer Boards" Technical Data Sheet.

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E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556