SIEMENS

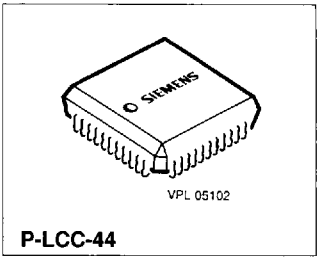
ISDN D-Channel Exchange Controller (IDEC®)

PEB 2075

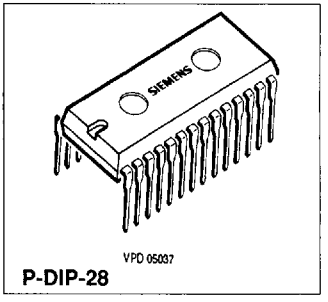
CMOS IC

1 Features

- Four independent HDLC channels
- 64-byte FIFO storage per channel and direction
- Handling of basic HDLC functions
  flag detection/generation
  zero deletion/insertion
  CRC checking/generation
  check for abort
- Address recognition
- C/I channel handler
- Single connection and quad connection modes
- IOM® interface or PCM interface
- Programmable time slots and channel data rates (up to 4 Mbit/s)
- Different methods of contention resolution
- Standard P- interface, multiplexed or non-multiplexed address and data buses
- Vectored interrupt
- Advanced CMOS technology
- Power consumption less than 50 mW during operation.



P-LCC-44



P-DIP-28

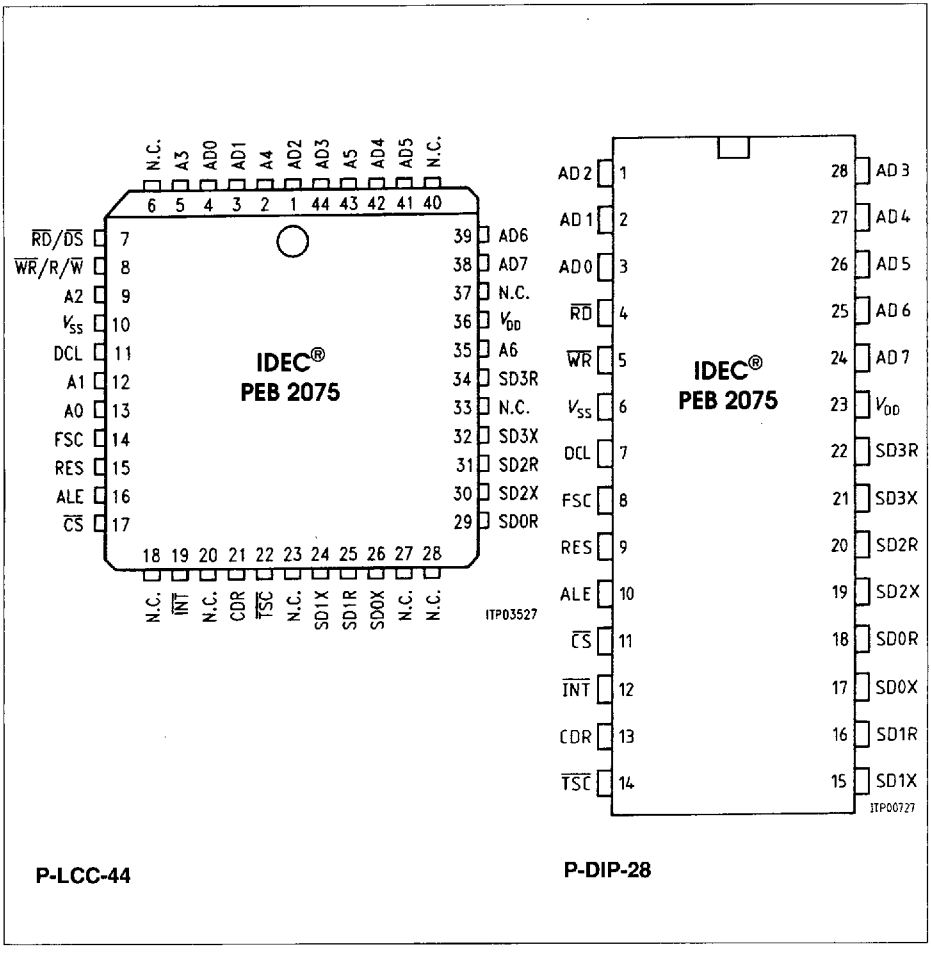
Type	Version	Ordering Code	Package
PEB 2075-N	V.1.3	Q67100-H6189	P-LCC-44 (SMD)
PEB 2075-P	V.1.3	Q67100-H6188	P-DIP-28

The ISDN Digital Exchange Controller PEB 2075 (IDEC) is a serial HDLC data communication circuit with four independent channels. Its telecommunication specific features make it especially suited for use in variable data rate PCM systems. In addition, the device contains sophisticated switching functions and it implements automatic contention resolution between packet data from different sources.

Its applications include: communication multiplexers, peripheral ISDN line cards, packet handlers and X.25 packet switching devices. The IDEC is a fundamental building block for networks with either centralized, de-centralized or mixed signaling/packet data handling architectures.

1.1 Pin Configuration

(top view)



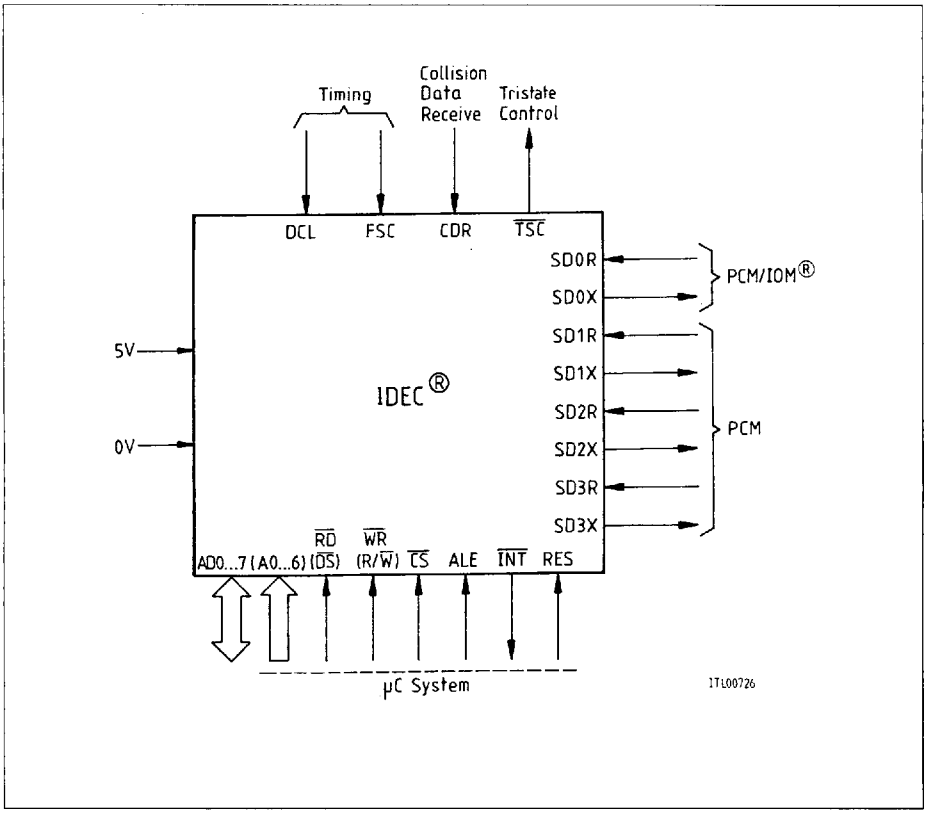
P-LCC-44 **P-DIP-28**

1.2 Pin Definitions and Functions

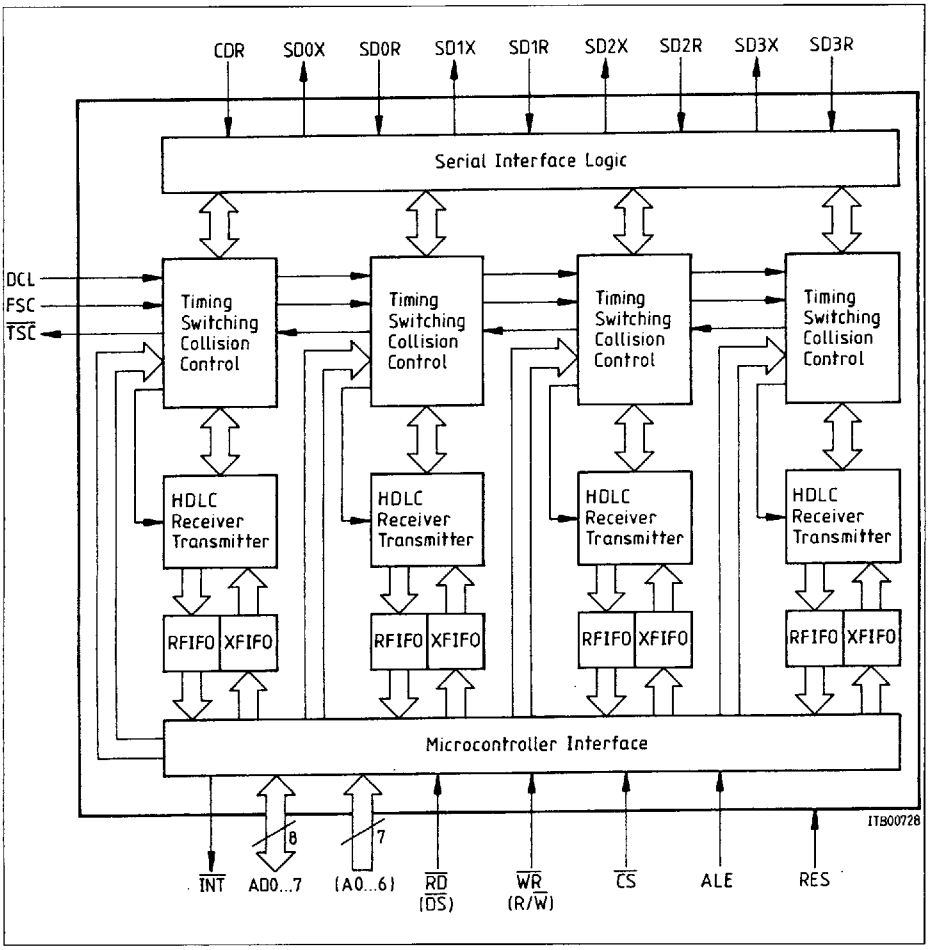
Pin No. P-LCC-44	Pin No. P-DIP-28	Symbol	Input (I) Output (O) Open Drain (OD)	Function
4 3 1 44 42 41 39 38	3 2 1 28 27 26 25 24	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I / O	**Address Data Bus.** If the multiplexed address/data µP interface bus mode is selected these lines transfer data and commands between the µP and the IDEC. If a demultiplexed mode is used, these lines interface with the system data bus.
13 12 9 5 2 43 35	- - - - - - -	A0 A1 A2 A3 A4 A5 A6	I	**Address Bus.** These inputs interface to the system´s address bus to select an internal register for a read or write access. Only provided in the P-LCC package and only active if a demultiplexed µP interface is selected.
17	11	$\overline{CS}$	I	**Chip Select.** A low on this line selects the IDEC for a read/write operation.
8	5	$\overline{WR}$	I	**Write.** This signal indicates a write operation, active low (Siemens/Intel bus mode).
8	-	R/$\overline{W}$	I	**Read/Write.** At "high", identifies a valid µP access as a read operation. At "low", identifies a µP access as a write operation (Motorola bus mode). Only provided in the P-LCC package.
7	4	$\overline{RD}$	I	**Read.** This signal indicates a read operation, active low (Siemens/Intel bus mode).
7	-	$\overline{DS}$	I	**Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode). Only provided in the P-LCC package.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC-44	Pin No. P-DIP-28	Symbol	Input (I) Output (O) Open Drain (OD)	Function
16	10	ALE	I	**Address Latch Enable.** In the Siemens/ Intel type multiplexed µP interface mode a "high" on this line indicates an address of an internal register on the external address/data bus. In the Siemens/Intel type demultiplexed µP interface mode this line should be connected to V_{SS}, in the demultiplexed Motorola type µP interface mode it should be connected to V_{DD}.
19	12	$\overline{INT}$	OD	**Interrupt Request.** This signal is activated when the IDEC requests an interrupt.
15	9	RES	I	**Reset.** A "high" on this interrupt brings the IDEC into the reset state.
29 25 31 34	18 16 20 22	SD0R SD1R SD2R SD3R	I	Serial data receive.
26 24 30 32	17 15 19 21	SD0X SD1X SD2X SD3X	O	Serial data transmit. Serial data transmit. Serial data transmit. Serial data transmit. Serial data transmit. Collision output. Serial data transmit. -
11	7	DCL	I	**Data Clock;** supplies a clock signal either equal to or twice the data rate.
14	8	FSC	I	Frame synchronization or data strobe signal.
22	14	$\overline{TSC}$	O	**Time-Slot Control.** Supplies a control signal for an external driver.
21	13	CDR	I	Collision data receive.
10	6	V_{SS}	I	Ground.
36	23	V_{DD}	I	Positive power supply.



Logic Symbol



Block Diagram

1.3 System Integration

Communication Multiplexers

The four independent serial HDLC communication channels implemented in the IDEC make the circuit suitable for use in communication multiplexers.

The collision detection/resolution capability of the circuit allows statistical multiplexing of packets in one or several physical data communication channels, for example in DMI (mode 3) applications.

Centralized Signaling / Data Packet Handlers

The IDEC can be used in central packet handlers of ISDN networks to process signaling or packet data of four ISDN subscribers. In this application, it may be used with or without the Extended PCM Interface Controller (EPIC®) PEB 2055.

The IDEC can be connected to the IOM interface of the EPIC, which is itself connected to the PCM system highway. The EPIC implements concentration and time slot assignment functions. As an alternative, the IDEC may be directly connected to PCM highways (**figure 1**).

The size (from 1 to 8 bits) and the position of the time slot associated with each HDLC controller is software programmable. In addition to the receive and transmit data highways, the IDEC accepts a third input connection for collision detection purposes. The mode of collision detection is programmable. A "collision highway" (or time slot) can be used for remote collision control, as a "clear to send" lead, or for local contention resolution among several IDECs.

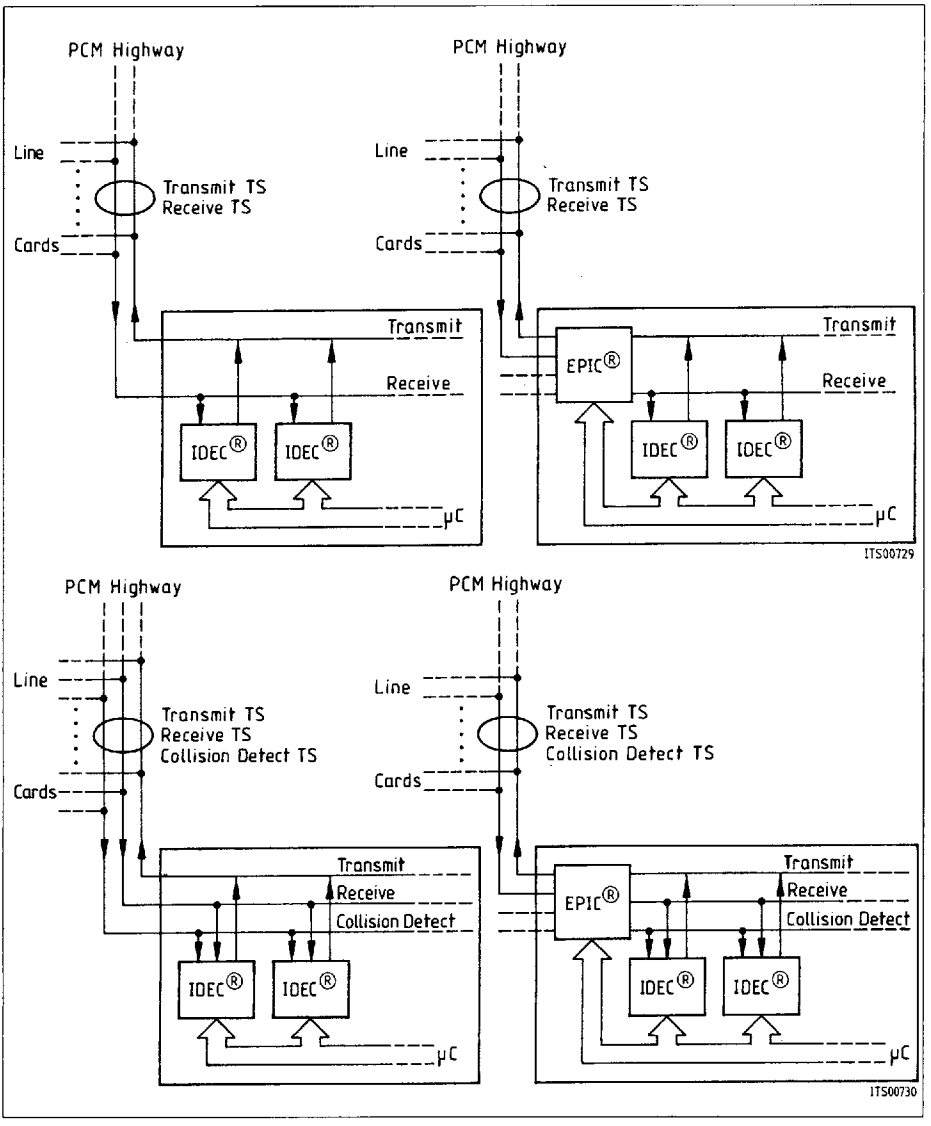


Figure 1
Use of IDEC® in Central Signaling / Data Packet Handlers

Line Cards in De-Centralized or Mixed Signaling / Data Packet Handling Architectures

The IDEC can be used on peripheral line cards to process D-channel packets for ISDN subscribers. The PCM Controller PEB 2055 has the layer-1 controlling capacity and a B-channel switching capacity for a total of 32 subscribers. The B and D channels and the control information for eight subscribers are carried by one IOM interface. Thus a line card dimensioned for 32-ISDN subscribers may employ up to eight IDECs, two for each IOM connection (**figure 2**). A High Level Serial Communication Controller (HSCX) SAB 82525 with two HDLC channels, or another IDEC may be used to transmit and receive signaling via the system highway in a common channel. Again, such a common channel may be shared among several line cards, due to the statistical multiplexing capability of these controllers.

In completely de-centralized D-channel processing architectures, the processing capacity of a line card is usually dimensioned so as to avoid blocking situations even under maximum conceivable D-channel traffic conditions. It may sometimes be more advantageous to perform p-packet handling in a centralized manner while keeping s-packet handling on the line cards. A statistical increase in p-packet traffic has then no effect on the line card, and can be easily dealt with by one of the modular architectures for a central packet handler shown in the previous section. A more effective sharing of the total p-packet handling capacity is the result, especially in a situation where p-packet traffic patterns vary widely from one subscriber group to another.

The use of an IDEC in the mixed D-channel processing architecture is illustrated in **figure 3**.

The additional "transparent data" connections supported by the IDEC enable a merging of p and s packets into one D channel. Possible collision situations are dealt with by the IDEC which uses either the additional collision detect line (**figure 3**) or a time slot on the system highway (**figure 3**) from the line card to the central packet handler.

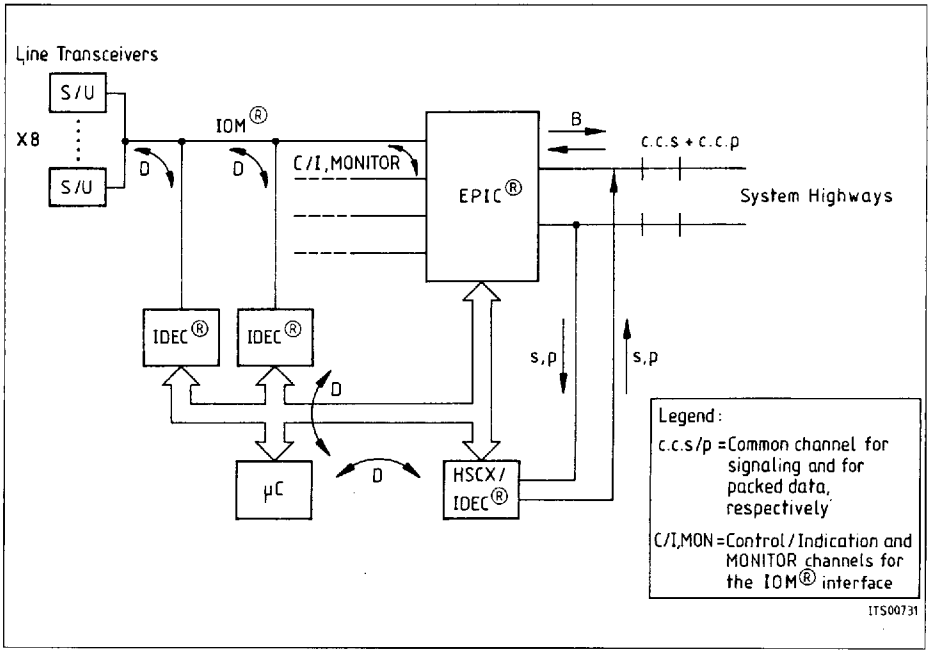


Figure 2
Line Card in a De-Centralized D-Channel Handling Architecture

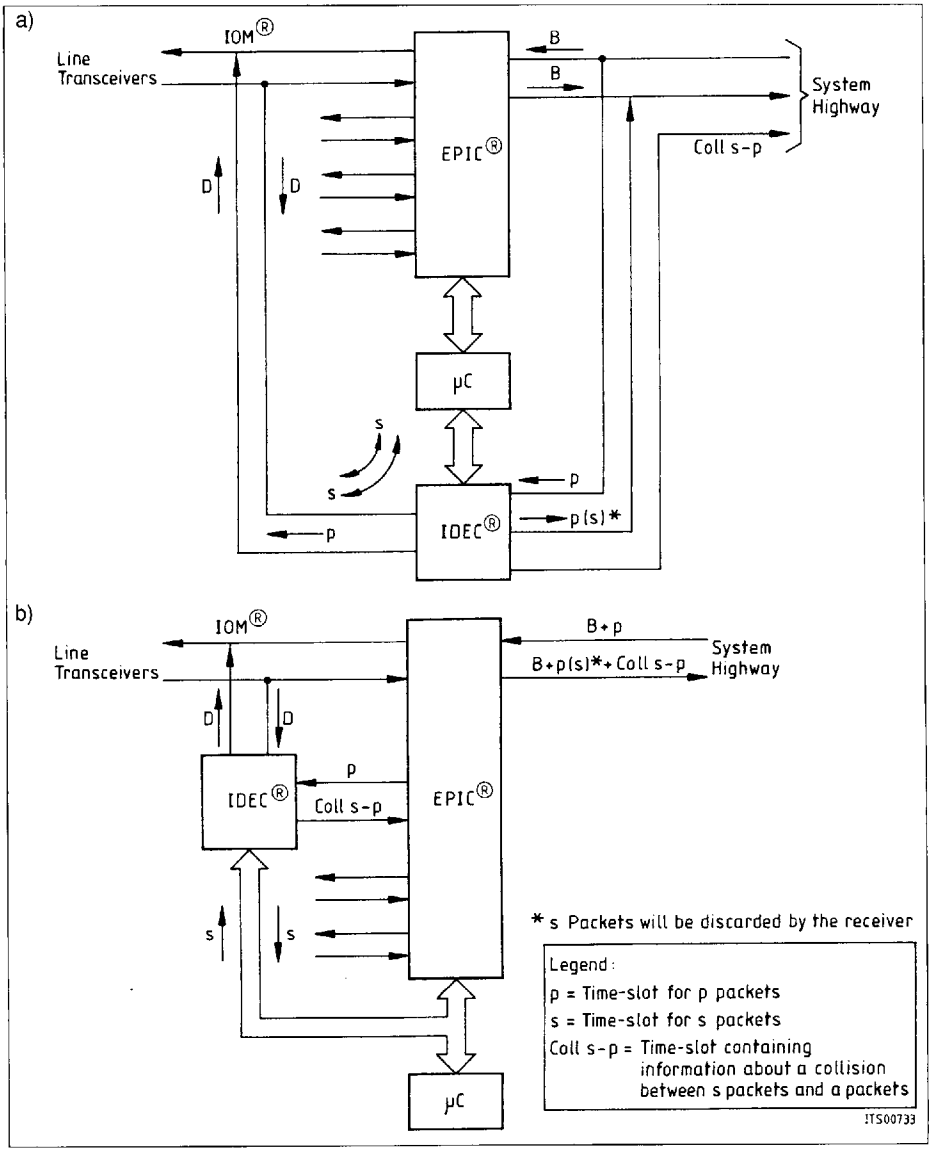


Figure 3
IDEC® on a Line Card in a Mixed D-Channel Processing Architecture

2 Functional Description

2.1 General Functions and Device Architecture

The IDEC is an HDLC controller which handles four HDLC communication channels, each channel fully independent and programmable by its own register set. The circuit performs the following functions:

- Extraction (reception) and insertion (transmission) of the HDLC data packets in a time division multiplex bit stream.
- Implementation of the basic HDLC functions of the layer-2 protocol, including address recognition.
- Interfacing of the data packets to the microprocessor bus. For the temporary storage of data packets internal FIFOs are used.
- Switching of data between serial interfaces.
- Implementation of different types of collision resolution.
- Test functions.

2.2 Operating Modes

Each HDLC controller of the IDEC is assigned to one time channel determined either by time slot assignment or by an external strobe signal.

Two basic configurations are distinguished (**figure 4**):

- In the quad connection configuration the four HDLC controllers (A - D) are connected to individual time multiplexed communication lines;
- In the single connection configuration the four HDLC channels are all connected to one time multiplexed communication line.

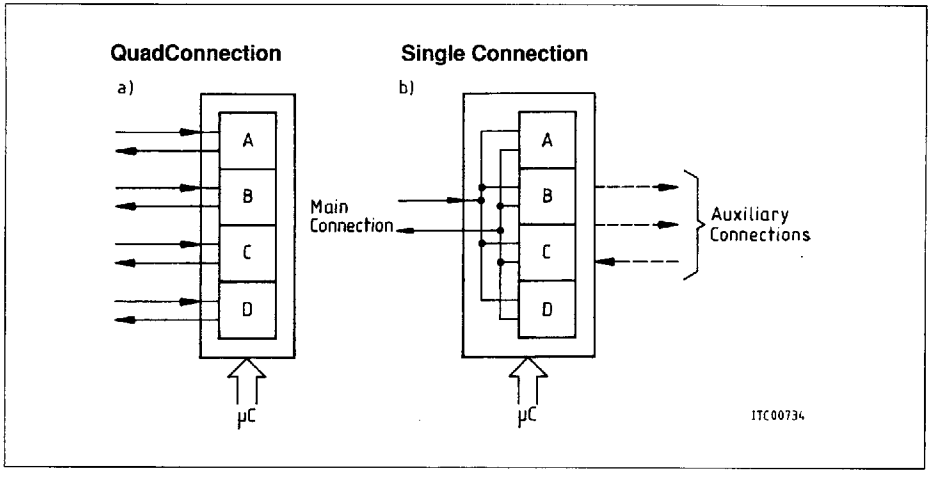


Figure 4

In the quad connection configuration two modes are distinguished as follows:

- Each connection is a time slotted highway, the lengths and positions of the time slots are programmable (quad connection time slot mode);
- Each connection is a communication line, the time channels are marked by an external strobe signal (quad connection common control mode).

Two modes are distinguished in turn for the single connection configuration as follows:

- The connection is a standard IOM interface with predefined channel positions (single connection IOM mode);
- The connection is a time slotted highway (single connection time slot mode).

For simplicity, a time slotted highway will usually be referred to as a "PCM highway", or PCM for short.

Table 1
Four Basic Operation Modes of the IDEC

MDS1	MDS0	Mode Description
0	0	Single connection time slot mode
0	1	Quad connection common control mode
1	0	Single connection IOM mode
1	1	Quad connection time slot mode

To program the single connection IOM mode (CCR:MDS1, MDS0 = 10)
with the slave mode (MODE3-0:CMS1, CMS0 = 01) or
with the multi master mode (MODE3-0:CMS1, CMS0 = 10) or
with the uncond. trans. mode (MODE3-0:CMS1, CMS0 = 00)

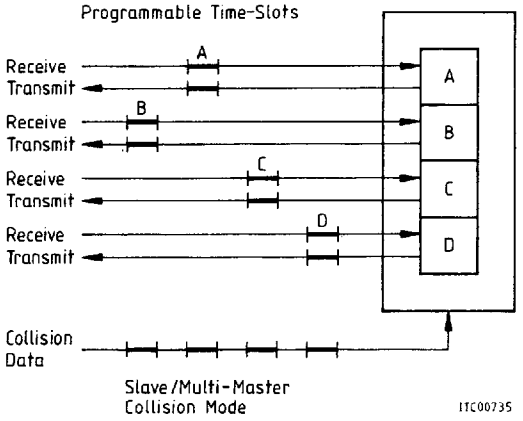
this additional programming has to be made:

MODE0:CCS1, CCS0 = 00 bin
MODE1:CCS1, CCS0 = 00 bin
MODE2:CCS1, CCS0 = 00 bin
MODE3:CCS1, CCS0 = 00 bin

TSR0 = 0C hex
TSR1 = 1C hex
TSR2 = 2C hex
TSR3 = 3C hex

The four modes of operation are illustrated in **figure 5.** Via channel-by-channel programming, one of a number of collision detection modes may be selected in each of the basic modes of operation. For future reference, they are also depicted in **figure 5.**

a) Quad Connection TS Mode



b) Quad Connection Common Control Mode

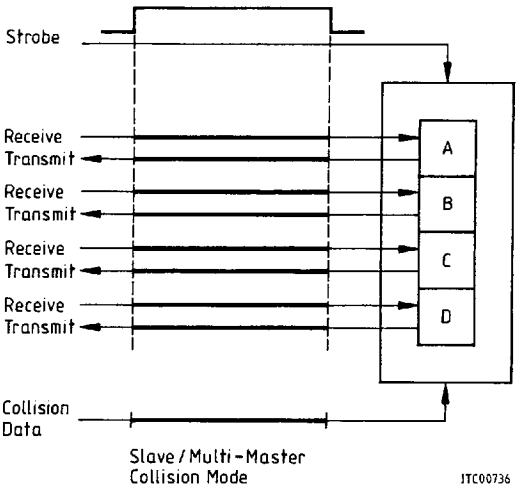
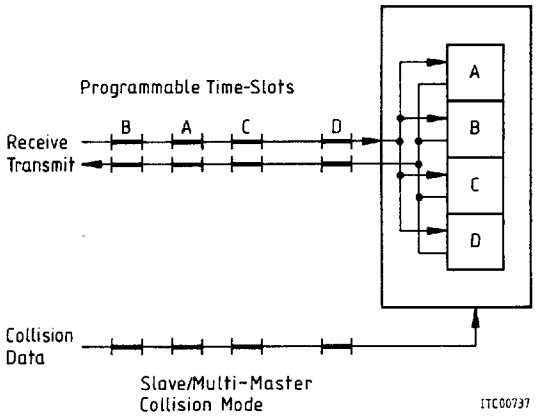


Figure 5a, 5b
Operating Modes of the IDEC

c) Single Connection TS Mode



d) Single Connection IOM® Mode

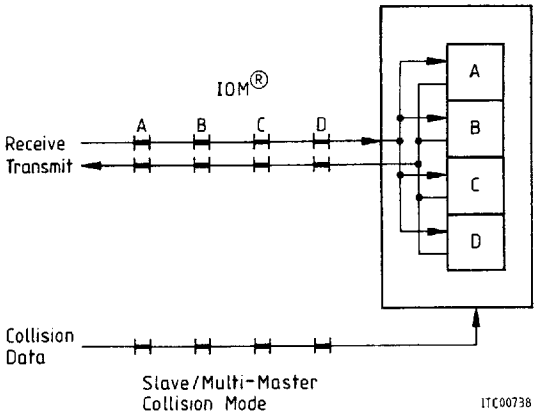


Figure 5c, 5c
Operating Modes of the IDEC

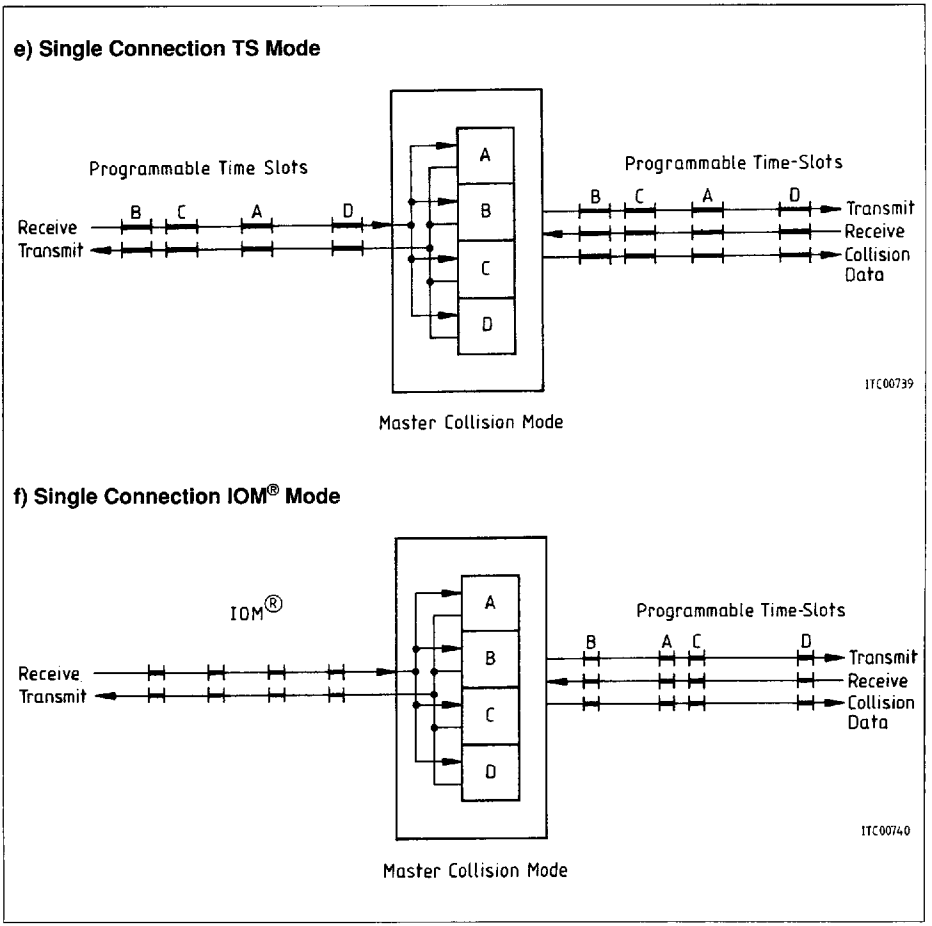


Figure 5e, 5f
Operating Modes of the IDEC

2.3 Interfaces

Microcontroller Interface

The IDEC is programmable over an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 (19) lines and is directly compatible with processors of the multiplexed and demultiplexed address/ data bus types (Siemens/Intel or Motorola processor families). The microprocessor interface signals are summarized in **table 2**.

Table 2
Microcontroller Interface Signals of the IDEC

Symbol	Input (I) Output (O) Open Drain (OD)	Function
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O	**Address Data Bus.** If the multiplexed address/data µP interface bus mode is selected these lines transfer data and commands between the µP and the IDEC. If a demultiplexed mode is used, these lines interface with the system data bus.
A0 ... A6	I	**Address Bus.** These inputs interface to the system´s address bus to select an internal register for a read or write access. Only provided in the P-LCC package and only active if a demultiplexed µP interface is selected.
$\overline{CS}$	I	**Chip Select.** A low on this line selects the IDEC for a read/write operation.
$\overline{WR}$ R/$\overline{W}$	I	**Write.** This signal indicates a write operation, active low (Siemens/Intel bus mode). **Read/Write.** At "high", identifies a valid µP access as a read operation. At "low", identifies a µP access as a write operation (Motorola bus mode). Only provided in the P-LCC package.
$\overline{RD}$ $\overline{DS}$	I	**Read.** This signal indicates a read operation, active low (Siemens/Intel bus mode). **Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode). Only provided in the P-LCC package.

Table 2 (cont'd)
Microcontroller Interface Signals of the IDEC

Symbol	Input (I) Output (O) Open Drain (OD)	Function
ALE	I	**Address Latch Enable.** In the Siemens/Intel type multiplexed µP interface mode a "high" on this line indicates an address of an internal register on the external address/data bus. In the Siemens/Intel type demultiplexed µP interface mode this line should be connected to V_{SS}. In the demultiplexed Motorola type µP interface mode it should be connected to V_{DD}.
$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the IDEC requests an interrupt.
RES	I	**Reset.** A "high" on this input brings the IDEC into the reset state.

In addition to 8-bit processors, the IDEC supports a direct connection to 16-bit processors. Thus, through an internal address transformation, it is possible to access all IDEC registers using either even microprocessor addresses only or odd microprocessor addresses only.

Serial Interfaces

Depending on the selected mode, the IDEC supports four physically separate, full duplex serial interfaces, or one full duplex serial interface.

In addition to the data input and data output lines, the serial interface requires a common data clock (input DCL) and a frame synchronization signal (input FSC). Input data is latched on the falling edge of DCL and output data is clocked off on the rising edge of DCL. The IDEC may be programmed so that the data clock rate is either equal to the data rate, or twice the data rate.

2.4 Individual Functions

2.4.1 Channel Access

The four HDLC controllers of the IDEC are connected to the serial interfaces as shown in **table 3.** The table indicates the selection of the data channel, the selectable time slot widths, the output driver type, and the function of the active-low Tri-State Control ($\overline{TSC}$) output in each of the operating modes.

The data output is set in a high impedance state outside the time channel where data is transmitted.

OD = Open-drain driver,
PP = Push-pull driver.
The output driver type refers to the SD0X (or SD0X, SD1 X, SD2X and SD3X) outputs.
$\overline{TSC}$ is a push-pull signal.

Quad Connection Time-Slot Mode

Channel selection is performed via the Time-Slot Select Registers (TSR). For each HDLC channel, the 8- bit TSR register gives the position of a time slot with a two-bit resolution. The length of the time slot, either 1, 2, 7 or 8 bits, can be selected using the MODE register (CCS1, 0). These parameters are common to the receive and the transmit channel.

In the case where the number of bits in a PCM frame is 256 or 512, the frame synchronization signal FSC need not be provided at every PCM frame beginning, since bit counters are automatically reset at frame end. When the PCM frame length is not equal to either 256 or 512 bits, the frame synchronization signal has to be provided at the beginning of every PCM frame.

Table 3
HDLC Controller Channel Selection and Characteristics

Mode		Channel Input				Channel Output				Description
MDS1	MDS0	A	B	C	D	A	B	C	D	
0	0	SD0R	SD0R	SD0R	SD0R	SD0X	SD0X	SD0X	SD0X	Single connection TS mode
0	1	SD0R	SD1R	SD2R	SD3R	SD0X	SD1X	SD2X	SD3X	Quad connection common control mode
1	0	SD0R	SD0R	SD0R	SD0R	SD0X	SD0X	SD0X	SD0X	Single connection IOM mode
1	1	SD0R	SD1R	SD2R	SD3R	SD0X	SD1X	SD2X	SD3X	Quad connection TS mode

Mode		Channel Characteristics		Tri-State Control ($\overline{TSC}$) Signal	Output Driver
MDS1	MDS0	Channel Select	Channel Width	Defined by	
0	0	TSR A-D registers	1, 2, 7, 8	TSR A-D	PP or OD
0	1	FSC strobe	Arbitrary	FSC inverted	PP or OD
1	0	Fixed two-bit TS´s	2	Fixed two-bit TS´s A-D	OD
1	1	TSR A-D registers	1, 2, 7, 8	TSR B	PP or OD

OD = Open-drain driver,
PP = Push-pull driver.
The output driver type refers to the SD0X (or SD0X, SD1X, SD2X and SD3X) outputs.
$\overline{TSC}$ is a push-pull signal.

The tristate control output line $\overline{TSC}$ marks the time slot when data is transmitted/received by the HDLC controller B.

The position of a time slot with respect to FSC, as a function of the TSR register contents, is shown in **figure 6**.

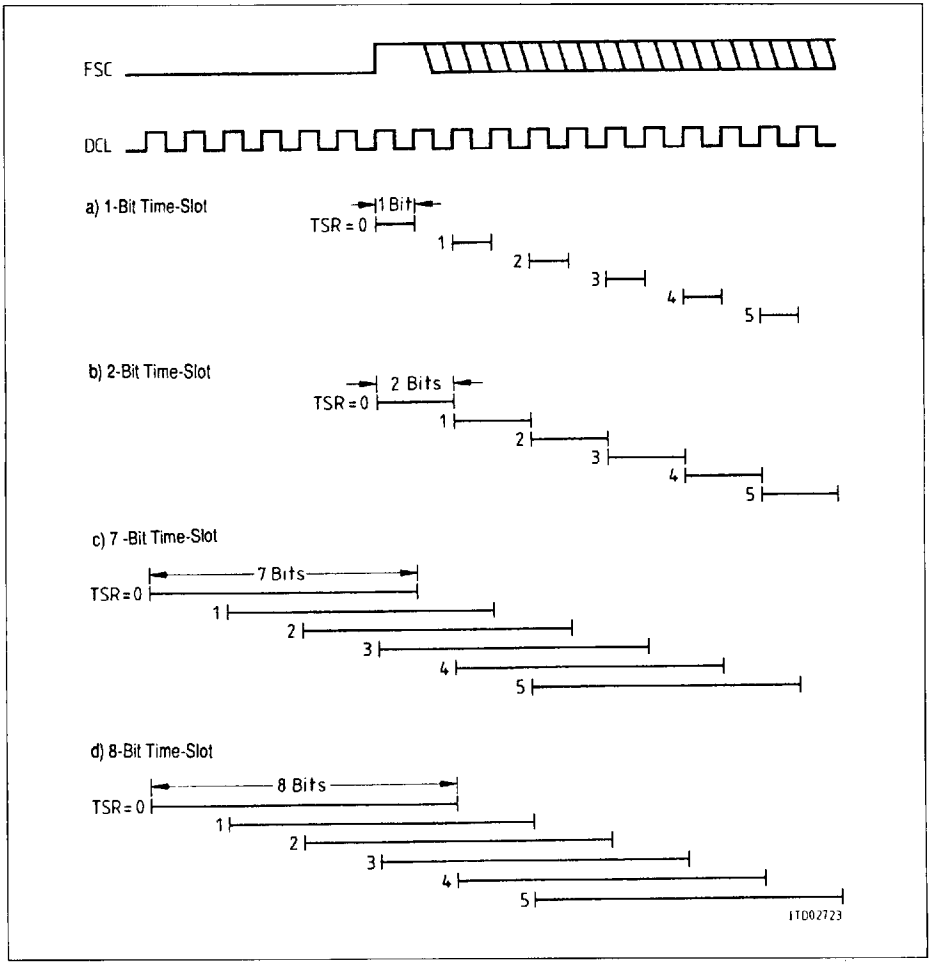


Figure 6
Position of Time Slot for Different Channel Widths as a Function of TSR Register Contents

Quad Connection Common Control Mode

Channel selection is performed by an active high strobe signal provided through the FSC input. The strobe signal is common to all four HDLC channels.

The $\overline{TSC}$ output is active when the FSC strobe is active.

Single ConnectionTS Mode

The time slots selected by the TSR registers all pertain to the same PCM highway. The programming of a channel otherwise proceeds exactly as explained above.

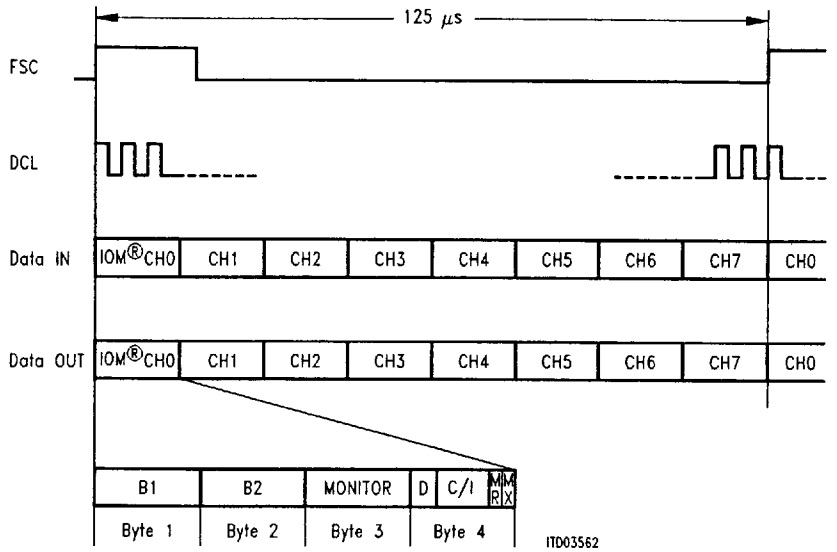
The tristate control output line $\overline{TSC}$ marks the time slots when data is transmitted/received by any of the four controllers.

Single Connection IOM - Mode

The IOM is an interface where a frame is composed of n IOM channels (n 1; n = 8 in **figure 7**). Each IOM channel has a unique structure. It consists of: two eight-bit bytes, corresponding to the ISDN B channels, a MONITOR byte, and a control byte of which the first two bits are allocated to the ISDN D channel.

In the single connection IOM mode the serial interface has an IOM frame structure and the four HDLC channels are assigned to the D bits of four consecutive IOM channels. The choice whether the four HDLC controllers are assigned to IOM channels 0 - 3 or 4 - 7 is governed by the microcontroller bit VIS (Common Configuration Register). See **figure 7**.

a) Multiplexed Frame Structure of the IOM® Interface (n = 8)



b) Assignment of HDLC Channels in IOM® Mode

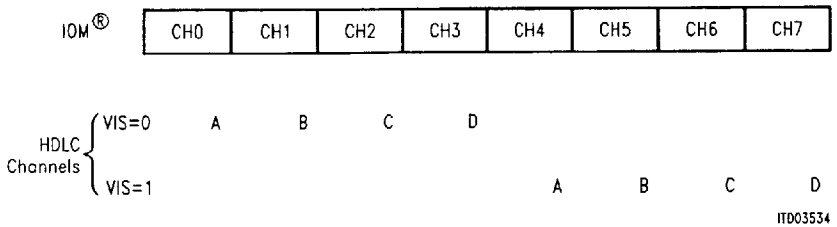


Figure 7

2.4.2 HDLC Communication Functions

Basic HDLC Functions

Each one of the four controller channels handles the following basic HDLC functions.

Receive direction

- Flag detection
  A zero followed by six consecutive ones and another zero is recognized as a flag.
- Zero delete
  A zero after five consecutive ones within an HDLC frame is deleted.
- Address recognition
  A frame may be accepted or rejected on the basis of a comparison of the most significant address byte (Service Access Point Identifier SAPI in Link Access Procedure for the D-channel LAPD) with three fixed SAPI values.
- CRC checking
  The CRC field of an HDLC frame is checked according to the generator polynomial $x^{16} + x^{12} + x^5 + 1$.
- Check for abort
  Seven or more consecutive ones are interpreted as an abort sequence.
- Check for idle
  Fifteen or more consecutive ones are interpreted as "idle", and reported to the processor via a status bit.
- Minimum length checking
  Reception of frames with less than three bytes between opening and closing flag is not reported to the microcontroller.

Transmit direction

- Flag generation
  A flag is generated at the beginning and at the end of every frame.
- Zero insert
  A zero is inserted after five consecutive ones within an HDLC frame.
- CRC generation
  The CRC field of the transmitted frame is generated according to the generator polynomial $x^{16} + x^{12} + x^5 + 1$.
- Abort sequence generation
  An HDLC frame may be terminated with an abort sequence under software control or due to a FIFO underrun condition.
- Inter-frame time fill
  As inter-frame time fill either flags or idle (continuous ones) may be transmitted.

Reception and Transmission Functions

FIFO Structure

Each HDLC controller uses a 64-byte FIFO per direction for the intermediate storage of data packets. All data bytes between the opening flag and the CRC field of an HDLC frame are passed through the FIFO.

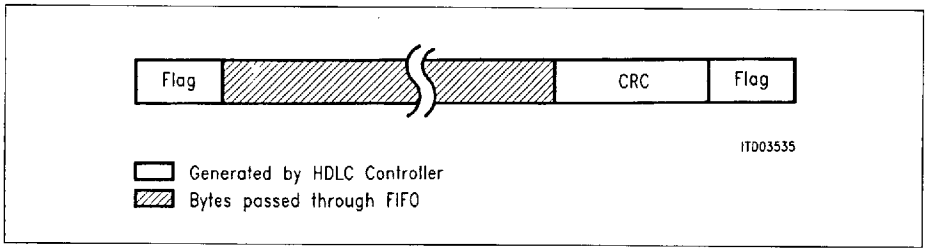


Figure 8
HDLC Frame Structure

The receive and transmit FIFOs are both divided, two blocks of 32 bytes each: One accessible to the microcontroller and one inaccessible to the microcontroller. While the microcontroller is reading (receive FIFO) or writing (transmit FIFO) data in one 32-byte block, the other block is filled (receive FIFO) or emptied (transmit FIFO) by the IDEC. Thus the length of the received or transmitted frame is not limited by the FIFO size.

Reception of Frames

Address Compare

Before a receive frame is stored, its address (the first byte following the opening flag) may optionally be compared against three fixed values.

SAPG	"Group SAPI"	63_D
SAPS	"Signaling SAPI"	0_D
SAPP	"Packet SAPI"	16_D

Each address compare may be individually enabled or disabled for each HDLC channel via bits AC0, 1, 2 and 3 (ACR register).

The effect of a match is programmable as shown in **table 4**. In the table it is assumed that the address compare enable bit (AC) is set for the channel in question. If AC = 0, all valid receive frames in that channel are accepted.

Table 4
Address Compare Logic

SCM	SCG	SCS	SGP	Effect	
	0	0	0	Accept all frames	
	0	0	1	Reject frames with	SAPP (16_D)
0	0	1	0		SAPS (0_D)
	0	1	1		SAPS (0_D) and SAPP (16_D)
	1	0	0		SAPG (63_D)
	1	0	1		SAPG (63_D) and SAPP (16_D)
	1	1	0		SAPG (63_D) and SAPS (0_D)
	1	1	1		SAPG (63_D), SAPS (0_D) and SAPP (16_D)
	0	0	0	Reject all frames	
	0	0	1	Accept frames with	SAPP (16_D)
1	0	1	0		SAPS (0_D)
	0	1	1		SAPS (0_D) and SAPP (16_D)
	1	0	0		SAPG (63_D)
	1	0	1		SAPG (63_D) and SAPP (16_D)
	1	1	0		SAPG (63_D) and SAPS (0_D)
	1	1	1		SAPG (63_D), SAPS (0_D) and SAPP (16_D)

Frame Storage

When a frame is accepted, it is stored in the receive FIFO.

In the case of a frame of length less than to 64 bytes, the whole frame may be stored in the receive FIFO. After the first 32 bytes have been received, the device prompts the microcontroller to read data from the FIFO (Receive Pool Full RPF interrupt status). Having done this, the microcontroller releases the FIFO. This is done by the RMC (Receive Message Complete) software command, after which the rest of the frame, when ready, is made available to the microcontroller (**figure 9**).

When a whole frame shorter than 32 bytes, or the final part of a frame longer than that becomes available, the condition is indicated by an RME (Receive Message End) interrupt status, instead of RPF.

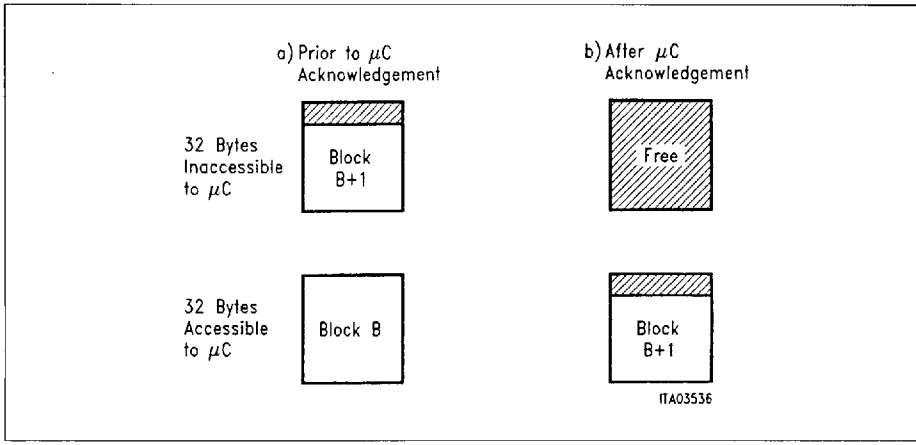


Figure 9
Receive FIFO in the Case of a Frame No Longer than 64 Bytes.

In the case of frames at least 64 bytes long, the microcontroller will repeatedly be prompted by an interrupt lo read out the FIFO in blocks of 32 bytes (except possibly the final block). Again, after reading a block, the microcontroller acknowledges the data by a software command and thus releases the FIFO. If this is not done before an additional 32-data bytes are received, the next data byte will lead to a "data overflow" condition.

In the case of several shorter frames up to seventeen may be stored inside the HDLC controller. After an interrupt (RME), one frame is available in the FIFO for the microcontroller to read. Up to sixteen other frames may be stored in the meanwhile in the upper half of the FIFO (**figure 10**). When the microcontroller releases the current data block from the FIFO by software command, the next frame becomes available and the corresponding space is freed in the upper half for (a) subsequent frame(s) (**figure 10**).

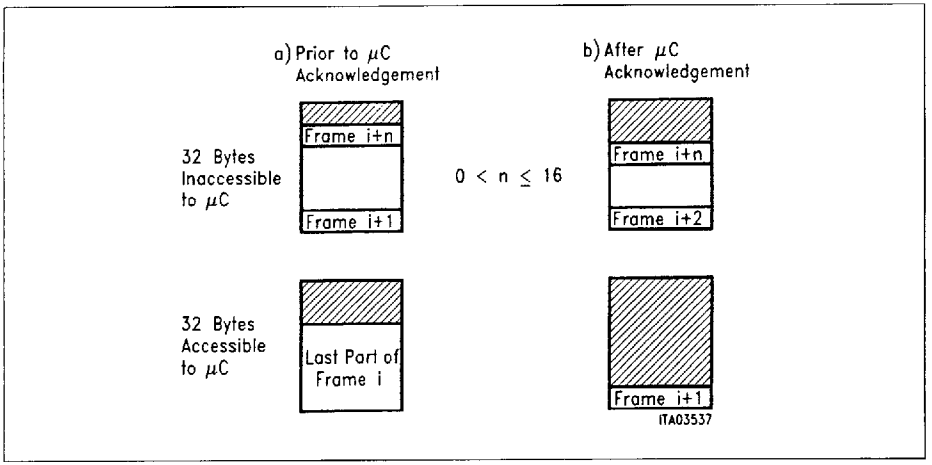


Figure 10
Receive FIFO in the Case of Short Frames

The interrupts accumulating in the process are incorporated into a queue and transferred one by one to the microcontroller as well as additional information about the frame. In particular, the frame length is stored in a register. Information such as "frame aborted yes/no" and "CRC error yes/no" and "data overflow yes/no", is included in an extra byte stored in the FIFO after the last byte of the corresponding frame.

Every interrupt has to be acknowledged by the microcontroller. A full FIFO at the beginning of a frame will lead to a frame overflow condition.

If the microcontroller does not wish to preserve an incoming frame, the possibility exists to ignore it. When the corresponding command (RMD) is issued, the part of the frame stored is deleted and the rest of the entire frame will be ignored.

Transmission of Frames

2 x 32 bytes of intermediate storage are provided per HDLC controller in the transmit direction. After up to 32 bytes have been written to the FIFO, transmission is started by a software command (XHF). If the previous transmission is still underway when a new transmission command is issued, microcontroller access to the FIFO will be blocked until the first transmission is completed (**figure 11**). This means that at most one complete frame may be written to the FIFO before a transmission is initiated. If a transmission request does not include a "frame end" indicator (XME), the HDLC controller will request the next data block via an interrupt if the FIFO contains no more than 32 bytes. This procedure will be repeated until the microcontroller indicates that the frame is to be closed.

In the case when this indication is not given and there is no more data ready for transmission, the frame is terminated with an abort sequence and the microcontroller is notified via a transmit data underrun (XDU) interrupt. The frame may also be aborted per software command. The completed transmission of an HDLC frame is reported by an XPR (Transmit Pool Ready) interrupt status..

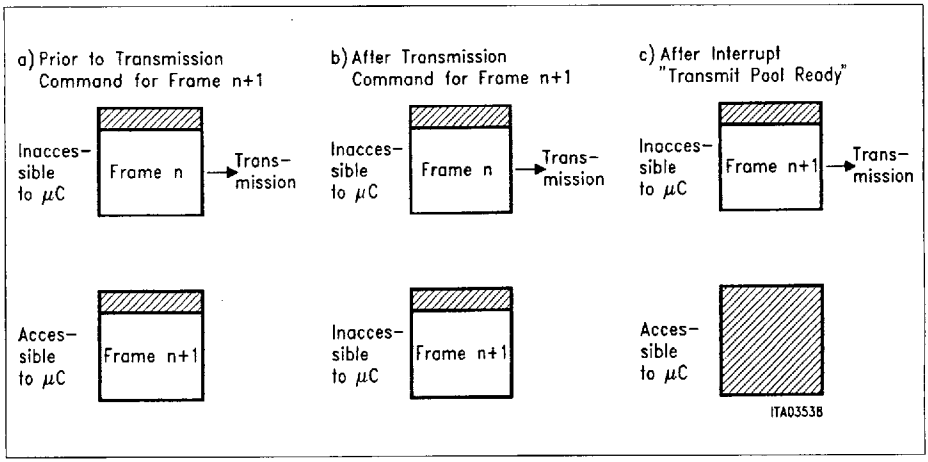


Figure 11
Transmit FIFO

2.4.3 Collision Control and Switching Functions

The IDEC possesses flexible collision control capabilities which are totally transparent to the microcontroller. The collision control modes enable use of the circuit in statistical multiplexing applications or in centralized or de-centralized packet switches. Each of the four HDLC controllers is individually programmed in one of four modes by its own register bits CMS1-0 (Collision Mode Select).

Table 5 lists the four collision modes that can be selected, along with the auxiliary I/O lines used in each case. The outputs SD1 X and SD2X can be selected to be of the open-drain or of the push-pull type.

Table 5
Collision Modes of the IDEC

CMS1	CMS0	Description	Auxiliary I/O Data IN	Data OUT	Coll. IN	Coll. OUT
0	0	Unconditional transmission				
0	1	Slave mode			CDR	
1	0	Multi-master mode			CDR	
1	1	Master mode	CDR	SD1X		SD2X

Unconditional Transmission Mode

The HDLC controller transmits frames without collision detection on the transmit line (time channel).

Slave Mode

The input CDR (Collision Data Receive) is used to control transmission of frames. This input is common to all HDLC controllers which are programmed in the slave mode.

Transmission is inhibited by a "low" on the CDR input. If CDR becomes "low" during the transmission of a frame, the frame is aborted by the HDLC controller, and the data output is set to high impedance. Refer to **figure 12**.

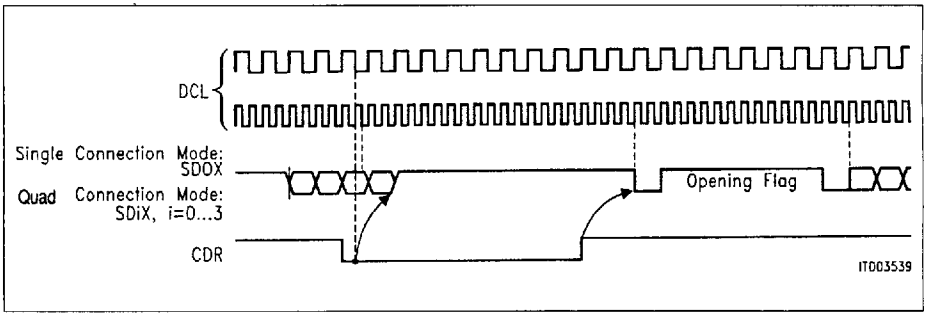


Figure 12
Transmission Control in the Slave Mode (example)

Note:

The CDR is evaluated

- at the falling edge of DCL, for a DCL rate equal to the data rate;
- at the falling edge of DCL immediately preceding the rising edge used for transmission, for a DCL rate twice the data rate.

The state of CDR is evaluated by the HDLC controller only in the time channel used for transmission by that controller. (**Figure 12** is simplified in that the grouping of bits into time slots on SD0X ... SD3X and CDR is not depicted, i. e. bits outside the transmit time channel are not shown.)

When CDR is switched high, inter-frame time fill is marked in the transmit time channel if no transmission request is pending, otherwise transmission starts at the first available instant. Transmission of a previously aborted frame is automatically re-started by the HDLC controller if the beginning of the frame is still available in the transmit FIFO. Otherwise an interrupt (XDU) to the microcontroller indicates that the transmission has failed.

The slave mode is applicable in all of the basic operation modes, in both single connection and quad connection applications. However, there is only one CDR line. This should especially be noted if:

- the IDEC is configured in the quad connection common control mode and more than one HDLC controller is operated in the slave mode;
- when the same time slot is used by more than one HDLC controller in the slave mode.

In both cases more than one controller is evaluating the CDR line during the same time interval, and when CDR goes "low" they all stop transmitting.

Multi-Master Mode

In the multi-master mode the controllers perform a bus access procedure and collision detection in their assigned time channel(s). As a result, any number of IDECs can be assigned to one physical channel, where they perform statistical multiplexing.

Collisions are detected by automatic comparison of each transmitted bit with the bit received via the CDR input. For this purpose a logical "and" of the bits transmitted by parallel controllers is formed and connected to the input CDR. This may be implemented most simply by defining the output line driver to be of the open drain type (ODS = 1). Consequently the logical "and" of the outputs is formed by simply tying them together ("wired or"). The result is returned to the CDR input of all parallel circuits.

The multi-master mode is applicable in all operating modes, in both single connection and quad connection applications. In the quad connection mode, those output lines (SD0X ... SD3X) for which this collision mode is selected may be connected to CDR. The four HDLC controllers may either be programmed to transmit in separate time channels or in the same time channel. A prerequisite for the multi-master mode is that the inter-frame time fill used is "idle".

The multi-master operation is as follows (refer to **figure 13**).

When a mismatch between a transmitted bit and the bit on CDR is detected, the HDLC controller stops sending further data and its output is set to high impedance.

As soon as it detects the transmit bus to be "idle" again, the controller automatically attempts to re-transmit its frame. By definition, the bus is assumed idle when x consecutive ones are detected in the transmit channel. Normally x is equal to 8.

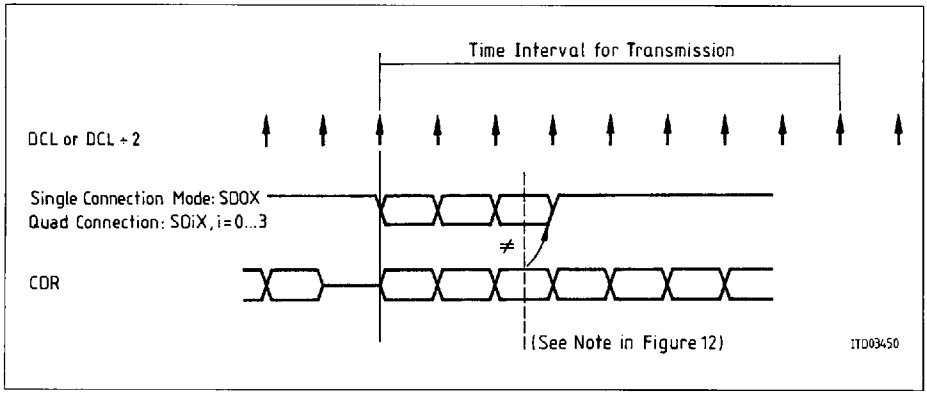


Figure 13
Collision Detection in the Multi-Master Mode (example)

An automatic priority adjustment is implemented in the multimaster mode. Thus, when a complete frame is successfully transmitted, x is increased to ten, and its value is restored to eight when a row of ten1's is detected on the bus (CDR). Furthermore, transmission of a new frame may be started by the HDLC controller after the tenth 1.

This multi-master, deterministic priority management ensures an equal right of access of every HDLC controller to the transmission medium, thereby avoiding blocking situations.

Master Mode

The master mode requires three auxiliary connections: data input CDR, data output SD1X and collision data out SD2X.

This mode is applicable only in single connection operation.

In the master mode, the controller performs two functions:

- Switching of data packets between the main connection SD0X, SD0R and the auxiliary input and output (CDR, SD1X)
- Resolution of collisions between data from the auxiliary connection CDR and HDLC frames from the local microcontroller.

Refer to **figure14**.

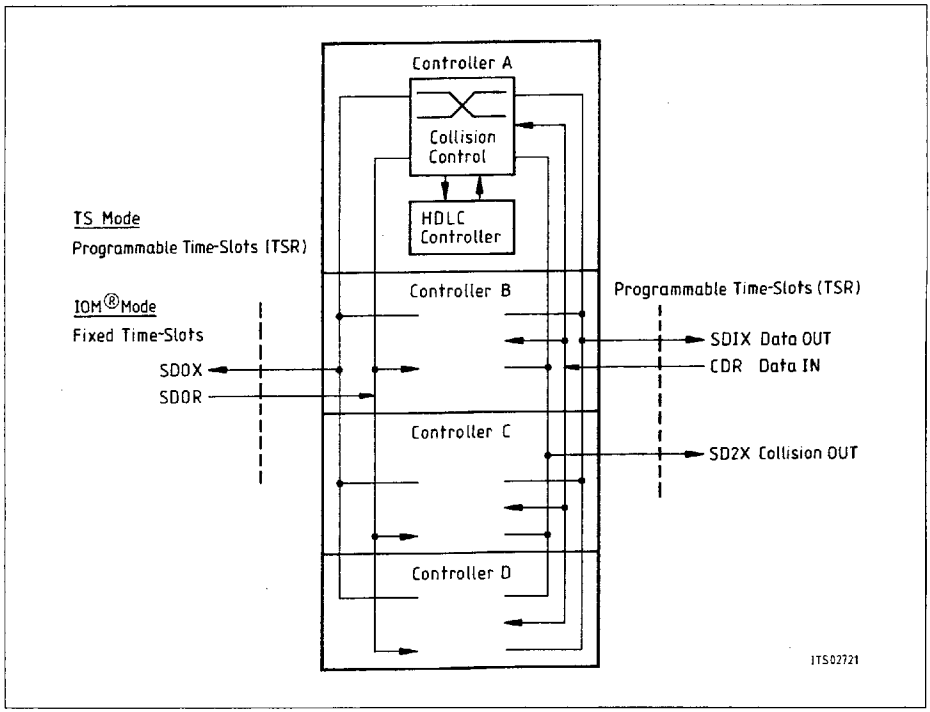


Figure 14
I / O Connections in the Master Mode

In the TS mode the time slot programmed via the Time-Slot Select Register TSR applies simultaneously to SD0X/SD0R and to the auxiliary lines CDR, SD1X and SD2X. In the IOM mode the TSR register selects a time channel on the auxiliary connections CDR, SD1X and SD2X only (however, the channel width selected should be two bits, as on the IOM interface, to ensure a correct data throughput).

The switching of data from SD0R to SD1X is transparent. The switching of data from CDR to SD0X depends on the state of the HDLC controller (transmit/no transmit) and on selected priorities, as follows.

When no transmission command is issued to the HDLC controller, data is transparently switched through from CDR to SD0X. When a transmit request is issued but the Force HDLC Frame (FHF) bit is not set to 1, the data currently being received (if any) on CDR is given priority. The HDLC controller starts transmitting its frame on SD0X only after CDR is detected to be idle, in other words, when a row of eight ones is observed on CDR. Simultaneously, SD2X is set "low" to indicate that no data will be accepted on CDR input data line.

Figure 15a shows the time relation between CDR (data in) and SD2X (collision out) as well as the logical relation between SD2X and SD0X (data out). The figures are simplified in that the grouping of bits into time slots on SD0X, and on SD2X/CDR is not depicted.

When a transmit command is issued and the Force HDLC Frame (FHF) bit is set to 1, the frame currently being received on CDR is aborted. Seven ones are appended to the last bit of the aborted frame on SD0X, after which the HDLC controller starts transmitting its frame (**figure 15b**).

In both cases, SD2X is set "high" again after a delay of eight bit-times following the last "0" of the closing flag, to indicate that data is accepted on the CDR input data line. However, if a new transmit command is issued before that time, SD2X remains "low" and transmission of the new frame starts immediately after the eighth 1.

Collision Resolution in the Master Mode with Programmable Priority (FHF)

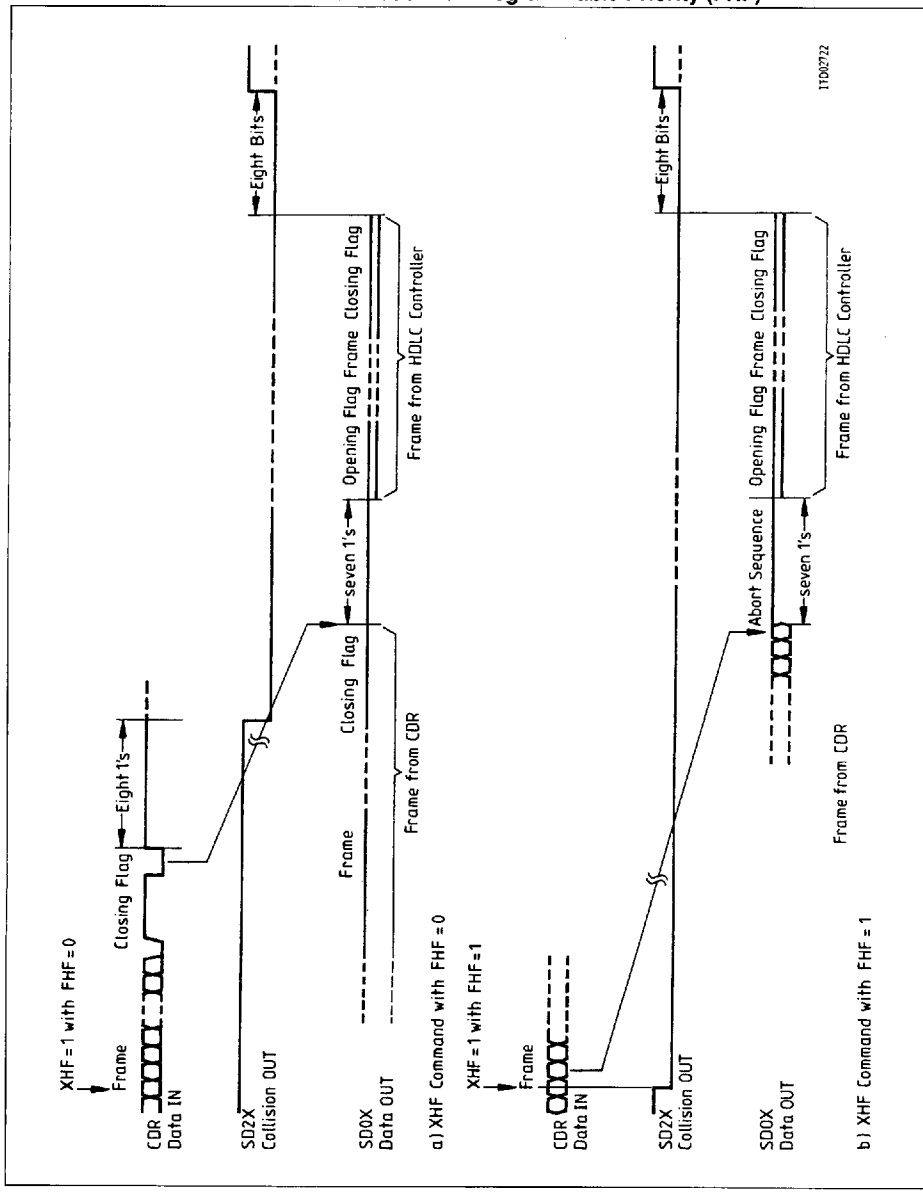


Figure 15

Note on Data Delay in Master Mode

The data bits are switched from SD0R to SD1X and from CDR to SD0X with a minimum delay as shown in **figure 16.**

Two different cases are distinguished:

a) TS mode.
In this case the time slots on SD0R/SD0X and on CDR/SD1X are identical. The data delay from CDR to SD0X is one bit, whereas the delay from SD0R to SD1 X is two bit times.
IOM mode with identical channel (time slot) on SD0R/SD0X and CDR/SD1X. This case is identical to the previous one.

b) IOM mode with a time slot on CDR/SD1X which does not coincide with the IOM channel bits on SD0R/SD0X. In this case, the data bits undergo (in addition to the inherent delay due to the different bit positions) a delay of one bit time from CDR to SD0X, whereas no additional bit delay is introduced when going from SDOR to SD1X.

Bit delay for coinciding channel/time slot position on SD0R/SD0X and on CDR/SD1X.

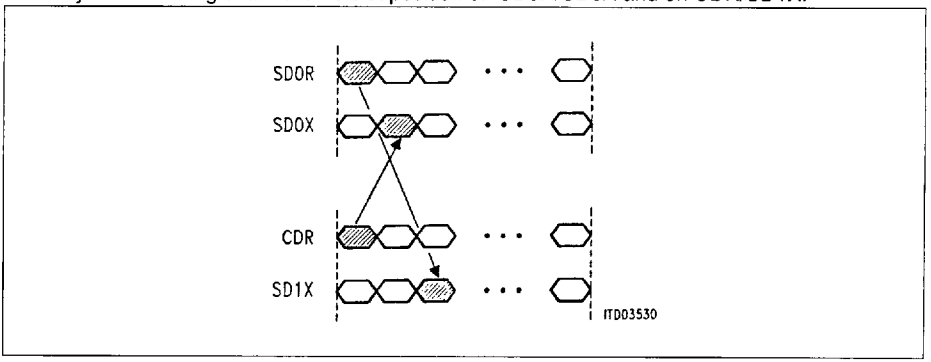


Figure 16a
Bit Delay from SD0R/CDR to SD1X/SD0X

Bit delay for non-identical channel/time slot position on SD0R/SD0X and on CDR/SD1X (possible only when SD0R/SD0X is an IOM interface).

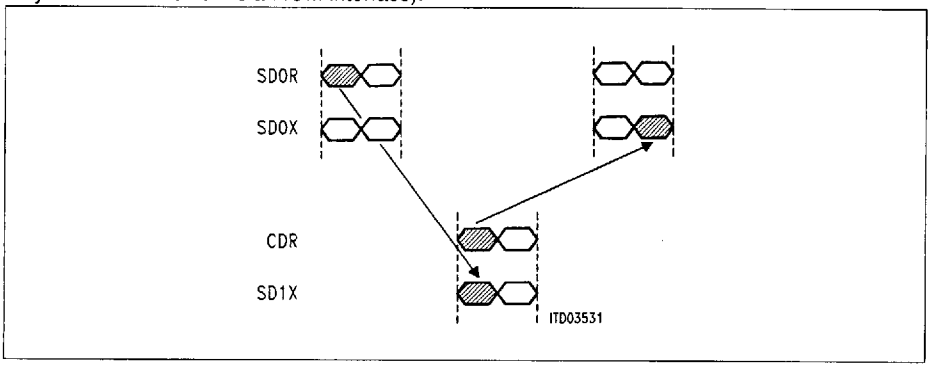


Figure 16b
Transmit Delay from SD0R/CDR to SD1X/SD0X

2.4.4 Test Functions

A test loop is provided in each of the four HDLC controllers of the IDEC. When the test loop is activated, the input and the output of the HDLC channel are connected together. The test loop control is independent for each HDLC channel (bit TLP).

The test loop is either transparent (forward data is outputted on the line) or non-transparent (forward data is not outputted on the line), depending on the selected mode. In the quad connection common control mode and in the single connection IOM mode the loops are transparent. In the other cases they are non-transparent. During a non-transparent loop, the data output is high impedance inside the assigned time channel.

2.5 Preprocessed Channels

The IDEC supports the

- Command/Indicate (C / I) channel at the IOM-2 interface.

The C/I handler takes care of the C/I channels.

C/I Channel Handler

To activate the C / I handler, CCR:CDEN is set to "1". The C/I handler can be used in the following switching modes:

- single connection IOM mode
- single connection time-slot mode

and in the following bus access modes:

- unconditional transmission
- master
- multi master (only 1 C / I transmitter is allowed per subscriber).

In the upstream direction the signaling handler MONITORS the received C / I channels. Upon a change

- an interrupt is generated (ISTAn:CD)
- the actual value is stored in registers CIR3 ... CIR0.

Only single last look is carried out. The C/I channel is sampled in each frame. The change detection only operates on the 4-bit C/I channel.

The ISTAn:CD interrupt is cleared when ISTAn is read.

In the downstream direction the value written to CIX3 ... CIX0 will be sent in the C / I channels in each frame.

3 Operational Description

3.1 Microprocessor Interface Operation

The IDEC microcontroller interface can be selected to be either of the

1. Motorola type with control signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$; address bus A0 ... 6; data bus AD0 ... 7
2. Siemens/Intel non-multiplexed bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$; Address bus A0 ... 6; data bus AD0 ... 7
3. or of the Siemens/Intel multiplexed address/data bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE; address/data bus AD0 ... 7

For a non-multiplexed bus including the Motorola type P interface the P-LCC-44 package of the IDEC needs to be used, since only this package provides the additional pins for a separate 7-line address bus.

The ALE input is used to control the interface type as follows

ALE tied to V_{DD} ⇒ (1)
ALE tied to V_{SS} ⇒ (2)
Edge on ALE ⇒ (3)

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects interface type (3). A return to one of the other interface types is possible only if a hardware reset is issued.

Table 6
Microcontroller Interface Summary

ALE	Interface	Bus Type	Address Bus	Data Bus	Control Pins					
					P-DIP-28			P-LCC-44		
					11	5	4	17	8	7
Tied to V_{DD}	Motorola	non-multiplexed	A0 ... 6	AD0 ... 7				$\overline{CS}$	R/$\overline{W}$	$\overline{DS}$
Tied to V_{SS}	Siemens/ Intel	non-multiplexed	A0 ... 6	AD0 ... 7				$\overline{CS}$	$\overline{WR}$	$\overline{RD}$
Switching	Siemens/ Intel	multiplexed	AD0 ... 6	AD0 ... 7	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$

3.2 Reset

After a hardware reset (pin RES), the configuration/command register bits are zeroed. No interrupts are active and all outputs are in a high impedance state.

Table 7 sums up the state of the IDEC immediately after a hardware reset has been applied.

Table 7
State of IDEC After a Hardware Reset

Register Name		Value after Hardware Reset (hex)	Meaning
Common registers			
	ACR	00	Address comparison disabled.
	CCR	00	Single connection TS mode. Interrupt vector may be read on AD bus bits 0 - 3. Bits per frame: 257 to 512. Bit rate is equal to clock rate. Output drivers are of the push-pull type.
	VISR	00	No interrupt from any IDEC channel.
	VISM	00	All channel interrupts are enabled.
Individual registers i = A, B, C, D			
	ISTA	00	No interrupts from channel i.
	ISM	00	All channel i interrupts enabled.
	STAR	50	Transmit FIFO is ready to be written to. Receive line is idle.
	CMDR	00	No commands.
	MODE	00	Test loop not active. No collisions will be detected (unconditional transmission). Inter-frame time fill = idle. Receiver de-activated. Channel i disabled (high impedance output). Channel capacity is 2 bits/time slot.
	RFBC	00	Zero bytes received.
	TSR	00	Time slot 0 selected.

3.3 Initialization

The purpose of the initialization is to set the IDEC into a state where it is able to correctly transfer HDLC frames and to manage collisions according to the requirements of the application.

The initialization process is divided into two phases. First, the common settings are determined via the registers CCR and VISM. These registers determine the number of HDLC channels used, the serial interface configuration and common characteristics of the serial input/output connections (**table 8**).

Table 8
Initialization of IDEC(common bits)

Function	Register	Bits	Effect
Configuration	CCR	MDS1-0	Basic configuration and timing mode
Serial interface characteristics	CCR	ODS	Output driver type is open-drain or push pull
		CRS	Clock rate = 1 or 2 x data rate
		BNS	Number of bits per PCM frame
Interrupt configuration	VISM	MIC3-0	Mask any HDLC channel(s)
	CCR	VIS	VISR may be read on AD bus bits 0-3 or 4-7
HDLC address recognition features	ACR	SCM	Address compare mode: accept/reject
		SCG, SCS, SCP	Selection of compare addresses
		AC0-3	Address compare on/off for HDLC channel 0, 1, 2, 3

Secondly, each of the HDLC channels is initialized via its own register set as shown in **table 9**.

The optional address comparison mode for each HDLC channel is selected by programming the ACR register, located in the common address space (**table 8**).

Table 9
Initialization of HDLC Channels (channel-per-channel)

Function	Register	Bits	Effect
Serial interface	MODE	CMS1-0 CCS1-0	Collision mode Channel capacity
	TSR	TSR7-0	Time slot
HDLC Controller	MODE	ITF	Inter-frame time fill pattern
		TLP	Test loop
		CAC	Active channel (enable receiver + transmitter, enable data outputs)
		RAC	Activate HDLC receiver

3.4 Interrupt Structure

Special events are reported to the processor by an interrupt logic in the IDEC. This logic allows the connection of more than one IDEC to one interrupt input of a microcontroller.

The interrupt structure of the IDEC is depicted in **figure 17**. Each HDLC channel of the circuit has its own Interrupt Status Register (ISTA) where up to five possible interrupt causes may be read directly. When an interrupt occurs in one of the HDLC channels, the corresponding bit is set in the ISTA register and the interrupt line ($\overline{INT}$) is activated. Simultaneously, a bit in the Vectored Interrupt Status Register (VISR) is set which indicates which of the four HDLC channels initiated the interrupt. Thus, to determine the cause of an interrupt, the microcontroller performs successively a read of the VISR register (address 36/3F) and a read of that ISTA register which was indicated by the contents of VISR.

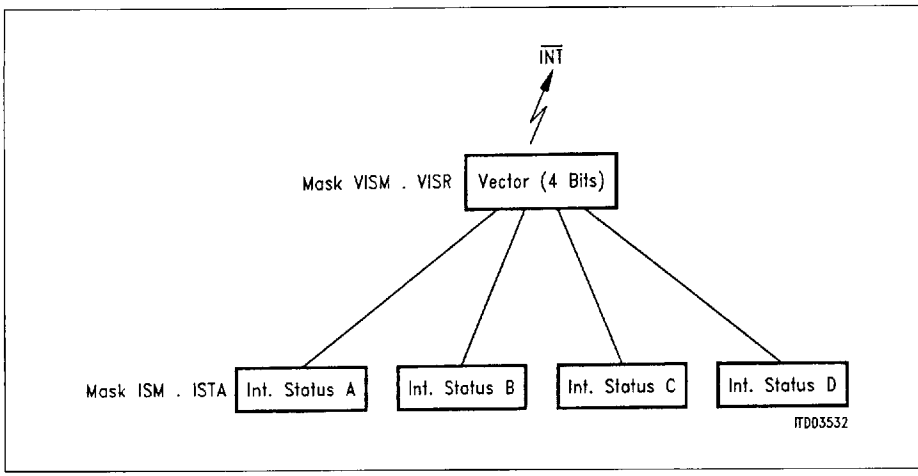


Figure 17
Interrupt Structure of the IDEC

A read of the ISTA clears the register and deactivates the $\overline{INT}$ line.

The position which the four bits of the Vectored Interrupt Status Register occupy on the AD7-0 bus when the register is read, is programmable via the Vectored Interrupt Selection bit VIS (CCR register). Thus, when VIS = 0, the VISR bits are read on AD bit positions 0-3, and when VIS = 1, VISR bits are read on AD bit positions 4-7. Unoccupied bit positions on the bus remain in a high impedance state.

The bits in VISR can be selectively masked by setting the corresponding bits in the Vectored Interrupt Status Mask (VISM) register to prevent one or several controllers from generating an interrupt. In that case, interrupts remain internally stored (pending) but are not displayed in the VISR or ISTA registers. Further, ISTA interrupts pertaining to a particular channel may be selectively masked via the Interrupt Status Mask register of that channel. Pending interrupts will cause the $\overline{INT}$ line to be activated and will be reported via ISTA (and VISR) only when the mask bits in ISM (and VISM) have been reset.

3.5 Processing

After being initialized via the configuration/mode registers listed in **tables 8** and **9** the IDEC is operational.

The control of the data transfer is performed by commands from the microcontroller written in the Command Register (CMDR). Events pertaining to the data transfer are reported via the Interrupt Status Register (ISTA) pointed to by the Vectored Interrupt Status Register (VISR). Other events which do not lead to interrupts may be monitored via the Status Register (STAR) and information about the receive frames is found in the RFIFO and in the Receive Frame Byte Counter (RFBC) register.

The powerful FIFO logic, which consists of a 2 x 32 byte receive and a 2 x 32 byte transmit FIFO per channel, as well as an intelligent FIFO controller, builds a flexible interface to the upper protocol layers implemented in the microcontroller.

Receive Frame Processing

Reception of HDLC frames with three or more bytes between the opening and closing flags is always reported to the microcontroller if address comparison is not enabled (AC = 0). If address comparison is enabled, the reception of the frame is dependent on the first byte of the received HDLC frame address field and the selected features of the address compare function (**table 4**).

All bytes between the opening flag and the CRC field are stored in the RFIFO.

When the frame (excluding the CRC field) is not longer than 31 bytes, the whole frame is transferred in one block. The reception of the frame is reported via the Receive Message End (RME) interrupt. The length of the frame can be read out from an 8-bit register (RFBC). A status byte is appended to the data in the RFIFO after an RME interrupt. It includes information about the frame, such as frame aborted yes/no or CRC valid yes/no. The frame and the status byte remain stored until the microcontroller issues an acknowledgment (Receive Message Complete: RMC).

A frame longer than 31 bytes is transferred to the microcontroller in blocks of 32 bytes plus one remainder block of length 0 to 31 bytes plus status byte. The reception of a 32-byte block is reported by a Receive Pool Full (RPF) interrupt and the data in RFIFO remains valid until this interrupt is acknowledged (RMC). This process is repeated until the reception of the remainder block reported by RME (**figure 18**). Bits 0-4 of the RFBC register represent the number of bytes stored in the RFIFO, including the status byte. Bits 7-5 indicate the total number of 32-byte blocks which were stored until the reception of the remainder block. Bits 7-5 do not overflow when the counter status 7 has been reached and indicate in this case a message length greater than 223 bytes.

The contents of the RFBC register are valid only after the occurrence of the RME interrupt, and remain valid until the microprocessor issues an acknowledgment (RMC). All receive interrupts accumulated in the meantime are stored (along with the status bytes and respective frame lengths) inside the controller and transferred one by one to the microcontroller after each RMC acknowledgment. If a frame could not be stored due to a full FIFO, the microcontroller is informed of this via the Receive Frame Overflow interrupt (RFO).

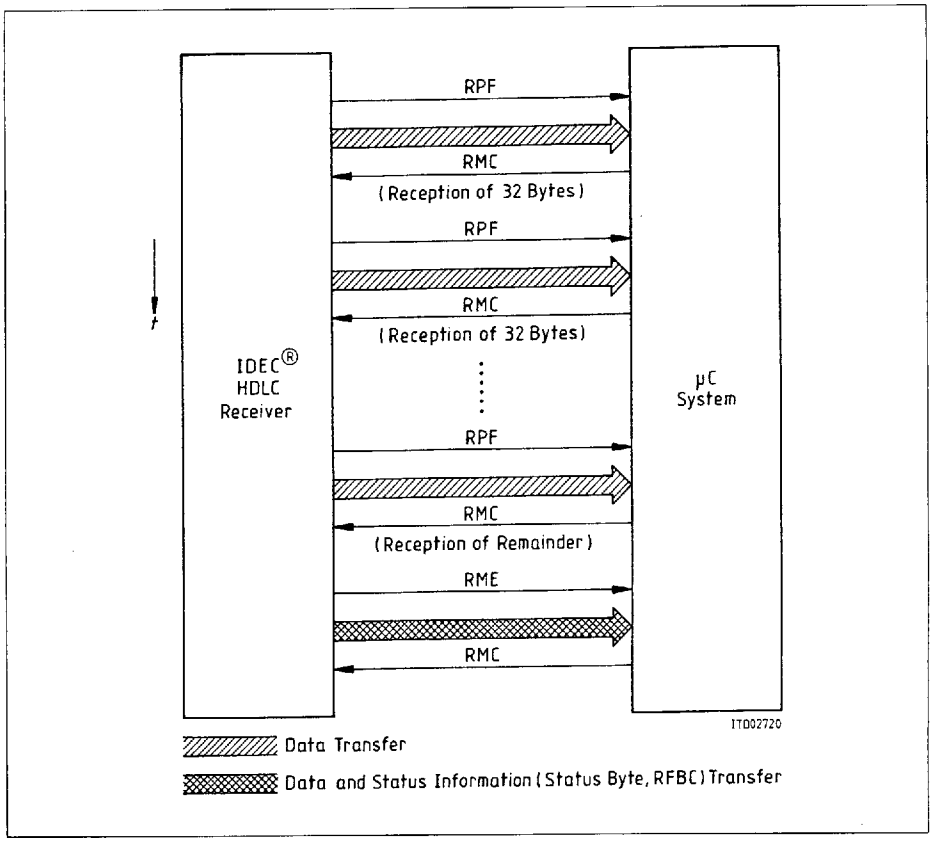


Figure 18
Reception of an HDLC Frame

Transmit Frame Processing

After checking the XFIFO status by polling the Transmit FIFO Write Enable (XFW) bit or after a Transmit Pool Ready (XPR) interrupt, up to 32 bytes may be entered by the microcontroller in the XFIFO. Transmission of an HDLC frame is started when the Transmit HDLC Frame (XHF) command is issued. The HDLC controller will request another data block by an XPR interrupt if there are no more than 32 bytes in the XFIFO and the frame close command bit (Transmit Message End XME) has not been set. When XME is set, all remaining bytes in the XFIFO are transmitted, the CRC field and the closing flag of the HDLC frame are appended and the controller generates a new XPR interrupt (**figure19**).

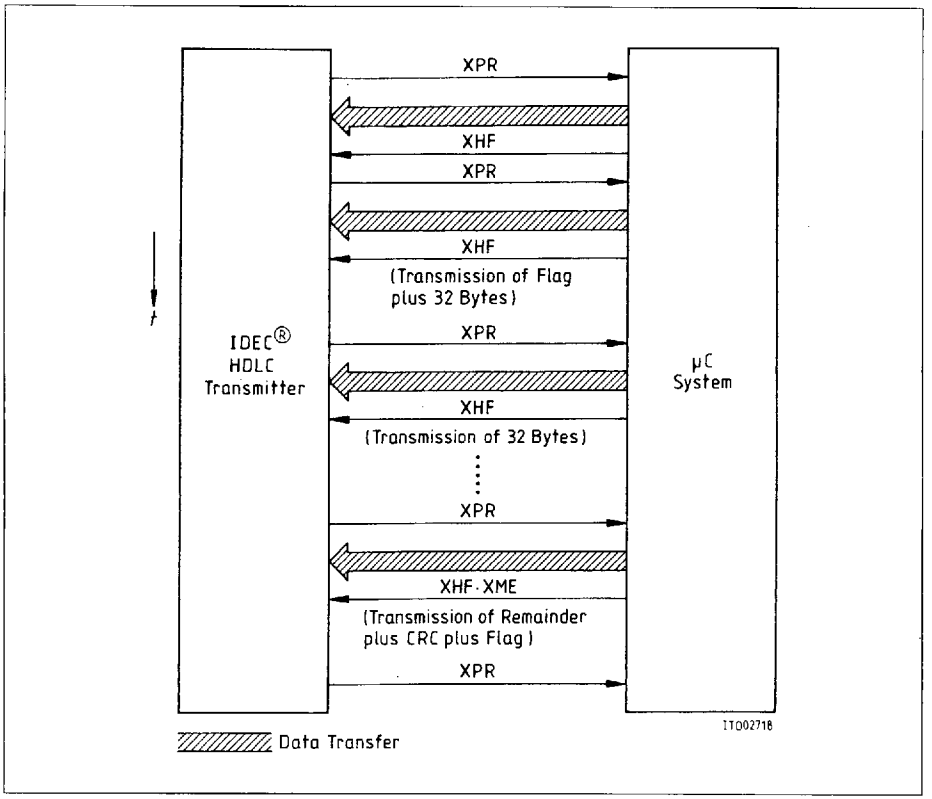


Figure 19
Transmission of an HDLC Frame

The microcontroller does not necessarily have to transfer a frame in blocks of 32 bytes. As a matter of fact, the sub-blocks issued by the microcontroller and separated by an XHF command, can be between 1 and 32 bytes long.

If the XFIFO runs out of data and the XME command bit has not been set, the frame will be terminated with an abort sequence (seven 1's) followed by inter-frame time fill, and the microcontroller will be advised by a Transmit Data Underrun (XDU) interrupt. An HDLC frame may also be aborted by setting the Transmit Reset (XRES) command bit.

Table 10 gives a summary of possible interrupts from the HDLC controller and the appropriate reaction to these interrupts.

Table 10
Possible Interrupt Causes and Reactions

Mnemonic	Meaning	Reaction
RPF	Receive Pool Full	Read 32 bytes from RFIFO and acknowledge with RMC.
RME	Receive Message End	Read "RFBC4-0" bytes from RFIFO and acknowledge with RMC.
RFO	Receive Frame Overflow	Error report for statistical purposes (loss of a complete frame). Probable cause: deficiency in software.
XPR	Transmit Pool Ready	Write data bytes in the XFIFO if the frame currently being transmitted is not finished or a new frame is to be transmitted, and issue an XHF (and possible XME) command.
XDU	Transmit Data Underrun	Acknowledged by a read of the ISTA. Possible causes: Excessive software reaction times, or transmit data collision.

Table 11 lists the most important commands which are issued by a microcontroller by setting one or several bits in the Command Register (CMDR).

Table 11
List of Commands

Command Mnemonic	Hex	Bit 7 ... 0		Meaning
RMC	80	1000	0000	Receive Message Complete. Acknowledges a block (RPF) or a frame (RME) stored in the RFIFO.
RRES	40	0100	0000	Reset HDLC Receiver. The RFIFO is cleared and the receiver is ready for reception.
RMD	20	0010	0000	Receiver Message Delete. The part of the frame in the RFIFO is deleted and the rest of the frame will be ignored by the receiver.
XHF	08	0000	1000	Transmit HDLC Frame. Enables the transmission of the block entered last into the XFIFO. The frame is not yet complete.
XHFC	0A	0000	1010	Transmit a HDLC Frame and close it with CRC and flag.
F_XHF F_XHFC	0C 0E	0000 0000	1100 1110	Same as preceding, but used in master mode to enforce a transmission even in the case of a collision.
XRES	01	0000	0001	Reset Transmitter. Clears the XFIFO; any frame currently being transmitted is aborted.

4 Detailed Register Description

The following symbols are used throughout chapter 4

x... don't care

n... not used. It has to be set to logical "0" in write accesses but may be switched by the IDEC to either logical level in read accesses.

4.1 Register Address Layout

The register set consists of:

- one configuration register common to all four channels (CCR)
- a maskable vectored interrupt status register (VISR, VISM)
- a register for setting the HDLC address recognition mode for the four channels (ACR)

and, for each of the four channels, a set of individual registers.

Multiplexed Address Bus

In order to support the use of a 16-bit microcontroller with multiplexed address bus, each register can be accessed with an even and an odd address value (**figure 20**).

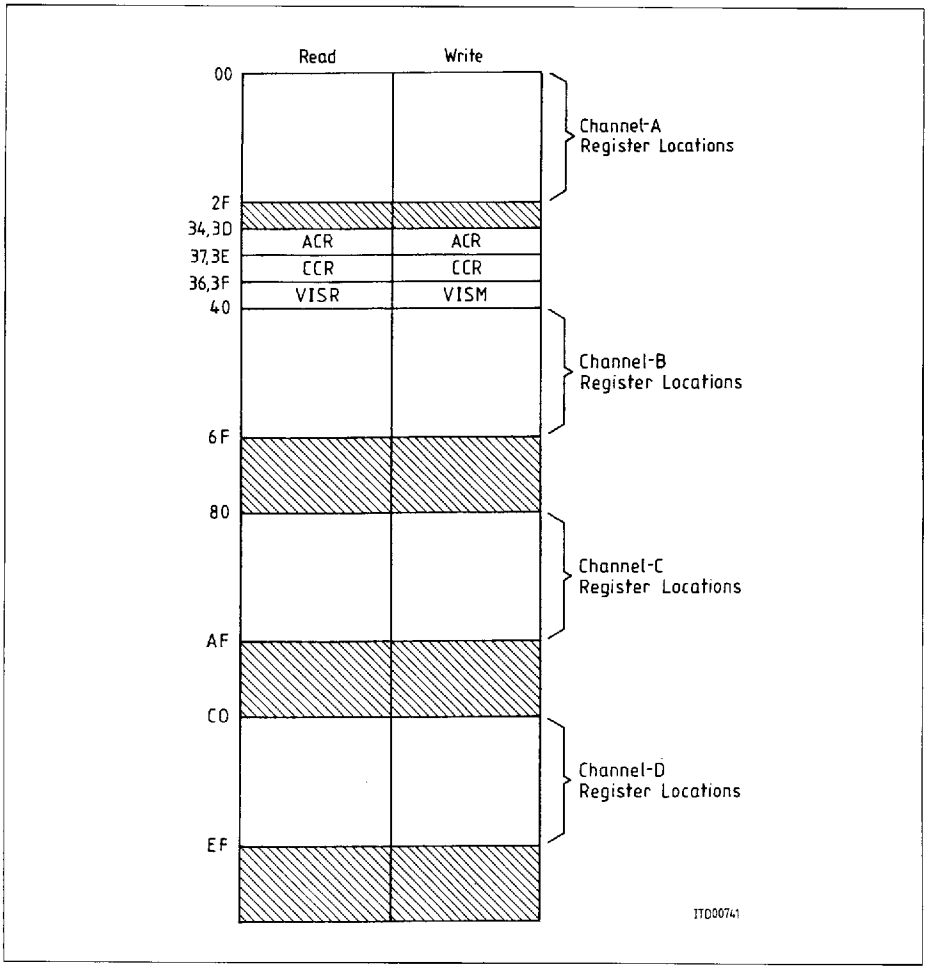


Figure 20
IDEC Register Map for a Multiplexed Address Bus

The address map of the individual registers of each channel is shown in **table 12**. In order to obtain the actual address of a register, a "base" has to be added to the address given in the table, as follows:

base = 00 for channel A
20 for channel B
40 for channel C
C0 for channel D.

Table 12
Address Map of HDLC Channel Registers (multiplexed address bus)

Address		Read	Write
Even	Odd		
00 to 1F		RFIFO	XFIFO
20	29	ISTA	ISM
28	21	STAR	CMDR
22	2B	MODE	MODE
2C	25	RFBC	TSR
2A	23	CIR	CIX

Non-Multiplexed Address Bus

The address layout is shown in **figure 21**.

The address map of the individual registers of each channel is shown in **table 13**. In order to obtain the actual address of a register, a "base" has to be added to the address given in the table, as follows:

base = 00 for channel A
20 for channel B
40 for channel C
60 for channel D.

Table 13
Address Map of HDLC Channel Registers

Address	Read	Write
00 to 0F	RFIFO	XFIFO
10	ISTA	ISM
11	STAR	CMDR
12	MODE	MODE
15	RFBC	TSR
13	CIR	CIX

Note:

The address values in the multiplexed A/D bus and non-multiplexed address bus cases are related to each other as follows.

Let AD0...7 be the multiplexed address bits and let A0...6 be the non-multiplexed address bits.

Then: A0 = AD0 exor AD3
A1 = AD1
A2 = AD2
A3 = AD4
A4 = AD5
A5 = AD6
A6 = AD7.

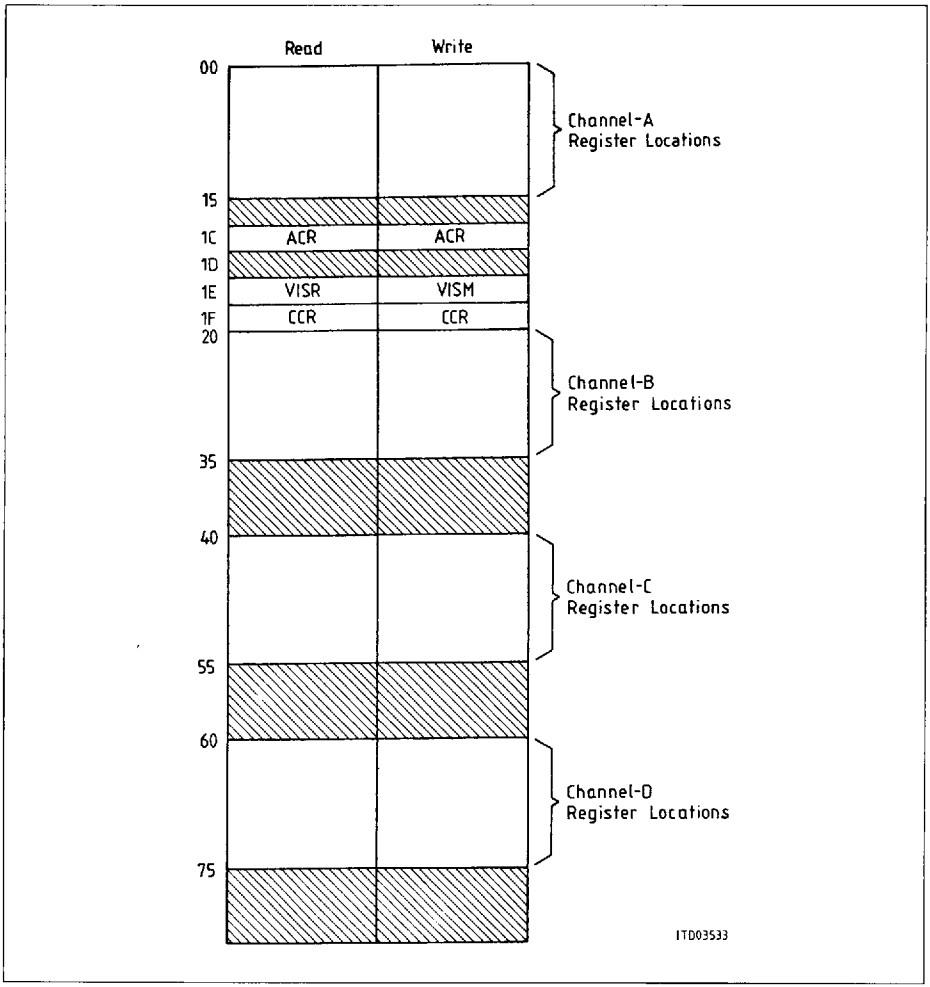


Figure 21
IDEC Register Map for Non-Multiplexed Address Bus

4.2 Register Description

Common Registers

Common Configuration Register (CCR) **Address: 37/3EH (1FH)** **Read/Write**

Value after reset: 000n0000B

7 0

MDS1	MDS0	VIS	n	CDEN	BNS	CRS	ODS

MDS1,0 Mode Select

MDS1	MDS0	Description	
0	0	Single connection	TS mode
0	1	Quad connection	common control mode
1	0	Single connection	IOM mode
1	1	Quad connection	TS mode

VIS Vectored Interrupt Selection

0 IOM channel 0 to 3 (IOM mode), P data bus bits 0 to 3 for VISR.

1 IOM channel 4 to 7 (IOM mode), P data bus bits 4 to 7 for VISR.

CDEN Change Detection Enable.

BNS Bit Number Select.

0 PCM frame is at most 256 bits long.

1 PCM frame is between 257 and 512 bits long.

CRS Clock Rate Selection.

0 DCL clock rate is equal to the data rate.

1 DCL clock rate is equal to twice the data rate.

ODS Output Driver Selection.

0 Tristate.

1 Open Drain.

The ODS bit selects the driver type simultaneously on all data outputs (and control output SD2X in master mode). However, in the single connection IOM mode SD0X is open-drain independent of the value of ODS.

Address Compare Register (ACR) **Address: 34/3DH (1CH)** **Read/Write**

Value after reset: 00H

7							0
AC3	AC2	AC1	AC0	SCM	SCG	SCS	SCP

AC0-3 Address Compare for channel A-D on (1) or off (0). The first byte following the opening flag of a receive frame will be compared against reference values if ACi = 1 and the frame is accepted or rejected on the basis of the comparison. If ACi = 0, all valid HDLC frames in that channel are stored.

SCM SAPI Compare Mode
1: Accept HDLC frames for which the first address byte matches selected SAPI values.
0: Reject HDLC frames for which the first address byte matches selected SAPI values.

SCG SAPI Compare Group
1: The first byte of a received HDLC frame is compared with "Group SAPI" SAPG (63_D).
0: The first byte of a received HDLC frame is not compared with SAPG.

SCS SAPI Compare Signaling
1: The first byte of a received HDLC frame is compared with "Signaling SAPI" SAPS (0_D).
0: The first byte of a received HDLC frame is not compared with SAPS.

SCP SAPI Compare Packet
1: The first byte of a received HDLC frame is compared with "Packet SAPI" SAPP (16_D).
0: The first byte of a received HDLC frame is not compared with SAPP.

The HDLC address compare logic is summarized in the table below.

SCM	SCG	SCS	SGP	Effect	
0	0	0	0	Accept all frames	
	0	0	1	Reject frames with	SAPP (16_D)
	0	1	0		SAPS (0_D)
	0	1	1		SAPS (0_D) and SAPP (16_D)
	1	0	0		SAPG (63_D)
	1	0	1		SAPG (63_D) and SAPP (16_D)
	1	1	0		SAPG (63_D) and SAPS (0_D)
	1	1	1		SAPG (63_D) and SAPS (0_D) and SAPP (16_D)
1	0	0	0	Reject all frames	
	0	0	1	Accept frames with	SAPP (16_D)
	0	1	0		SAPS (0_D)
	0	1	1		SAPS (0_D) and SAPP (16_D)
	1	0	0		SAPG (63_D)
	1	0	1		SAPG (63_D) and SAPP (16_D)
	1	1	0		SAPG (63_D) and SAPS (0_D)
	1	1	1		SAPG (63_D) and SAPS (0_D) and SAPP (16_D)

Vectored Interrupt Status Register (VISR) **Address: 36/3FH (1EH)** **Read**

Value after reset: xxxx0000B

7							0
X	X	X	X	IC3	IC2	IC1	IC0

or

7							0
IC3	IC2	IC1	IC0	X	X	X	X

IC0-3 Interrupt from Channel A-D

When VISR is read, these four bits are placed on the µP data bus with an offset determined by bit VIS (register CCR). Other bit positions on the bus remain in high impedance.

Mask for Vectored Interrupt Status Register (VISM) **Address: 36/3FH (1 EH)** **Write**

Value after reset: nnnn0000B

7							0
n	n	n	n	MIC3	MIC2	MIC1	MIC0

MIC0-3 Mask for Interrupt from Channel A-D.

The mask bits are active high.

A masked interrupt is not visible when VISR is read. Instead, it remains internally stored (pending). Any pending interrupt will be generated and the corresponding IC0-3 bit will be set when the mask bit is reset to zero.

You are recommended to set bits 7-4 to 1 during write accesses.

Individual Channel Registers

FIFOs

RFIFO (read), XFIFO (write) **Address: Base + 00 to 1 FH (Base + 00 to 0FH)**

The FIFO's have an identical address range. All the 32 addresses give access to the 'current' FIFO location.

Note on RFIFO The RFBC register bits 0 to 4 indicate the number of bytes currently accessible to the microcontroller in the visible 32-byte RFIFO pool. If more bytes are read, the data read after "RFBC" accesses is the "old" data loaded in that part of the RFIFO previous to the current data. For more than 32 accesses, the RFIFO will be read cyclically (modulo 32). This will not disturb the next received frame.

Note on XFIFO If more than 32 bytes are written to the XFIFO (without a transmit command), an XDOV interrupt is generated. The byte that was entered first (first byte to be sent) will be continuously overwritten by the extra write operations.

When the closing flag of a receive frame is detected, a status byte is appended to the data in the RFIFO.

This byte has the following format:

7							0
RBC	RDO	CRC	RAB	0	0	0	0

RBC: Receive Byte Count
The length of the received frame (excluding flags and Frame Check Sequence FCS) is N x 8 bits if RBC = 1 (N ∈ {1,2,3,...}). The length is not a multiple of 8 bits if RBC = 0.

RDO: Receive Data Overflow
If RDO = 1, part of the frame has been lost because the receive FIFO was full.

CRC: CRC Check
The received FCS bytes were correct if CRC = 1.

RAB: Receive Abort
RAB = 1 implies that the received frame was aborted.

A status byte equal to A0H indicates a correctly received frame.

Status / Command Registers

Interrupt Status Register (ISTA) **Address: Base + 20/29H (Base + 10H)** **Read**

Value after reset: 00H

7							0
RME	RPF	RFO	XPR	XDU	n	CD	n

RME Receive Message End.
One complete frame of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte. The number of bytes stored is given by RFBC bits 0-4.

RPF Receive Pool Full.
32 bytes of a frame have arrived in the receive FIFO. The frame is not yet completely received.

RFO Receive Frame Overflow.
At least one complete frame was lost because no storage space was available in the RFIFO.

XPR Transmit Pool Ready.
One data block may be entered into the XFIFO.

XDU Transmit Data Underrun.
Transmitted frame was terminated with an abort sequence because
either 1) no data was available for transmission in XFIFO and no XME command was issued,
or 2) a collision has occurred after at least one block of data has been completely transmitted, and thus an automatic retransmission cannot be attempted.

CD Change detection interrupt. A new value has been entered into the CIR register.

Note:

It is not possible to transmit frames when an XDU interrupt remains unacknowledged.

Mask for Interrupt Status Register (ISM) **Address: Base + 20/29H (Base + 10H)** **Write**

Value after reset: 00H

7							0
RME	RPF	RFO	XPR	XDU	n	CD	n

Each interrupt source in ISTA register can be selectively masked by setting to "1" the corresponding bit in ISM. Masked interrupts are not indicated when ISTA is read. Instead, they remain internally stored and pending. An interrupt is generated after the mask is reset to zero.

Status Register (STAR) **Address: Base + 21 /28H (Base + 11H)** **Read**

Value after reset: 50H

7							0
XDOV	XFW	BSY	RNA	VN3	VN2	VN1	VN0

XDOV Transmit Data Overflow.
More than 32 bytes have been written into the XFIFO.

XFW Transmit FIFO Write Enable.
Data can be entered into the XFIFO.

BSY Busy state on the receive line.
A "0" in this bit position indicates an "idle" state on the input data line (15 or more consecutive ones).

RNA Receive line Not Active.
Indicates whether flags/frames are being received on the line (0) or not (1). RNA takes on the value "1" after seven consecutive ones are received on the line.

VN3-0 Version Number of chip
0... A1 version
1... A2 version
2... 1.3 version

Command Register (CMDR) **Address: Base + 21/28H (Base + 11H)** **Write**

Value after reset: 00H

7							0
RMC	RRES	RMD	X	XHF	FHF	XME	XRES

RMC Receive Message Complete.
Reaction to RPF or RME internupt. The receive FIFO pool currently accessible by the microcontroller is released for a subsequent frame (or 32-byte block of data).

RRES Receiver Reset.
The HDLC receiver is reset, the receive FIFO is cleared of any data.

RMD Receive Message Delete.
Reaction to RPF or RME interrupt. The entire frame is to be ignored by the receiver. The part of the frame already stored is discarded.

XHF Transmit HDLC Frame.
Transmission of an HDLC frame (or of a block thereof) is initiated.

FHF Force HDLC Frame.
Used in the master collision mode (CMS1,0 = 11). When this bit is set and a Transmit HDLC Frame (XHF) command is issued, the controller aborts the frame from CDR (if any) by sending seven 1's on SD0X and then starts transmission. SD2X is set "low" to indicate that no data will be accepted on CDR input data line.

XME Transmit Message End.
Indicates that the current transmit frame is to be closed with CRC and flag.

XRES Transmitter Reset.
The HDLC transmitter is reset, XFIFO is cleared of any data and the HDLC frame currently being transmitted (if any) is aborted.

Mode Register (MODE) **Address: Base + 22/2BH (Base + 12H)** **Read/Write**

Value after reset: 00H

7							0
TLP	CMS1	CMS0	ITF	RAC	CAC	CCS1	CCS0

TLP Test Loop
Input and output of HDLC channel are connected together when TLP = 1. The test loop is either transparent (if MDS1,0 = 01, 10) or not (if MDS1,0 = 00, 11).

CMS1,0 Collision Mode Select.

CMS1	CMS0	Description
0	0	Unconditional transmission
0	1	Slave mode
1	0	Multi-master mode
1	1	Master mode

ITF Interframe Time Fill
Idle (ITF = 0) or flags (ITF = 1) are used as interframe time fill.

RAC Receiver Active.
Receiver is activated (1) or deactivated (0).

CAC Channel Active.
A channel is completely disabled (receiver and transmitter are inactive, transmit line is high impedance, no $\overline{TSC}$ is output) as long as CAC is "0".

CCS1,0 Channel Capacity Select.
These bits select the number of bits in the time slot where data are received and transmitted. They have a significance only when MDS1,0 = 00 or 11 (Single connection TS mode and Quad connection TS mode).

The bit rates given below assume a channel repetition rate of 8 kHz.

CCS1	CCS0	Time - Slot Width	Channel Data Rate
0	0	2 bits	16 kbit/s
0	1	1 bit	8 kbit/s
1	0	8 bits	64 kbit/s
1	1	7 bits	56 kbit/s

Command/Indicate Channel Receive Channel 0 - 3 (CIR0 - 3) (read)

Address: 23,2A + offset (multiplexed), 13 + offset (demux)

Reset value: nnnn1111 B

bit 7							bit 0
n	n	n	n	CI3	CI2	CI1	CI0

bit7: Not used.

bit6: Not used.

bit5: Not used.

bit4: Not used.

CI3-0: Received C/I code, will be updated in each frame.
CI3 is the bit received first.

Command/Indicate Channel Receive Channel 0 - 3 (CIX0 - 3) (write)

Address: 23,2A + offset (multiplexed), 13 + offset (demux)

Reset value: nnnn1111 B

bit 7							bit 0
n	n	n	n	CI3	CI2	CI1	CI0

bit7: Not used.

bit6: Not used.

bit5: Not used.

bit4: Not used.

CI3-0: Received C/I code, will be updated in each frame.
CI3 is the bit received first.

Receive Frame Byte Counter (RFBC) **Address: Base + 25/2CH (Base + 15H)** **Read**

Value after reset: 00H

7							0
RDC7	RDC6	RDC5	RDC4	RDC3	RDC2	RDC1	RDC0

RDC7-0 Receive Data Count

Total number of bytes of received frame, including the status byte. The contents of the register are valid after an RME interrupt. RDC4-0 indicate the length of the data block currently available in the receive FIFO. RDC7-5 count the number of full 32-byte blocks of a frame which have already been received. If the frame length exceeds 223 bytes, RDC7-5 hold the value "111", only RDC4-0 continue to count modulo 32.

Time-Slot Register (TSR) **Address: Base + 25/2CH (Base + 15H)** **Write**

Value after reset: 00H

7							0
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0

TS7-0 Time-Slot Select

Determine the particular time slot where the HDLC controller is to receive and transmit. This register has a significance only when MDS1,0 = 00,10 or 11 (single connection modes and quad connection TS mode).

The register gives the position of a time slot (either 1, 2, 7 or 8 bits wide, cf. CCS1,0) in two-bit increments (two-bit resolution).

The position of the time slot is relative to a frame sync signal that marks the beginning of a PCM frame.

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	C
Storage temperature	T_{stg}	– 65 to 125	C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V

DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V 5 %, V_{SS} = 0 V

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
L-input voltage		V_{IL}	– 0.4	0.8	V	
H-input voltage		V_{IH}	2.0	V_{CC} + 0.4	V	
L-output voltage		V_{OL}		0.45	V	I_{OL} = 7 mA (SD0X...SD3X) I_{OL} = 2 mA (all other pins)
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V	I_{OH} = – 400 µA I_{OH} = – 100 µA
Power supply current	operational	I_{CC}		10	mA	V_{DD} = 5 V, DCL = 4096 kHz Inputs at 0 V/V_{DD}, No output loads
	power down			1	mA	
Input leakage current Output leakage current		I_{LI} I_{LO}		+ 10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

T_A = 25 °C; V_{DD} = 5 V 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input capacitance	C_{IN}	5	10	pF	
I/O capacitance	C_{IO}	10	20	pF	

AC Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V 5 %

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".

The AC testing input/output waveforms are shown below.

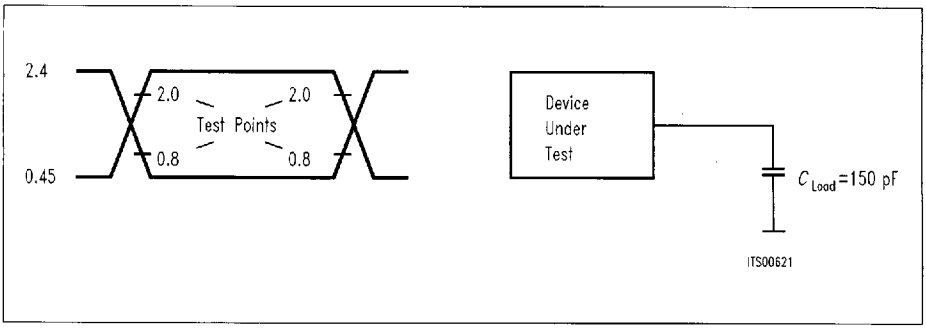


Figure 22
Input/Output Waveforms for AC Tests

Microcontroller Interface TimingmP Read Cycle

Siemens/Intel Bus ModemP Read CyclemP Read CyclemP Read Cycle

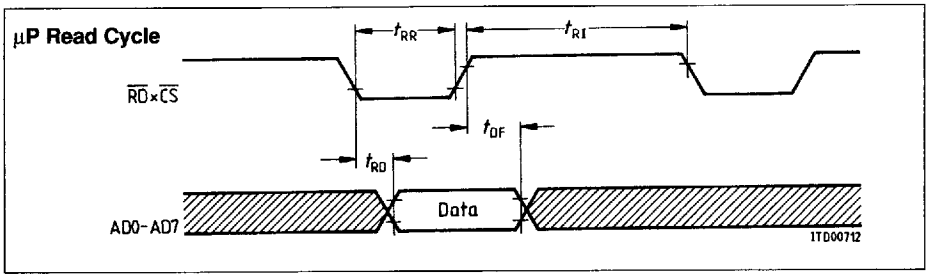


Figure 23

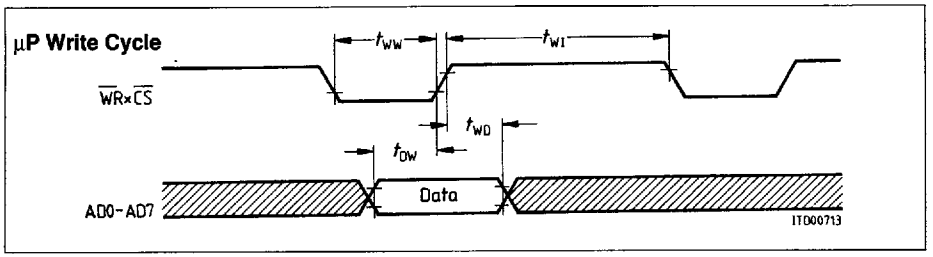


Figure 24

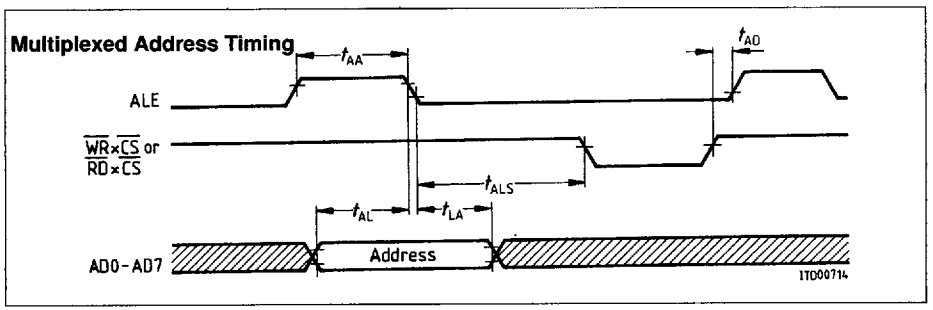


Figure 25

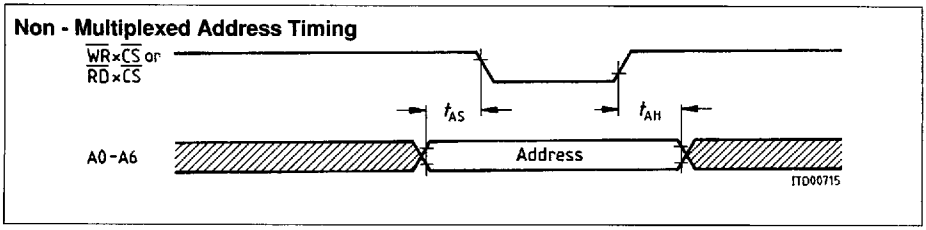


Figure 26

Motorola Bus Mode

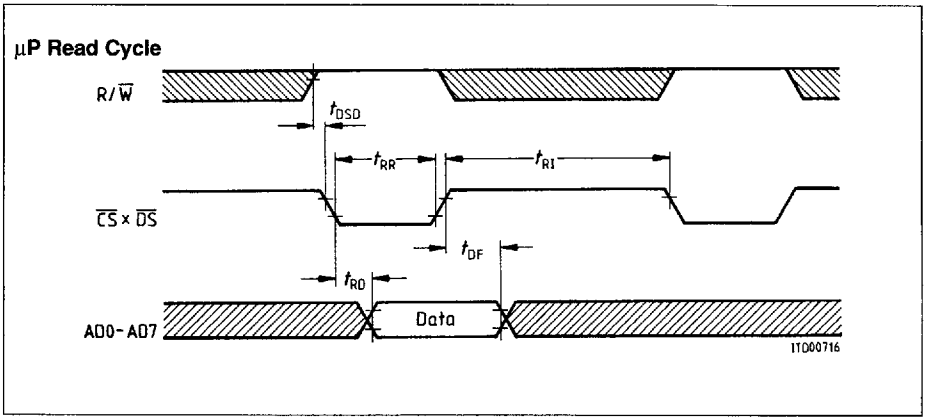


Figure 27

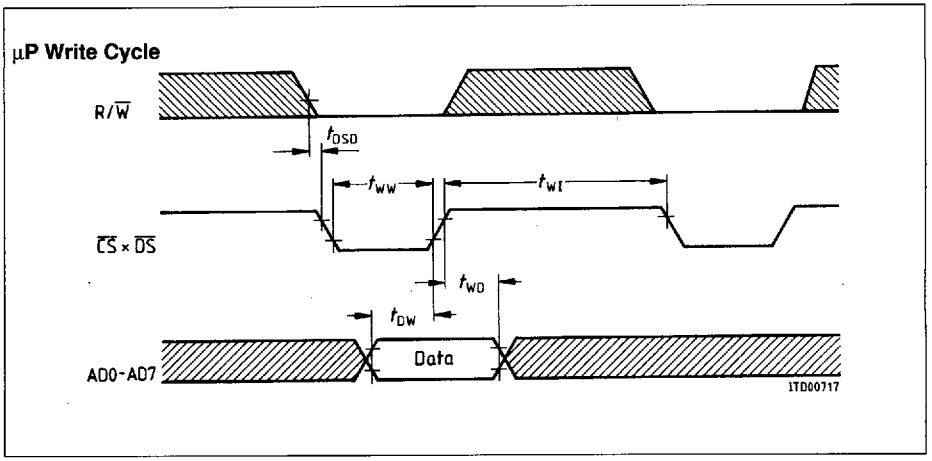


Figure 28

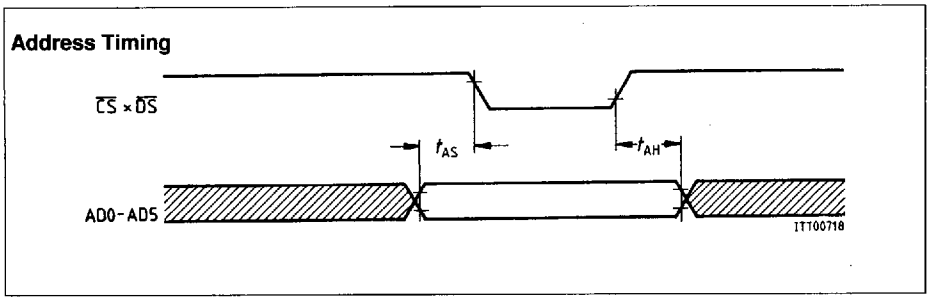


Figure 29

Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	20		ns
Address hold time from ALE	t_{LA}	35		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	35		ns
Address setup time	t_{AS}	10		ns
Address hold time	t_{AH}	25		ns
ALE guard time	t_{AD}	15		ns
$\overline{RD}$ Delay after $\overline{WR}$ setup	t_{DSD}	0		ns
RD pulse width	t_{RR}	120		ns
Data output delay from $\overline{RD}$	t_{RD}		120	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	75		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$ x $\overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR}$ x $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

Serial Interface Timing

DCL Characteristics

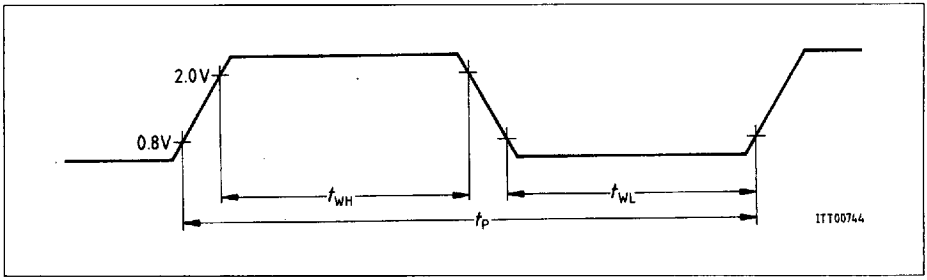


Figure 30
Definition of DCL Period and Width

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	typ.		
DCL period	t_P	230 160		ns ns	single clock rate double clock rate
DCL high	t_{WH}	90 50		ns ns	single clock rate double clock rate
DCL low	t_{WL}	70		ns	

Input/Output Characteristics

FSC in Single Connection Modes and Quad Connection in TS Mode

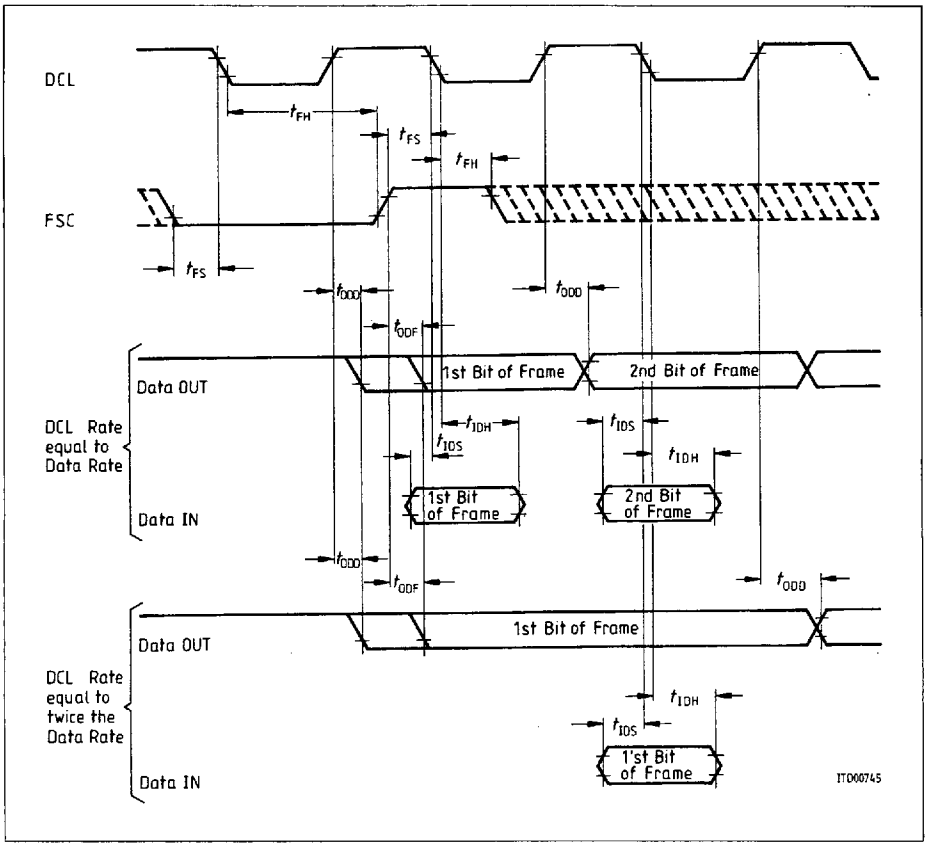


Figure 31
FSC Timing Characteristics

FSC Timing Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC set-up time	t_{FS}	60		ns
FSC setup time*	t_{FS2}	110		
FSC hold time	t_{FH}	30		ns
Output data delay from DCL	t_{ODD}		60	ns
Input data set-up	t_{IDS}	25		ns
Input data hold	t_{IDH}	20		ns
Output data delay from FSC*	t_{ODF}		160	ns

***Note:**

This delay is applicable in two cases when the first time slot has been programmed:

1) When FSC appears for the first time, e.g. at system power-up.

2) When the number of bits in the PCM frame is not equal to either 256 or 512.

FSC in Quad Connection Common Control Mode

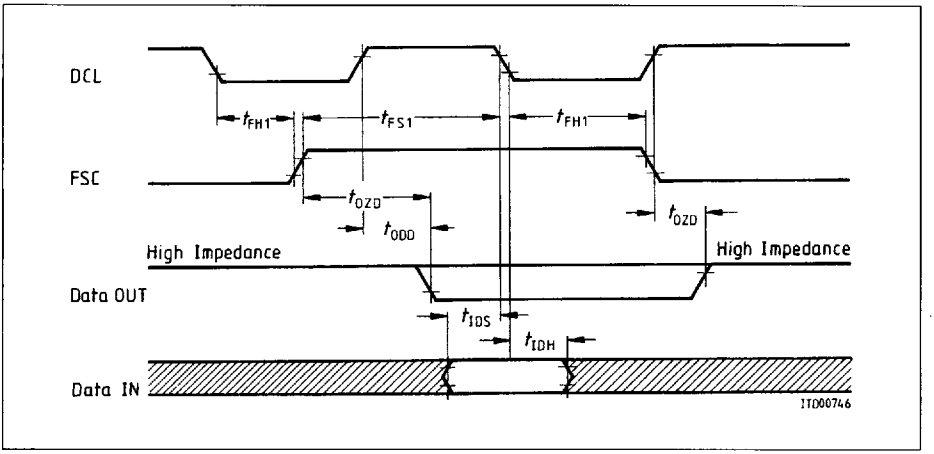


Figure 32
FSC Characteristics (strobe)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC set-up time	t_{FS1}	60		ns
FSC hold time	t_{FH1}	30		ns
Output data from high impedance to active	t_{OZD}		80	ns
Output data from active to high impedance	t_{ODZ}		40	ns
Output data delay from DCL	t_{ODD}		60	ns
Input data set up	t_{IDS}	25		ns
Input data hold	t_{IDH}	20		ns

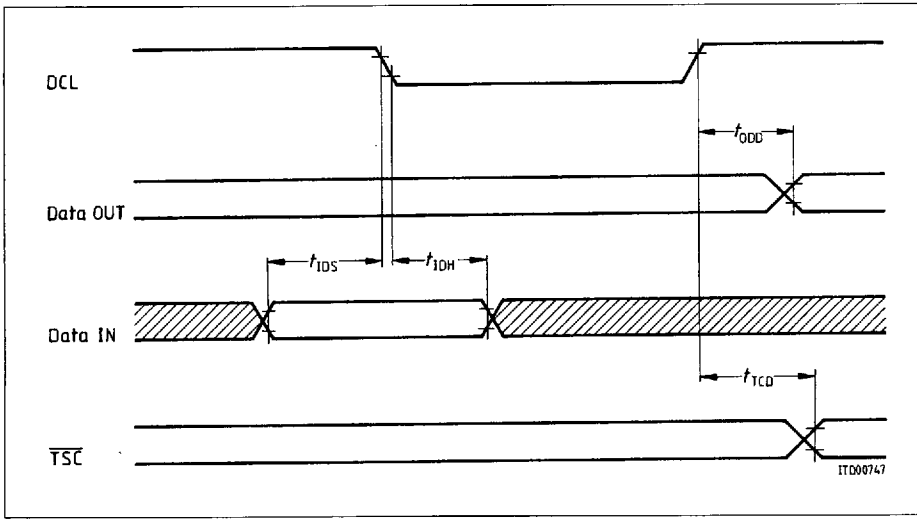


Figure 33
Data I/O Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Output data delay from DCL	t_{ODD}		60	ns
Input data set-up	t_{IDS}	25		ns
Input data hold	t_{IDH}	20		ns
$\overline{TSC}$ delay from DCL	t_{TCD}		60	ns

Data OUT: SD0X in single connection modes
SD0X, SD1X, SD2X, SD3X in quad connection modes
SD1X, SD2X in master mode

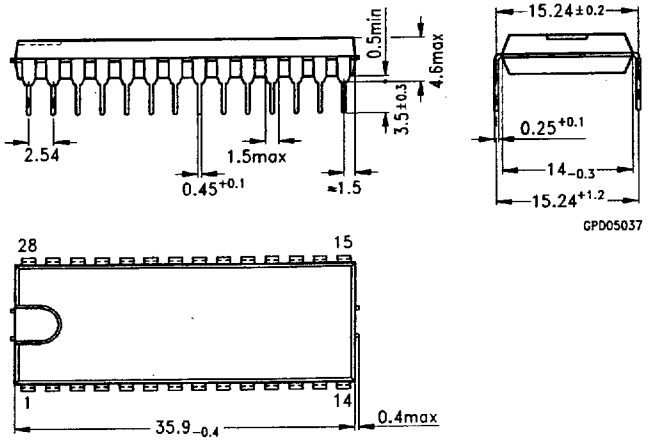
Data IN: SD0R in single connection mode
SD0R, SD1X, SD2R, SD3R in quad connection modes
CDR in slave, multi-master and master modes

RES Characteristics

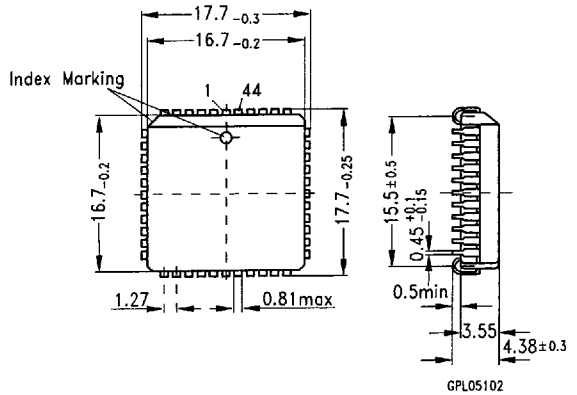
Parameter	Symbol	Limit Values		Unit
		min.	max.	
RES high	t_{RWL}	16 x t_P		ns

7 Package Outlines

Plastic Dual-In-Line Package, P-DIP-28



Plastic-Leaded Chip Carrier, P-LCC-44 (SMD)



SMD = Surface Mounted Device

Dimensions in mm