PA09 • PA09A

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FEATURES

- POWER MOS TECHNOLOGY — 2A peak rating
- HIGH GAIN BANDWIDTH PRODUCT — 150MHz
- VERY FAST SLEW RATE — 400V/µs
- PROTECTED OUTPUT STAGE — Thermal shutoff
- EXCELLENT LINEARITY — Class A/B output
- WIDE SUPPLY RANGE — ±12V to ±40V
- LOW BIAS CURRENT, LOW NOISE — FET input

APPLICATIONS

- VIDEO DISTRIBUTION AND AND AMPLIFICATION
- HIGH SPEED DEFLECTION CIRCUITS
- POWER TRANSDUCERS TO 5MHz
- COAXIAL LINE DRIVERS
- POWER LED OR LASER DIODE EXCITATION

DESCRIPTION

The PA09 is a high voltage, high output current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolithic FET input transistor which is cascoded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA09 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from second breakdown is assured by a complementary Power MOS output stage. For optimum linearity, especially at low levels, the Power MOS transistors are biased in the class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit protects the amplifier against overloading. Transient inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

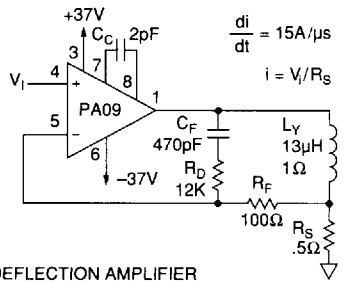
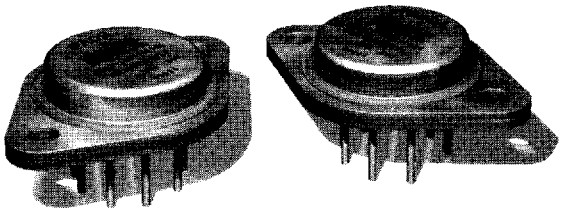


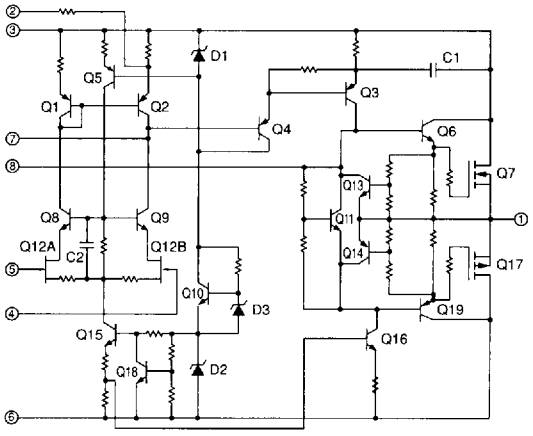
FIGURE 1. PA09 AS DEFLECTION AMPLIFIER



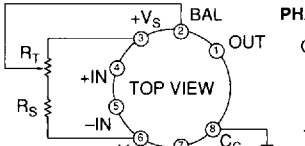
DEFLECTION AMPLIFIER (Figure 1)

The deflection amplifier circuit of Figure 1 achieves arbitrary beam positioning for a fast heads-up display. Maximum transition times are 4µs while delivering 2A pk currents to the 13mH coil. The key to this circuit is the sense resistor (R_S) which converts yoke current to voltage for op amp feedback. This negative feedback forces the coil current to stay exactly proportional to the control voltage. The network consisting of R_D, R_F and C_F serves to shift from a current feedback via R_S to a direct voltage feedback at high frequencies. This removes the extra phase shift caused by the inductor thus preventing oscillation. See Application Note 5 for details of this and other precision magnetic deflection circuits.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C	R_C
1	100pF	200Ω
10	15pF	0Ω
100	5pF	0Ω
1000	none	none

$R_S = (|+V_S| + |-V_S|)\ R_T/1.6$

NOTE: Input offset voltage trim optional. R_T = 10KΩ MAX

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	78W
INPUT VOLTAGE, differential	40V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

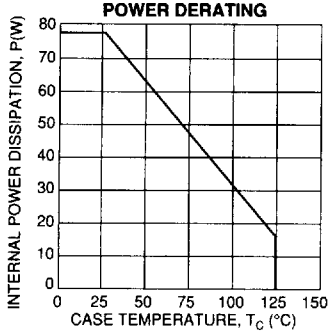
PARAMETER	TEST CONDITIONS[2]	PA09 MIN	PA09 TYP	PA09 MAX	PA09A MIN	PA09A TYP	PA09A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		.5	± 3		± .25	± .5	mV
OFFSET VOLTAGE, vs. temperature	T_C = 25 to +85°C		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25 to +85°C		20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		5	100		3	20	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	T_C = –25 to +85°C	$\pm V_S$–10	$\pm V_S$–8		*	*		V
COMMON MODE REJECTION, DC	T_C = –25 to +85°C, V_{CM} = ± 20V		104			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 1kΩ		90			*		dB
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 15Ω	80	88		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, R_L = 15Ω, C_C = 5pF		150			*		MHz
POWER BANDWIDTH, gain of 100 comp	T_C = 25°C, R_L = 15Ω, C_C = 5pF		1.2			*		MHz
POWER BANDWIDTH, unity gain comp	T_C = 25°C, R_L = 15Ω, C_C = 100pF		.75			*		MHz
OUTPUT								
VOLTAGE SWING[3]	T_C = –25 to +85°C, I_O = 2A	$\pm V_S$ –8	$\pm V_S$ –7		*	*		V
CURRENT, PEAK	T_C = 25°C		4.5			*		A
SETTLING TIME to .1%	T_C = 25°C, 2V step		.3			*		µs
SETTLING TIME to .01%	T_C = 25°C, 2V step		1.2			*		µs
SLEW RATE, gain of 100 comp	T_C = 25°C, C_C = 5pF		400			*		V/µs
SLEW RATE, unity gain comp	T_C = 25°C, C_C = 100pF		75			*		V/µs
POWER SUPPLY								
VOLTAGE	T_C = –25 to +85°C	± 12	± 35	± 40	*	*	*	V
CURRENT, quiescent	T_C = 25°C		70	85		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[4]	T_C = –25 to +85°C, F > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	T_C = –25 to +85°C, F < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	T_C = –25 to +85°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+ 85	*	*	*	°C

NOTES: * The specification of PA09A is identical to the specification for PA09 in applicable column to the left.

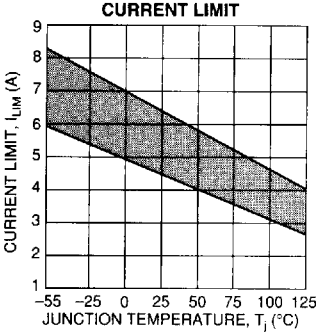
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±35V unless otherwise specified as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

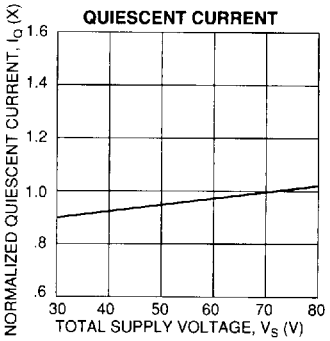
POWER DERATING



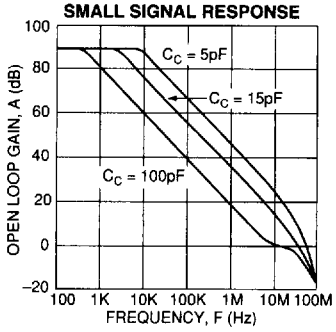
CURRENT LIMIT



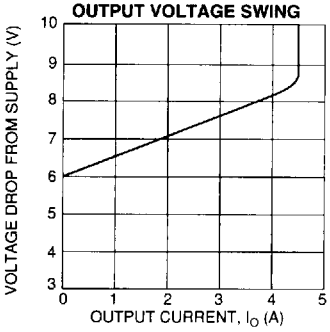
QUIESCENT CURRENT



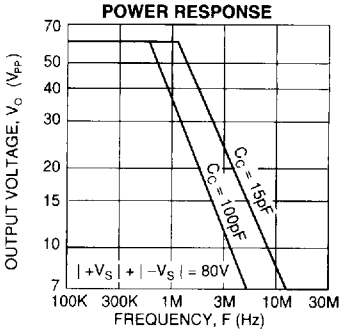
SMALL SIGNAL RESPONSE



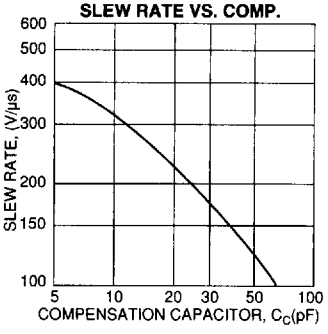
OUTPUT VOLTAGE SWING



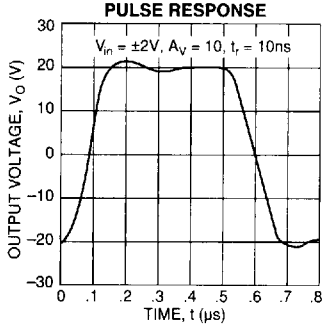
POWER RESPONSE



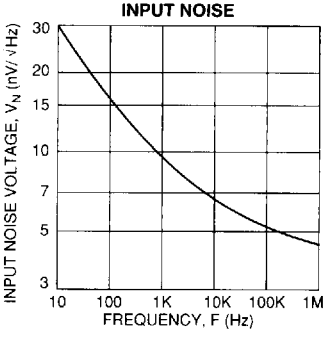
SLEW RATE VS. COMP.



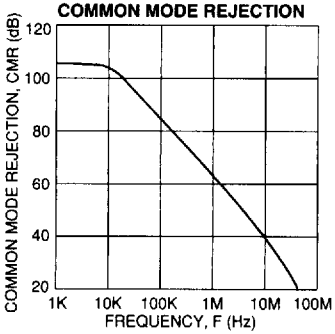
PULSE RESPONSE



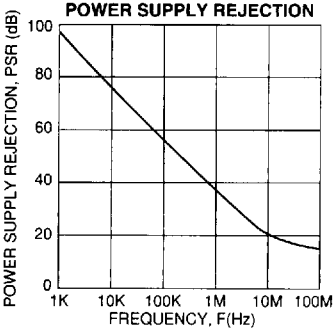
INPUT NOISE



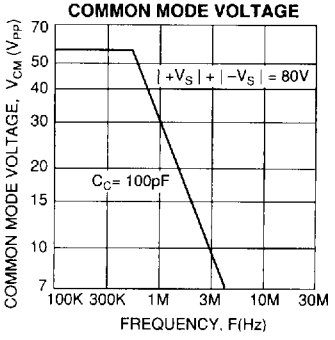
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SUPPLY VOLTAGE

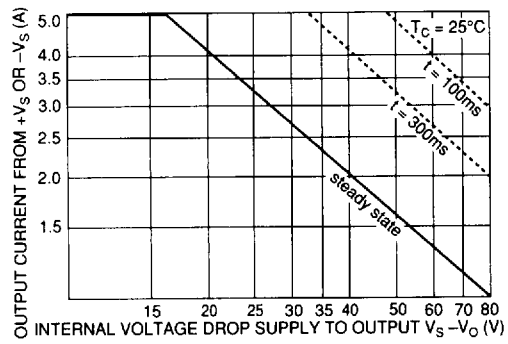
The specified voltage ($\pm V_S$) applies for a dual (±) supply having equal voltages. A nonsymmetrical (ie. +70/–10V) or a single supply (ie. 80V) may be used as long as the total voltage between the $+V_S$ and $-V_S$ rails does not exceed the sum of the voltages of the specified dual supply.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

SAFE OPERATING AREA CURVES



The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Capacitive and inductive loads up to the following maximums are safe:

±VS	CAPACITIVE LOAD	INDUCTIVE LOAD
40V	.1µF	11mH
30V	500µF	24mH
20V	2500µF	75mH
15V	∞	100mH

2. Short circuits to ground are safe with dual supplies up to ±20V.
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

BYPASSING OF SUPPLIES

Each supply rail must be bypassed to common with a tantalum capacitor of at least 47µF in parallel with a .47µF ceramic capacitor directly connected from the power supply pins to the ground plane.

OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductance, raising the interconnection impedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

GROUNDING

Single point grounding of the input resistors and the input signal to a common ground plane will prevent undesired current feedback, which can cause large errors and/or instabilities.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier, If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

STABILITY

Due to its large bandwidth the PA09 is more likely to oscillate than lower bandwidth Power Operational Amplifiers. To prevent oscillations a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections on the first page of this data sheet and interpolate if necessary. The phase margin can be increased by using a larger capacitor and a smaller resistor than the slew rate optimized values listed in the table.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or bypassing of the feedback resistor.
3. Connect the case to a local AC ground potential.

CURRENT LIMIT

Internal current limiting is provided in the PA09. Note the current limit curve given under typical performance graphs is based on junction temperature. If the amplifier is operated at cold junction temperatures, current limit could be as high as 8 amps. This is above the maximum allowed current on the SOA curve of 5 amps. Systems using this part must be designed to keep the maximum output current to less than 5 amps under all conditions. The internal current limit only provides this protection for junction temperatures of 80°C and above.

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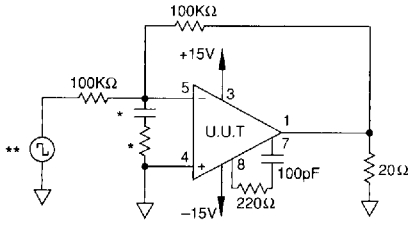
TABLE 4 GROUP A INSPECTION

PA09M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±35V	V_{IN} = 0, A_V = 100		85	mA
1	Input Offset Voltage	V_{OS}	25°C	±35V	V_{IN} = 0, A_V = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±12V	V_{IN} = 0, A_V = 100		5.3	mV
1	Input Offset Voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		3.5	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±35V	V_{IN} = 0		100	pA
1	Inout Bias Current, –IN	$-I_B$	25°C	±35V	V_{IN} = 0		100	pA
1	Input Offset Current	I_{OS}	25°C	±35V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±35V	V_{IN} = 0, A_V = 100		165	mA
3	Input Offset Voltage	V_{OS}	–55°C	±35V	V_{IN} = 0, A_V = 100		5.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±12V	V_{IN} = 0, A_V = 100		7.7	mV
3	Input Offset Voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		5.9	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±35V	V_{IN} = 0		100	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±35V	V_{IN} = 0		100	pA
3	Input Offset Current	I_{OS}	–55°C	±35V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±35V	V_{IN} = 0, A_V = 100		140	mA
2	Input Offset Voltage	V_{OS}	125°C	±35V	V_{IN} = 0, A_V = 100		6	mV
2	Input Offset Voltage	V_{OS}	125°C	±12V	V_{IN} = 0, A_V = 100		8.3	mV
2	Input Offset Voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		6.5	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±35V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 3A	V_O	25°C	±21.3V	R_L = 3.75Ω	11.3		V
4	Output Voltage, I_O = 66mA	V_O	25°C	±40V	R_L = 500Ω	33		V
4	Output Voltage, I_O = 2A	V_O	25°C	± 38V	R_L = 15Ω	30		V
4	Current Limits	I_{CL}	25°C	±32.2V	R_L = 3.75Ω	3.4	6	A
4	Stability/Noise	E_N	25°C	±35V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
4	Slew Rate	SR	25°C	±35V	R_L = 500Ω	25	500	V/µs
4	Open Loop Gain	A_{OL}	25°C	±35V	R_L = 500Ω, F = 10Hz	80		dB
4	Common Mode Rejection	CMR	25°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±22.5V	64		dB
6	Output Voltage, I_O = 3A	V_O	–55°C	±21.3V	R_L = 3.75Ω	11.3		V
6	Output Voltage, I_O = 66mA	V_O	–55°C	±40V	R_L = 500Ω	33		V
6	Output Voltage, I_O = 2A	V_O	–55°C	±38V	R_L = 15Ω	30		V
6	Stability/Noise	E_N	–55°C	±35V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
6	Slew Rate	SR	–55°C	±35V	R_L = 500Ω	25	500	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±35V	R_L = 500Ω, F = 10Hz	80		dB
6	Common Mode Rejection	CMR	–55°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±22.5V	64		dB
5	Output Voltage, I_O = 66mA	V_O	125°C	±40V	R_L = 500Ω	33		V
5	Output Voltage, I_O = 1A	V_O	125°C	±23.5V	R_L = 15Ω	15		V
5	Stability/Noise	E_N	125°C	±35V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
5	Slew Rate	SR	125°C	±35V	R_L = 500Ω,	20	500	V/µs
5	Open Loop Gain	A_{OL}	125°C	±35V	R_L = 500Ω, F = 10Hz	80		dB
5	Common Mode Rejection	CMR	125°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±22.5V	64		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

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