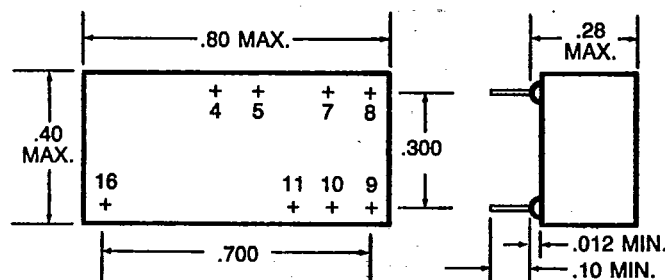
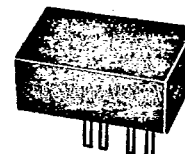


YCL

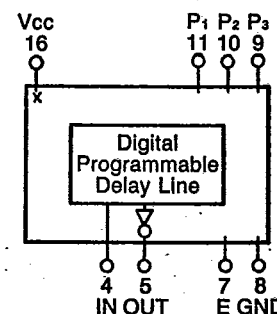
TTL DIGITAL PROGRAMMABLE DELAY LINES 16 PIN PACKAGE 3 BIT

SERIES P1

White Dot locates Pin 1



Model No.	Zero Step Delay (ns)	Maximum Delay (ns) (nom)	Delay per step (ns)
P10714	7 ± 2	14	1 ± .5
P10721		21	2 ± .5
P10728		28	3 ± .6
P10735		35	4 ± .8
P10742		42	5 ± 1
P10749		49	6 ± 1
P10756		56	7 ± 1
P10763		63	8 ± 1
P10770		70	9 ± 1
P10777		77	10 ± 1



TYPICAL TRUTH TABLE EXAMPLE:									
Model Number	Data Select Pins	P3-9	L	L	L	L	H	H	H
		P2-10	L	L	H	H	L	L	H
		P1-11	L	H	L	H	L	H	L
P10735			7	5	10	15	20	25	30

SPECIFICATIONS:

- Zero step delay is measured from the input pin #4
 - All programmable delays after step zero are referenced to step zero
 - Programmable delay tolerances: ±2ns or ±5% whichever is greater
 - Rise Time: 4ns max
 - Temp. coeff. of delay: 0°C to +70°C
 - Vol: 1.0ns + 500ppm/°C
 - Voh: .4V max
 - Vcc: 2.4V min
 - Icc: 5VDC ±0.25V
 - Minimum Pulse Width: 85mA
 - Maximum Duty Cycle: 40% of Total Delay
 - Terminals: 50%
- Electro tin plated alloy 42, .020w x .010th

TEST CONDITIONS:

- Vcc = 5.0VDC, temp. 25°C
- Enable is grounded.
- Time delay measured at the 1.5 volt level of the leading edge
- Rise time measured from .75V to 2.4 volts
- Output loaded with 15pf
- Input pulse width: 3 x max time delay
- Pulse amplitude: 3.0 volts
- Pulse spacing: 1000ns