

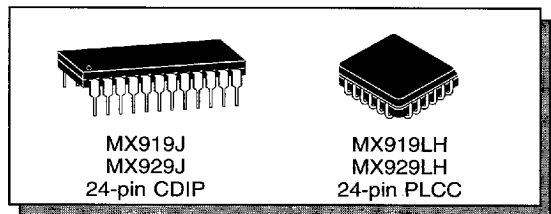
HIGH-SPEED FOUR-LEVEL FSK "PACKET DATA" MODEMS

MX919: General Purpose

MX929: RD-LAP* (ARDIS)**

Features

- MX-COM MX'D Signal CMOS
- FM Radio Packet Data Applications
 - Wireless Data Systems
 - Radio Telemetry
 - Mobile Data Links
 - Wireless LANs
 - Medical Telemetry
 - Wireless Bar-Code Readers
- 4-Level FSK - 4.8/9.6/19.2 kbps
- Low Power Requirement
- Custom Frame Capabilities (MX919)
- Automatic Protocol Handling (General Purpose & RD-LAP)
 - Symbol and Frame Sync
 - Block Formatting
 - Forward Error Correction
 - CRC Check and Generation
 - Interleaving
- PCMCIA Packaging Available***



Description

The MX919 and MX929 are half-duplex high-speed, 4-level FSK 'packet data' modems. They work with a host μ Controller to provide packet data transfer via FM radio systems.

The MX919 provides a versatile frame structure for general-purpose applications. The MX929 is designed specifically for the ARDIS RD-LAP network.

Having a low power requirement of 5.0mA at 5 volts, the MX919 and MX929 modems provide:

- Automatic handling of general purpose (MX919) and RD-LAP (MX929) frame structures, including RX symbol and frame synchronization, block formatting, CRC generation and checking, Forward Error Correction and Interleaving to reduce the processing load on the host μ Controller.
- Selectable data rates of 2400/4800/9600 symbols/s (4.8/9.6/19.2 kbps) for high-speed operation.
- 4-Level FSK (2 bits per baud) baseband

modulation enables high-speed, economical data rates in a narrow RF bandwidth.

- On-chip baseband processing and filtering.
- Pre-selectable signal acquisition and tracking permits the rapid acquisition of received signals, followed by automatic tracking of signal dc level variations.

Clock recovery PLL bandwidth and RX signal level measurement circuitry will react automatically when set.

RX and TX data and control between the host μ Controller and this microcircuit is via an 8-bit bi-directional parallel interface; input and output signals to and from the radio system are in analog form suitable for connection to the radio's discriminator and frequency modulator.

The MX919 and MX929 modems are available in 24-pin CDIP and Surface Mount packages, as well as packaging for PCMCIA applications***.

*RD-LAP is a trademark of Motorola, Inc.

**ARDIS is a service mark of ARDIS.

***Contact MX-COM for more information.

MX919 and MX929 Circuit Descriptions**Data Bus Buffers**

Eight bi-directional 3-state logic-level buffers between the modem's internal registers and the controlling μ Controller's data-bus lines.

R/W, CS and Address Lines

Control the transfer of data bytes between the μ Controller and the modem's internal registers, according to the state of the Write and Read Enable ($\overline{WR}$ and $\overline{RD}$) inputs, the Chip Select ($\overline{CS}$) input and the Register Address inputs (A_0 and A_1).

The Data Bus Buffers and Address & R/W Decode blocks provide a byte-wide parallel μ Controller interface.

Status and Data Quality Registers

8-bit registers which the μ Controller can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers

The values written by the μ Controller to these 8-bit registers control the operation of the modem.

Data Block Buffer

An 12-byte buffer used to hold RX or TX data to or from the μ Controller.

CRC Generator/Checker

A circuit which generates (transmit mode) or checks (receive mode) the Cyclic Redundancy Checksum bits which may be included in transmitted data blocks so that the receive modem can detect transmission errors.

FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, then converts the resulting binary data to 4-level symbols. In receive mode, it translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors. The 4 possible levels of a symbol are referred to in this Data Sheet as: +3, +1, -1 and -3.

Interleave/De-interleave Buffer

Interleaves data symbols within a data block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

RX Input Amp

The amplifier that allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components.

Frame Sync Detect

This circuit, which is only active in the receive mode, is used to look for the user-specified 24-symbol Frame Synchronization pattern which is transmitted to mark the start of every frame.

Root Raised Cosine (RRC) Filter

This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response.

In TX mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In RX mode this filter is used to reject HF noise and to equalize the received signal to a form suitable for extracting the 4-level symbols.

RX Symbol/Clock Extraction

These circuits, which operate only in receive mode, extract a symbol-rate clock from the received signal, and measure the received signal amplitude and its dc offset.

This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit.

Clock Oscillator and Dividers

This circuit derives the transmit symbol-rate (and the nominal receive symbol-rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or fed from an external source.

TX Output Buffer

A unity-gain amplifier used in the transmit mode to buffer the output of the RRC filter. In receive mode, the input of this buffer is normally connected to V_{BIAS} unless the RXEYE bit of the Control Register is set. When the modem is set to the powersave mode, the buffer is turned off and the TX Output pin connected to V_{BIAS} via a high value resistance.

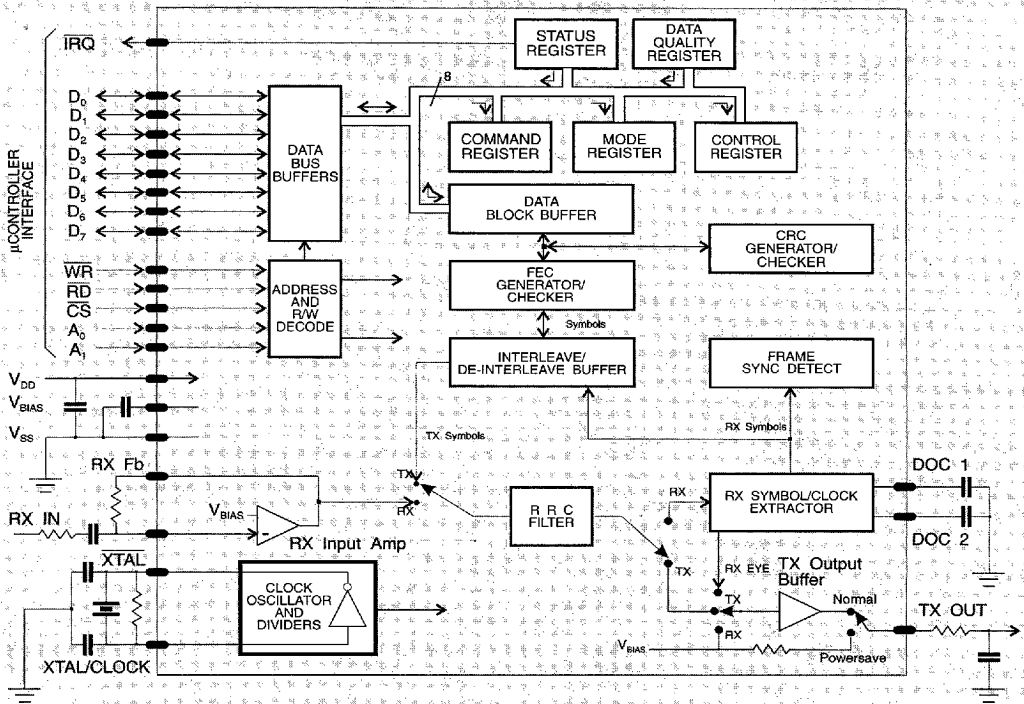


Figure 1 - MX919/MX929 Functional Block Diagram

MX919 and MX929 Pin Functions

Pin	Function
1	IRQ: A 'wire-ORable' output for connection to the controlling μ Controller's Interrupt Request input. This output has a low-impedance pull-down to V_{ss} when active, and is high-impedance when inactive.
2	D₇:
3	D₆:
4	D₅:
5	D₄: 8 bi-directional 3-state μ Controller interface data lines.
6	D₃:
7	D₂:
8	D₁:
9	D₀:
10	RD: An active-low logic level input used to control the reading of data from the modem into the controlling μ Controller.
11	WR: An active-low logic level input used to control the writing of data into the modem from the controlling μ Controller.
12	V_{ss}: The negative supply rail (ground).
13	CS: An active-low logic level input to the modem used to enable a data Read or Write operation (see Figure 26, Timing).
14	A₀: Two logic-level modem register selection inputs.
15	A₁:
16	Xtal: The output of the on-chip Xtal oscillator.
17	Xtal/Clock: The input to the on-chip Xtal oscillator. Operation of the MX919/MX929 without a suitable Xtal or clock input may cause device damage.
18	Doc 2: Connections to the internal RX signal level measurement circuitry. Capacitors as
19	Doc 1: shown in Figure 2 should be installed from each of these pins to V_{ss} .
20	TX Out: The TX signal output from the modem.
21	V_{BIAS}: The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{ss} by a capacitor mounted close to the device pins.
22	RX In: The input to the RX input amplifier.
23	RX Feedback: The output of the RX input amplifier, and the input to the (RX) Lowpass Filter.
24	V_{DD}: The positive supply. Levels and voltages within the modem are dependent upon this supply. This pin should be decoupled to V_{ss} by a capacitor mounted close to the device pins.

Installation Information

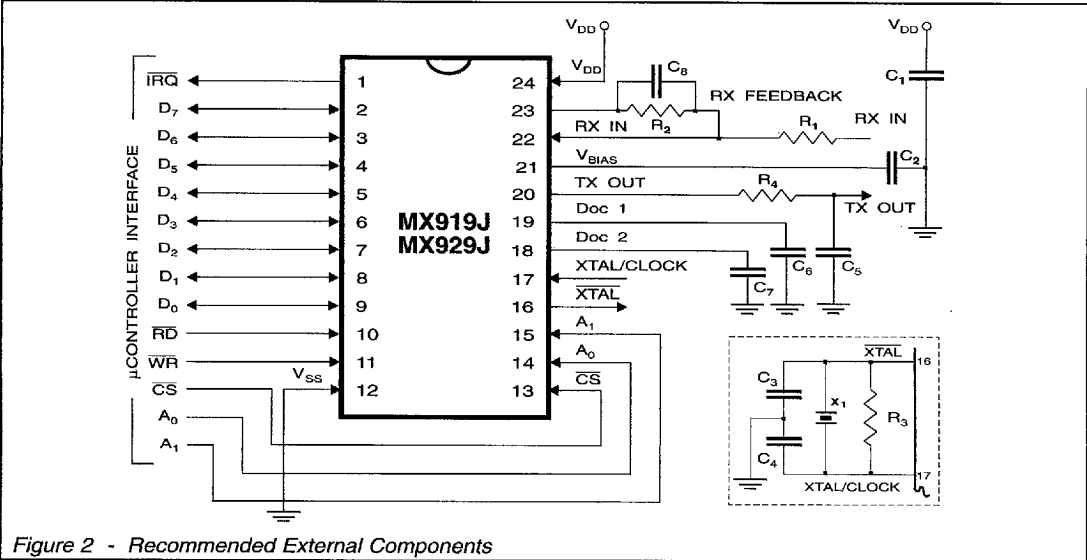


Figure 2 - Recommended External Components

Component	Value	Tolerance
R ₁	Note 1	±10%
R ₂	100kΩ	±10%
R ₃	1.0MΩ	±20%
R ₄	Note 2	
C ₁	0.1μF	±20%
C ₂	0.1μF	±20%
C ₃	Note 3	±20%
C ₄	Note 3	±20%
C ₅	Note 2	
C ₆	Note 2	±20%
C ₇	Note 4	±20%
C ₈	TBD	
X ₁	Note 3	

R₄ and C₅ should be chosen so that the product of R₄ (Ohms) and C₅ (Farads) is:

$$\frac{0.34}{\text{bit rate (bits per sec)}}$$

R₄ should be not less than 20kΩ; the value used for C₅ should take into account parasitic capacitance.

Examples	R ₄	C ₅
8000bps	100kΩ	430pF
4800bps	100kΩ	710pF

3. The values used for C₃ and C₄ are determined by the frequency of X₁.

As a guide:

$$C_3 = C_4 = 33\text{pF for } X_1 < 5.0\text{MHz.}$$

$$C_3 = C_4 = 18\text{pF for } X_1 > 5.0\text{MHz.}$$

If the on-chip Xtal oscillator is to be used, then the external components X₁, C₃, C₄, and R₃ are required as shown in Figure 2 (inset). If an external clock source is used these components are not required; the input should be connected to the Xtal/clock pin and the Xtal pin left unconnected. Table 8 provides advice on the selection of the correct Xtal value.

4. External capacitors C₆ and C₇ form part of the received signal level measuring circuit. For optimum performance the values of these components should be as shown below.

For	C ₆ and C ₇
2400 symbols/sec	0.02μF
4800 symbols/sec	0.01μF
9600 symbols/sec	0.0047μF

Installation Information...

Binary to Symbol Translation

Although the over-air signal, and hence the signals at the modem TX Out and RX In pins, consists of 4-level symbols, the raw data passing between the modems and the μ Controller is in binary form. The MX919/929 translates between binary data and the 4-level symbols in one of two ways, depending on the task being performed:

Direct

The simplest form, which converts between 2 binary bits and one symbol according to the table below.

Symbol	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

This scheme can be expanded so that an 8-bit byte translates to four symbols:

MSB					LSB			
Bits	7	6	5	4	3	2	1	0
Symbols	a		b		c		d	
	sent first				sent last			

With Forward Error Correcting (FEC)

This is more complicated, but essentially translates 3 binary bits to two 4-level symbols using an FEC coding scheme which lets the receiving modem detect and correct a large proportion of transmission errors. Full details are given later in this document

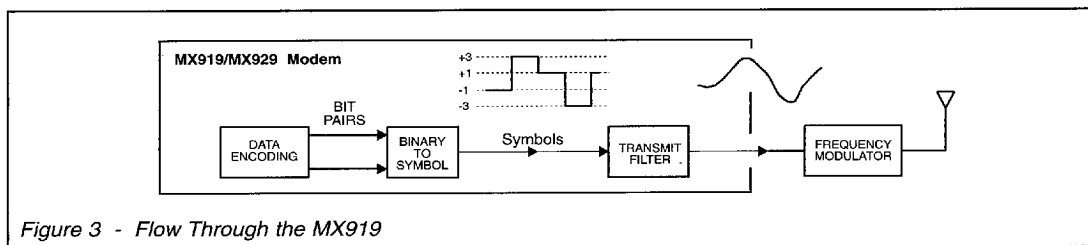


Figure 3 - Flow Through the MX919

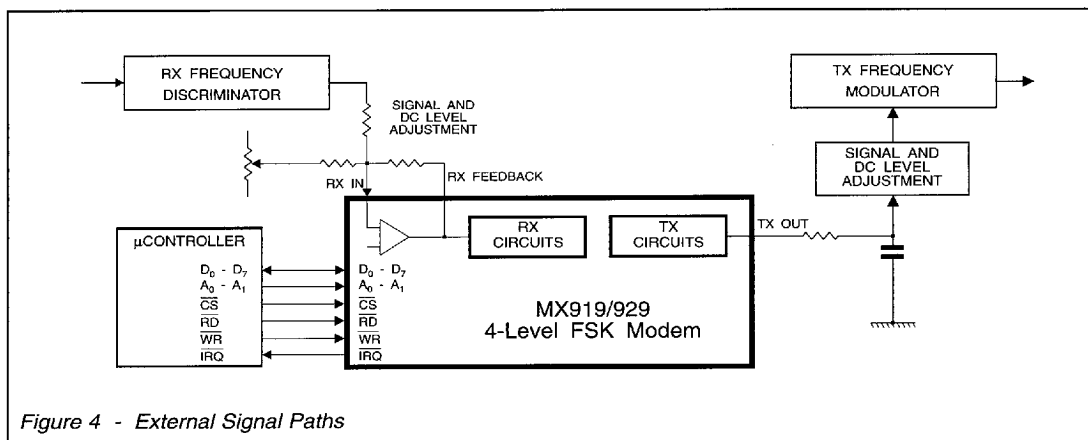


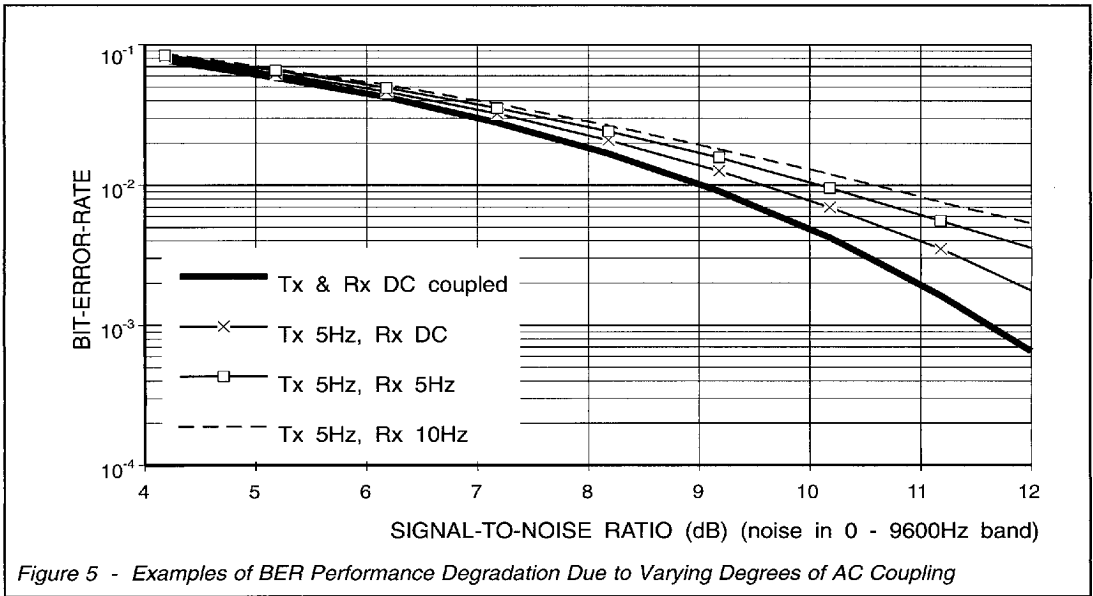
Figure 4 - External Signal Paths

Installation Information

AC Coupling

For a practical application, AC coupling from the modem's transmit output to the Frequency Modulator and from the receiver's Frequency Discriminator to the receive input of the modem may be desired. There are, however, two problems.

1) AC coupling of the signal degrades the bit-error-rate performance of the modem. Figure 5 illustrates the typical bit error rates at 4800 symbols/sec (without FEC) for differing degrees of AC coupling;

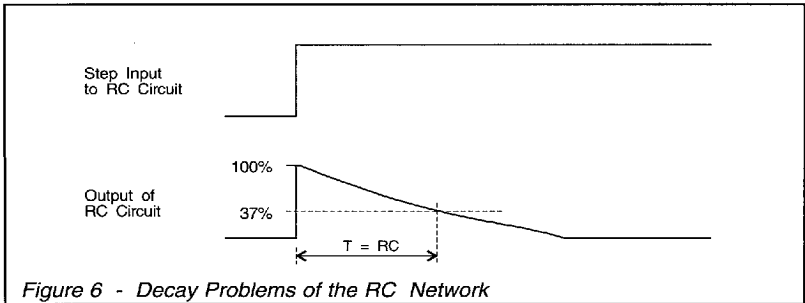


2) Any AC coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated below, the time for this voltage step to decay to 37% of its original value is:

$$RC = \frac{1}{(2\pi \times f)}$$

Where f is the 3dB cut-off frequency of the AC coupling network; RC is 32msec -or 153 symbol-times at 4800symbols/sec- for a 20Hz network.

In general, it will be best to DC couple the receive discriminator to the modem, and to ensure that any AC coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz (for 4800symbols/sec).



Radio Performance

The maximum data rate that can be transmitted over a radio channel using the MX919/929 depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- TX and RX reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec can be achieved -subject to local regulatory requirements- over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ± 2.5 kHz peak for a repetitive +3 +3 -3 -3 pattern and the maximum difference between transmitter and receiver "carrier" frequencies is less than 2400Hz.

The modulation scheme employed by these modems is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio. In particular, attention must be paid to:

- Linearity, frequency and phase response of the TX Frequency Modulator. For a 4800 symbol/sec system, the frequency response should be within ± 2 dB over a range 3Hz to 5Hz, relative to 2400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the TX and RX reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a DC offset at the discriminator output.

Viewing the received signal eye (using the Mode Register RX Eye function) gives a good indication of the overall transmitter/receiver performance. See Figure 7 for the appearance of the RX Signal Eye.

*RX Mode,
RX EYE bit = '1'
(Mode Register B4)*

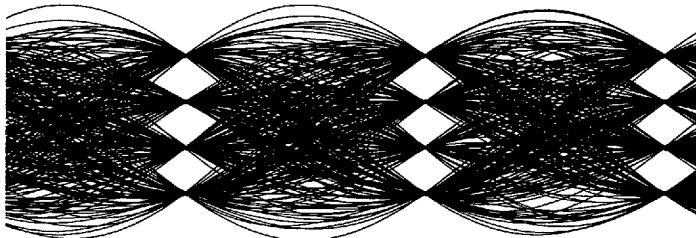


Figure 7 - RX Eye Signal at the TX Out pin for Pseudo-Random Received Data

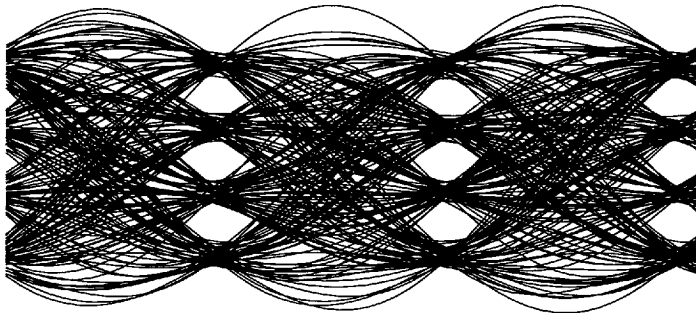


Figure 8 - TX Eye Diagram

Baseband and RF Frequency Requirements

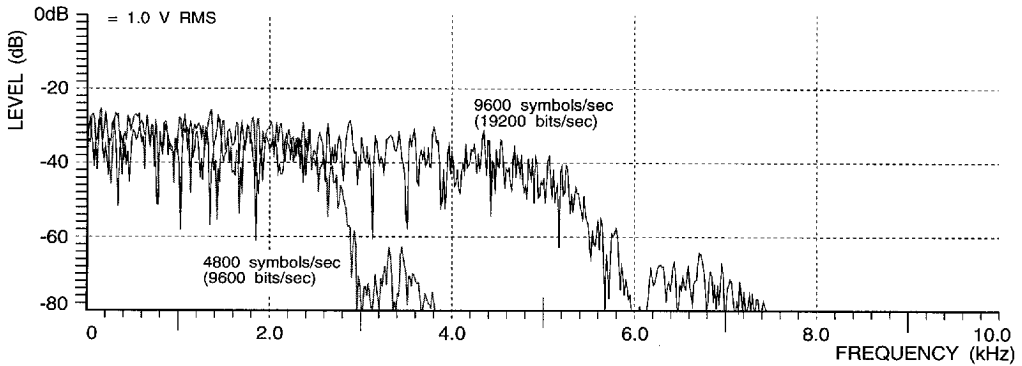


Figure 9 - "TX Out" Spectrum Plot

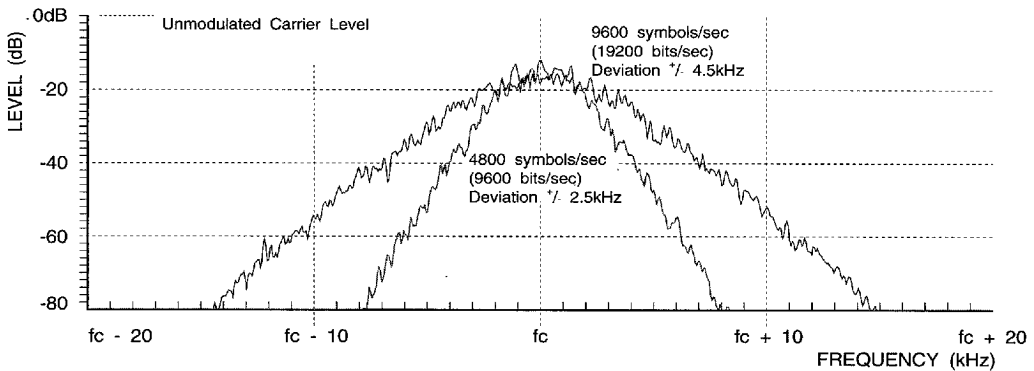


Figure 10 - Theoretical RF Spectrum Plot

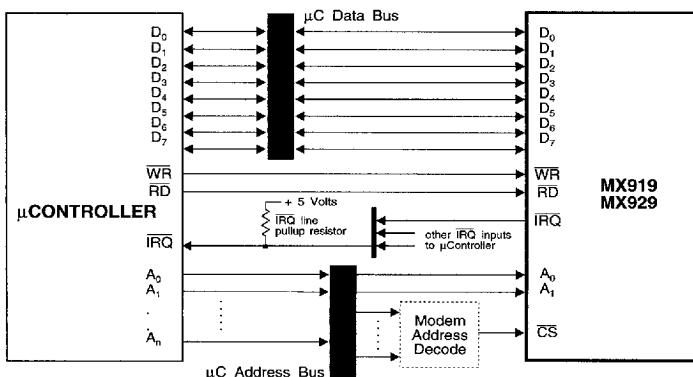


Figure 11 - Typical Modem to μ Controller Interface

The Data Bus Buffers and Address and Read/Write Decode blocks form a byte-wide parallel μ Controller interface. This diagram shows how this function can be memory mapped.

Programming Information

Data Formats

Frame and Data Structures

The MX919 Frame and data structures are illustrated in Figure 12, and the MX929 in Figure 13. The structures consist of a Frame Preamble (comprising Symbol and Frame Synchronization patterns) followed by one or more 'Header', 'Intermediate' or 'Last' blocks. The binary data transferred between the modem and the controlling μ Controller is that shown in the shaded area near the top of the diagram.

The 'Header' block is self-contained in that it includes its own CRC, and would normally carry information such as the addresses of the called and calling parties, the number of following blocks in the frame (if any), and miscellaneous control information.

The 'Intermediate' block(s) contain only data, the CRC checksum for all of the data in the 'Intermediate' and 'Last' blocks is contained at the end of the 'Last' block.

This arrangement, while efficient in terms of data capacity, may not be optimum for poor signal-to-noise conditions, since a reception error in any one of the 'Intermediate' or 'Last' blocks would invalidate the whole frame. In these conditions, increased throughput may be obtained by using the 'Header' block format for all blocks of the frame, so that blocks which are received correctly can be identified, and need not be retransmitted.

In the TX mode, the modem translates the 96 bits of the block into 66 4-level symbols as follows:

The 12 bytes are divided into 32 groups of three bits each (Tri-bits). An extra tri-bit ('0' '0' '0') is added giving a total of 33 tri-bits.

The 33 tri-bits are then passed to the Trellis Encoder which provides 66 4-level symbols.

In the RX mode, the modem takes the 66 received symbols and decodes them into tri-bits.

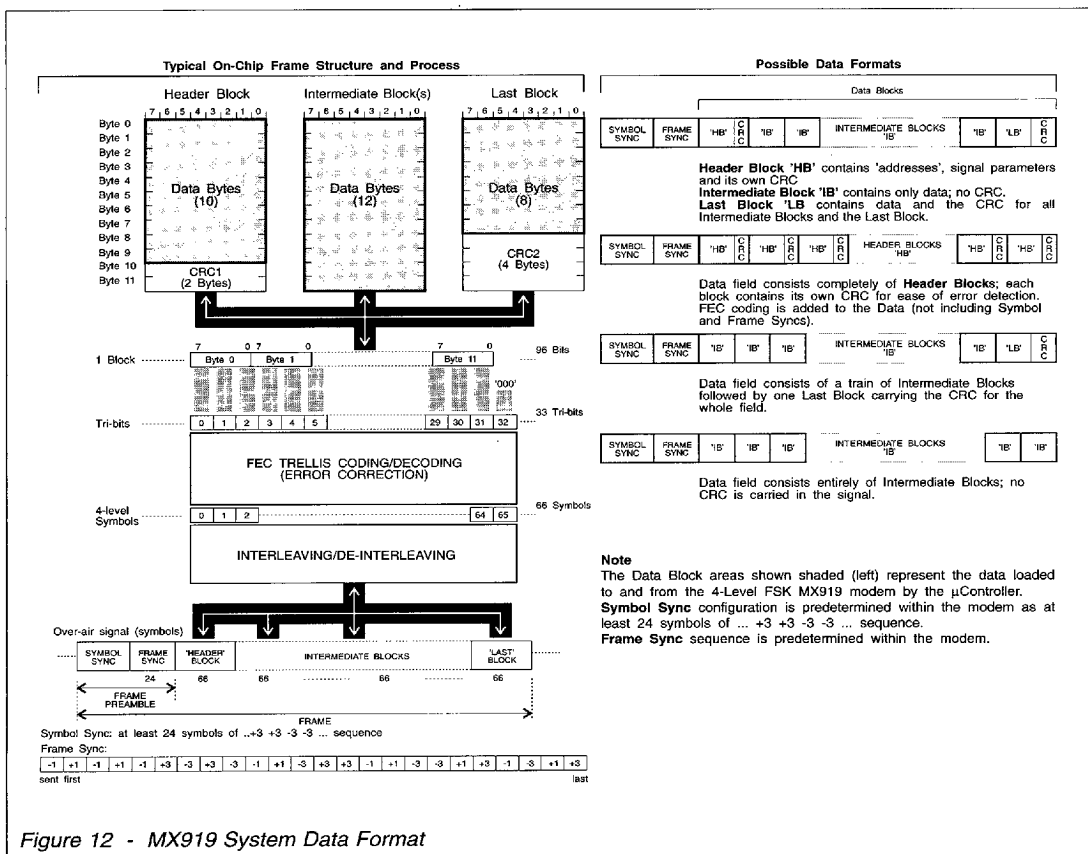


Figure 12 - MX919 System Data Format

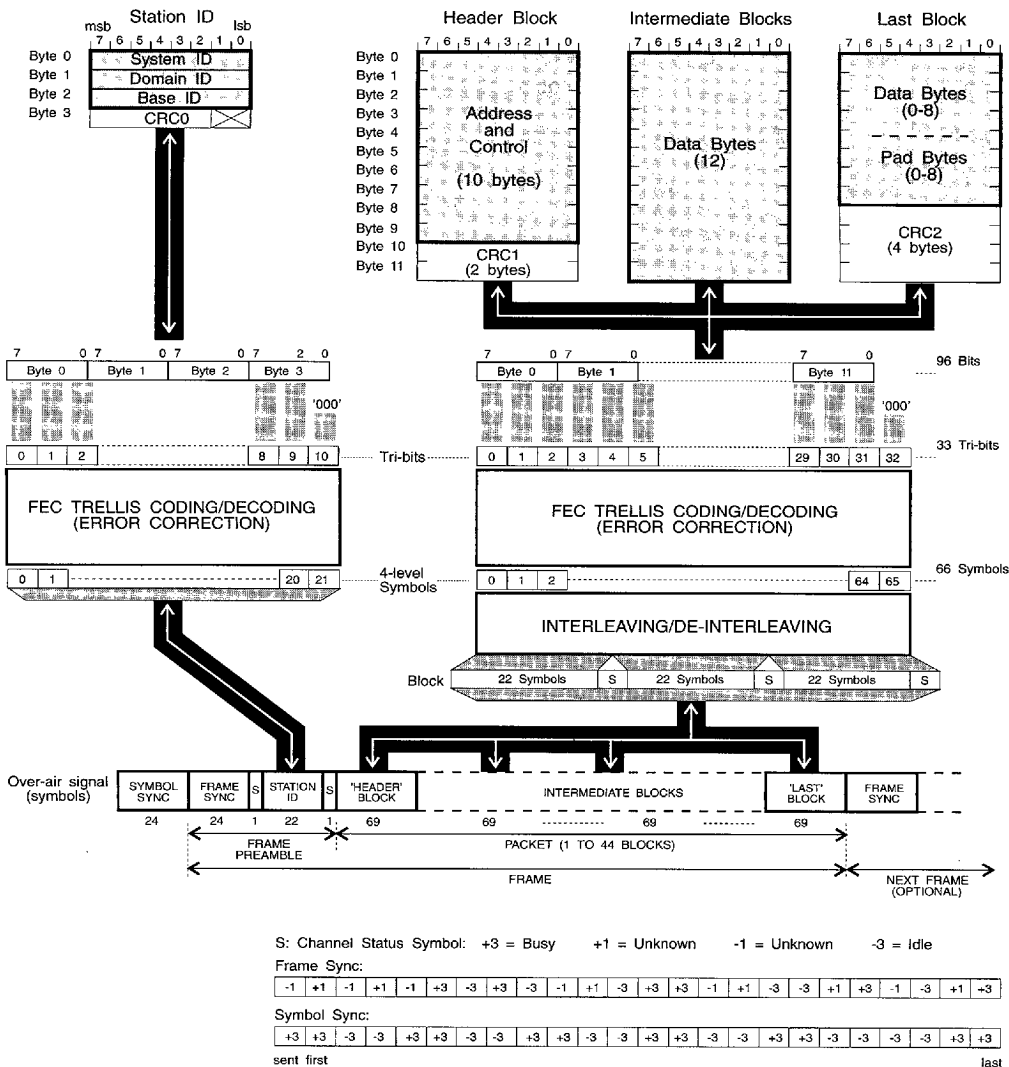


Figure 13 - MX929 System Data Format

Programming Information

Modem/ μ Controller Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction coding and interleaving. Details of the message format handled by the MX919 is shown in Figure 12; the format of the MX929 is in Figure 13.

To reduce the processing load on the associated μ Controller, the MX919/929 has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and - when in receive mode - in searching for and synchronizing onto the Frame Preamble. In normal operation the modem will only require servicing by the

μ Controller once per received or transmitted block.

Thus, to transmit a block, the controlling μ Controller has only to load the -unformatted - 'raw' binary data into the modem's Data Block Buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding) and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary -using the FEC coding to correct as many errors as possible- and check the resulting CRC before placing the received binary data into the Data Block Buffer for the μ Controller to read.

The MX919/929 can also handle the transmission and reception of unformatted data -to allow for example the transmission of Symbol and Frame Synchronization sequences or special test patterns.

Register Selection

The MX919 modem appears to the programmer as 4 write-only 8-bit registers shadowed by 3 read-only registers. Individual registers are selected by the A_1 and A_0 inputs; see Read and Write cycle timing diagrams (Figure 26).

Table 1 Register Selection

A_1	A_0	Write to Modem	Read from Modem
0	0	Data Block Buffer	Data Block Buffer
0	1	Command Register	Status Register
1	0	Control Register	D Q Register
1	1	Mode Register	not used

Data Block Buffer

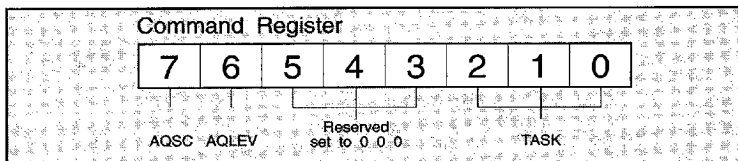
A 12-byte read/write buffer is used to transfer data (as opposed to Command, Status, Mode, Data-Quality and Control information) between the modem and the controlling μ Controller.

The Data Block Buffer appears to the μ Controller as a single 8-bit register; the modem ensures that sequential μ Controller 'read' or 'write' actions to the buffer are routed to the correct locations within this buffer. When the modem is in the TX mode, any attempt by the μ Controller to 'read' from this buffer will have no effect. Similarly, any attempt to 'write' to this buffer will have no effect when the modem is in the RX mode.

Command Register

Writing to this register instructs the modem to perform a specific action or actions, depending upon the setting of the TASK, AQLEV, and AQSC bits.

Figure 14 - The Command Register



When it has no action to perform (but is not powersaved), the modem will be in an idle state, and if it is in the TX mode the input to the TX Filter will be connected to a voltage mid-way between the '+1' and '-1' symbol voltages.

In the RX mode the modem will continue to measure the received data quality and extract bits from the received signal, feeding them into the De-Interleave Buffer, but will otherwise ignore the received data.

Programming Information

Command Register

B7

AQSC

Acquire Symbol Clock: This bit has no effect in the TX mode.

In the RX mode, whenever a byte with the AQSC bit set to logic '1' is written to the Command Register, it initiates an automatic sequence designed to achieve timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received symbol-timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to logic '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be restarted every time that a byte written to the Command Register has the AQSC bit set to logic '1'. The AQSC bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFSH/SFP (Search for Frame Sync + Header for MX919 / Search for Frame Preamble for MX929) task, however it may also be used independently to re-establish clock synchronization quickly after a long fade. Alternatively, an SFS or SFSH/SFP task may be written to the Command Register with the AQSC bit at logic '0' if it is known that clock synchronization does not need to be re-established. Refer to the Operational Information section for further details.

B6

AQLEV

Acquire Receive Signal Levels: This bit has no effect in the TX mode.

In receive mode, whenever a byte with the AQLEV bit set to a logic '1' is written to the Command Register, it initiates an automatic sequence designed to measure the amplitude and DC offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time -hence improving the measurement accuracy- until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to a logic '0' (or changing it from '1' to '0') has no effect. Note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQLEV bit set to a logic '1'.

The AQLEV bit will normally be set at the same time as an SFS (Search for Frame Sync) or SFSH/SFP (Search for Frame Sync + Header for MX919 / Search for Frame Preamble for MX929) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFSH/SFP task may be written to the Command Register with the AQLEV bit at logic '0' if it is known that there is no need to re-establish the received signal levels. Refer to the Operational Information section of this publication for further details.

B5

B4

B3

These bits should each be set to a logic '0'.

B2

B1

B0

TASK

Task: Operations such as transmitting a data block are treated by the modem as 'Tasks'. Information on Task functions is given on the following pages.

A task is initiated when the μ Controller writes a byte to the Command Register with the Task bits set to anything other than the 'NULL' ('0' '0' '0') code.

The μ Controller should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is a logic '0'.

Different tasks apply in receive and transmit modes.

TX Mode: All tasks other than NULL, RESET instruct the modem to transmit data from the Data Block Buffer, formatting it as required. For these tasks the μ Controller should wait until the BFREE (Buffer Free) bit of the Status Register is a logic '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number '0' of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will: Set the BFREE (Buffer Free) bit of the Status Register to a logic '0', take the data from the Data Buffer as quickly as it can -transferring it to the Interleave Buffer for eventual transmission. (continued...)

Programming Information

Command Register

B2

B1

B0

TASK

Task: This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer. Once all of the data has been transferred from the Data Block Buffer the modem will set the BFREE and IRQ bits of the Status Register to a logic '1', (causing the IRQ output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the μ Controller that it may write new data and the next task to the modem.

In this way the μ Controller can write a task -and the associated data- to the modem while the modem is still transmitting the data from the previous task.

RX Mode: The μ Controller should wait until the BFREE bit of the Status Register is a logic '1', then write the desired task to the Command Register. Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to a logic '0'.

Wait until enough received bits are in the De-Interleave Buffer.

Decode them as needed, and transfer any resulting data to the Data Block Buffer.

Then the modem will set the BFREE and IRQ bits of the Status Register to logic '1', (causing the IRQ output to go low if the IRQEN bit of the Mode Register has been set to a logic '1') to tell the μ Controller that it may read from the Data Buffer and write the next task to the modem.

In this way the μ Controller can read data and write a new task to the modem while the received symbols needed for this new task are being stored in the De-Interleave Buffer.

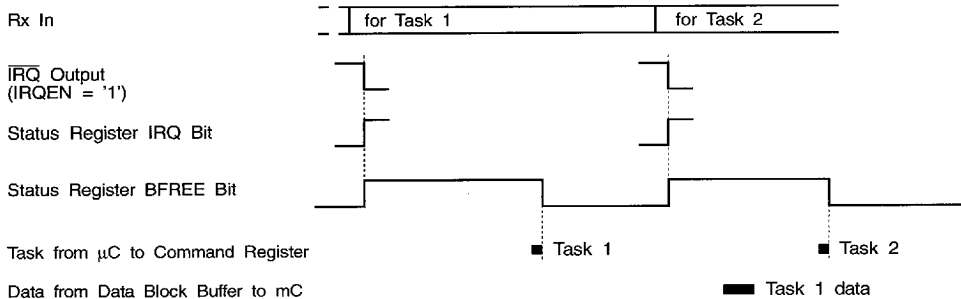


Figure 15 - The Receive Process

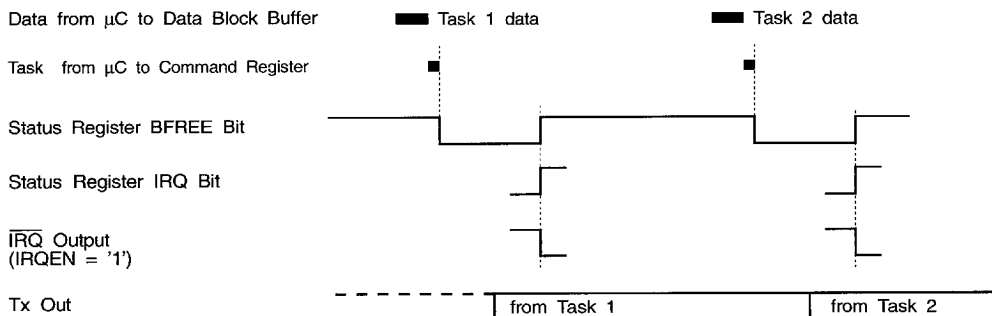


Figure 16 - The Transmit Process

Programming Information

Modem Tasks in Detail

The following tables describe the setting and format of the Command Register 'task' bits (bits 2, 1 and 0). Note that before a task is programmed the TX/RX bit in the Mode Register must be placed in the relevant position.

MX919 General Purpose Modem Tasks										
Command Bits										
2	1	0		Receive Mode			Transmit Mode			
0	0	0	NULL	..	..	..	NULL	..	..	..
0	0	1	SFSH	Search for Frame Sync + Header			T24S	Transmit 24 Symbols		
0	1	0	RHB	Read Header Block			THB	Transmit Header Block		
0	1	1	RILB	Read Intermediate or Last Block			TIB	Transmit Intermediate Block		
1	0	0	SFS	Search for Frame Sync			TLB	Transmit Last Block		
1	0	1	R4S	Read 4 Symbols			T4S	Transmit 4 Symbols		
1	1	0	NULL	..	..	..	NULL	..	..	..
1	1	1	RESET	Cancel any Current Action			RESET	Cancel any Current Action		
Table 2 - MX919 Modem Task Details										

Table 2 - MX919 Modem Task Details

MX929 RD-LAP Modem Tasks										
Command Bits										
2	1	0		Receive Mode			Transmit Mode			
0	0	0	NULL	..	..	..	NULL	..	..	..
0	0	1	SFP	Search for Frame Preamble			T24S	Transmit 24 Symbols		
0	1	0	RHB	Read Header Block			THB	Transmit Header Block		
0	1	1	RILB	Read Intermediate or Last Block			TIB	Transmit Intermediate Block		
1	0	0	SFS	Search for Frame Sync			TLB	Transmit Last Block		
1	0	1	R4S	Read 4 Symbols			T4S	Transmit 4 Symbols		
1	1	0	RSID	Read Station ID			TSID	Transmit Station ID		
1	1	1	RESET	Cancel any Current Action			RESET	Cancel any Current Action		
Table 3 - MX929 Modem Task Details										

Table 3 - MX929 Modem Task Details

MX919 Modem Tasks	
NULL	No Effect. This task is provided so that an AQSC or AQLEV (Command Register) command can be initiated without loading a new task.
SFSH	Search for Frame Sync + Header Block. Causes the MX919 to search the received signal for a valid 24-symbol Frame Sync sequence followed by a Header Block which has a correct CRC1 checksum. This task continues until a valid Frame Sync + Header Block has been found. The search consists of two stages: 1. The MX919 will attempt to match the incoming symbols against the General Purpose Modem Frame Synchronization pattern to within

MX929 Modem Tasks	
NULL	No Effect. This task is provided so that an AQSC or AQLEV (Command Register) command can be initiated without loading a new task.
SFP	Search for Frame Preamble. Causes the MX929 to search the received signal for a valid RD-LAP Frame Preamble, consisting of a 24-symbol Frame Sync sequence followed by Station ID data which has a correct CRC0 checksum. This task continues until a valid Frame Preamble has been found. The search consists of four stages: 1. The MX929 will attempt to match the incoming symbols against the RD-LAP Frame Synchronization pattern

MX919 Modem Tasks

the tolerance defined by the Frame Sync Tolerance (FSTOL) bits of the Control Register.

2. Once a match has been found, the MX919 will read the next 66 symbols as if they were a 'Header' block, decoding the symbols and checking the CRC1 checksum. If the CRC1 checksum is incorrect the modem will resume the search, looking for a fresh Frame Sync pattern. If the CRC1 is correct, the 10 decoded data bytes will be placed into the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1' and the CRC Checksum Error (CRCERR) bit cleared low to a logic '0'.

On detecting that the BFREE bit of the Status Register has gone to a logic '0', the μ Controller should read the 10 bytes from the Data Block Buffer and then write the next task to the MX919's Command Register.

RHB

Read Header Block. Causes the MX919 to read the next 66 symbols as a 'Header' block, decoding them, placing the resulting 10 data bytes and the 2 received CRC bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register high to a logic '1' when the task is complete to indicate that the μ Controller may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to a logic '1' or '0' depending on the validity of the received CRC1 checksum bytes.

MX929 Modem Tasks

to within the tolerance defined by the Frame Sync Tolerance (FSTOL) bits of the Control Register

2. Once a match has been found, the MX929 will read the next 'S' symbol, then update the SVAL bits of the Status Register and set the SRDY bit to '1'. (The IRQ bit of the Status Register will also be set to '1' at this time if the SSIEN bit of the Mode Register is '1'.)
3. The MX929 will then read the next 22 symbols as Station ID data. The 22 Station ID symbols will be decoded and the CRC0 checked. If this is incorrect the MX929 will resume the search, looking for a fresh Frame Sync pattern.
4. If the received CRC0 is correct, the next 'S' symbol will be read, the SVAL bits of the Status Register updated and the SRDY, BFREE and IRQ bits set to a logic '1'. The CRC Checksum Error (CRCERR) bit will be cleared to a logic '0', and the three decoded Station ID bytes placed into the Data Block Buffer.

On detecting that the BFREE bit of the Status Register has gone to a logic '1', the μ Controller should read the 3 Station ID bytes from the Data Block Buffer and then write the next task to the MX929's Command Register.

RHB

Read Header Block. Causes the MX929 to read the next 69 symbols as a 'Header' block. It will strip out the 'S' symbols, then de-interleave and decode the remaining 66 symbols, placing the resulting 10 data bytes into the Data Block Buffer. It also sets the BFREE and IRQ bits of the Status Register to a logic '1' when the task is complete to indicate that the μ Controller may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to a logic '1' or '0' depending on

Programming Information

MX919 Modem Tasks

RILB

Read 'Intermediate' or 'Last' Block.
Causes the modem to read the next 66 symbols as an 'Intermediate' or 'Last' block (the µController should be able to tell from the received 'Header' block how many blocks are in the frame, and hence when to receive the 'Last' block).

In each case, the modem will decode the 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register high to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the modem's Command Register. If an 'Intermediate Block is received then the µController should read-out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µController need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum. Note that in the RX mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB.

MX929 Modem Tasks

the validity of the received CRC1 checksum bytes.

As each of the 3 'S' symbols of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1' the Status Register IRQ bit will also be set to '1'.)

RILB

Read 'Intermediate' or 'Last' Block.
Causes the modem to read the next 69 symbols as an 'Intermediate' or 'Last' block (the µController should be able to tell from the received 'Header' block how many blocks are in the frame, and hence when to receive the 'Last' block).

In each case, the MX929 will strip out the 3 'S' symbols, de-interleave and decode the remaining 66 symbols and place the resulting 12 bytes into the Data Block Buffer. The BFREE and IRQ bits of the Status Register are set to a logic '1' when the task is complete to indicate that the µController may read the data from the Data Block Buffer and write the next task to the MX929's Command Register.

If an 'Intermediate Block is received then the µController should read all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register. For a 'Last' block the µController needs only to read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum. Note that in the RX mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB.

As each of the 3 'S' symbols of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1' the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received the SRDY bit will be set to '1' at the same time the BFREE bit is set to '1'.

Programming Information

MX919 Modem Tasks

SFS **Search for Frame Sync.** Causes the MX919 to search the received signal for a 24-symbol sequence which matches the Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the modem will set the BFREE and IRQ bits of the Status Register high to a logic '1' to indicate to the μ Controller that it should write the next task to the Command Register.

R4S **Read 4 Symbols.** This task is intended for special tests and channel monitoring - perhaps preceded by an SFS task. Causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set high to a logic '1' to indicate that the μ Controller may read the data byte from the Data Block Buffer and write the next task to the Command Register.

MX929 Modem Tasks

SFS **Search for Frame Sync.** This task is intended for special test and channel monitoring purposes. It performs the first two parts of an SFP task.

SFS causes the MX929 to search the received signal for a 24-symbol sequence which matches the RD-LAP Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the MX929 will read the following 'S' symbol, then set the BFREE, IRQ and SRDY bits of the Status Register to a logic '1' and update the SVAL bits. The μ Controller may then write the next task to the Command Register.

R4S **Read 4 Symbols.** This task is intended for special test and channel monitoring purposes, perhaps preceded by an SFS task. It causes the MX929 to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set to a logic '1' to indicate that the μ Controller may read the data byte from the Data Block Buffer and write the next task to the Command Register.

RSID **Read Station ID.** This task causes the MX929 to read and decode the next 23 symbols as Station ID data followed by an 'S' symbol. It is similar to the last two parts of an SFP task except that it will not re-start if the received CRC0 is incorrect. It normally follows an SFS operation.

The decoded System, Domain and Base ID bytes will be placed into the Data Buffer, and the CRCERR bit of the Status Register will be set to '1' if the received CRC0 is incorrect. Otherwise it will be cleared to '0'. The SVAL bits of the Status Register will be updated and the BFREE, SRDY and IRQ bits will be set to '1' to indicate that the μ C may read the 3 Station ID bytes from the Data Block Buffer and write the next task to the MX929's Command Register.

Programming Information

MX919 Modem Tasks

T24S **Transmit 24 Symbols.** This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC or FEC.

Byte '0' of the Data Block Buffer is sent first, byte '5' last.

Once the modem has read all the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the μ Controller that it may write the next task and its data to the modem.

Table 4 shows what data has to be written to the Data Block Buffer to transmit the modem Symbol and Frame Sync Sequences.

THB **Transmit Header Block.** Takes 10 bytes of data (Address & Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the μ Controller that it may write the next task and its data to the modem.

TIB **Transmit Intermediate Block.** Takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Intermediate' Block. Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the μ Controller that it may write the next task and its data to the modem.

Note that in TX mode the CRC2 checksum circuits are initialized on completion of any

MX929 Modem Tasks

T24S **Transmit 24 Symbols.** This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC or FEC, interleaving or adding any 'S' symbols.

Byte '0' of the Data Block Buffer is sent first, byte '5' last.

Once the MX929 has read all the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the μ Controller that it may write the next task and its data to the modem.

Table 5 shows what data has to be written to the Data Block Buffer to transmit the modem Symbol and Frame Sync Sequences.

THB **Transmit Header Block.** Takes 10 bytes of data (Address & Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block, inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the μ Controller that it may write the next task and its data to the modem.

TIB **Transmit Intermediate Block.** Takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as an RD-LAP formatted 'Intermediate' Block, inserting 'S' symbols at 22-symbol intervals.

Once the MX929 has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the

Programming Information

MX919 Symbol and Frame Sync Sequences

Symbol Sync				Values written to Data Block Buffer		
Symbols					Binary	Hex
+3	+3	-3	-3	Byte 0 :	11110101	F5
+3	+3	-3	-3	Byte 1 :	11110101	F5
+3	+3	-3	-3	Byte 2 :	11110101	F5
+3	+3	-3	-3	Byte 3 :	11110101	F5
+3	+3	-3	-3	Byte 4 :	11110101	F5
+3	+3	-3	-3	Byte 5 :	11110101	F5

Frame Sync				Values written to Data Block Buffer		
Symbols					Binary	Hex
-1	+1	-1	+1	Byte 0 :	00100010	22
-1	+3	-3	+3	Byte 1 :	00110111	37
-3	-1	+1	-3	Byte 2 :	01001001	49
+3	+3	-1	+1	Byte 3 :	11110010	F2
-3	-3	+1	+3	Byte 4 :	01011011	5B
-1	-3	+1	+3	Byte 5 :	00011011	1B

Table 4 - MX919 Symbol and Frame Sync Sequences (T24S)

MX929 Symbol and Frame Sync Sequences

Symbol Sync				Values written to Data Block Buffer		
Symbols					Binary	Hex
+3	+3	-3	-3	Byte 0 :	11110101	F5
+3	+3	-3	-3	Byte 1 :	11110101	F5
+3	+3	-3	-3	Byte 2 :	11110101	F5
+3	+3	-3	-3	Byte 3 :	11110101	F5
+3	+3	-3	-3	Byte 4 :	11110101	F5
-3	-3	+3	+3	Byte 5 :	01011111	5F

Frame Sync				Values written to Data Block Buffer		
Symbols					Binary	Hex
-1	+1	-1	+1	Byte 0 :	00100010	22
-1	+3	-3	+3	Byte 1 :	00110111	37
-3	-1	+1	-3	Byte 2 :	01001001	49
+3	+3	-1	+1	Byte 3 :	11110010	F2
-3	-3	+1	+3	Byte 4 :	01011011	5B
-1	-3	+1	+3	Byte 5 :	00011011	1B

Table 5 - MX929 Symbol and Frame Sync Sequences (T24S)

Programming Information

MX919 Modem Tasks

task other than NULL, TIB or TLB.

TLB **Transmit 'Last' Block.** Takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12-bytes to 4-level symbols with (FEC), interleaves the symbols and transmits the result as a formatted 'Last' Block. Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set high to a logic '1', indicating to the μ Controller that it may write the next task and its data to the modem.

T4S **Transmit 4 Symbols.** This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

RESET **RESET.** Stop any current action. This 'task' takes effect immediately, and terminates any current action (task, AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register high to a logic '1', without setting the IRQ bit. RESET should be used to set the modem into a known state when V_{DD} is applied.

Note that due to delays in the transmit filter, it will take several symbol-times for any change to become apparent at the TXOp pin.

MX929 Modem Tasks

μ Controller that it may write the next task and its data to the modem.

Note that in TX mode the CRC2 checksum circuits are initialized on completion of any task other than NULL, TIB or TLB.

TLB **Transmit 'Last' Block.** Takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12-bytes to 4-level symbols with (FEC), interleaves the symbols and transmits the result as an RD-LAP formatted 'Last' Block, inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to a logic '1', indicating to the μ Controller that it may write the next task and its data to the modem.

T4S **Transmit 4 Symbols.** This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

TSID **Transmit Station ID.** This task takes 3 ID bytes from the Data Block Buffer, calculates and appends the 6-bit CRC0 checksum, translates the result to 4-level symbols (with FEC) and transmits the resulting 22 symbols preceded and followed by 'S' symbols.

RESET **RESET.** Stop any current action. This 'task' takes effect immediately, and terminates any current action (task, AQSC or AQLEV) the MX929 may be performing and sets the BFREE bit of the Status Register high to a logic '1', without setting the IRQ bit. RESET should be used to set the modem into a known state when V_{DD} is applied.

Note: due to delays in the transmit filter, it will take several symbol-times for any change to become apparent at the TXOp pin.

Programming Information

RRC Filter Delay

The Task Timing figures detailed in Tables 6 and 7 are based upon: the signal at the input to the RRC Filter in the transmit mode, or the signal at the input to the de-interleave circuits in the receive mode. As can be seen from the diagram in Figure 17, there is an additional delay of approximately 8 (eight) symbol-times in both TX and RX modes due to the (TX/RX) RRC Filter.

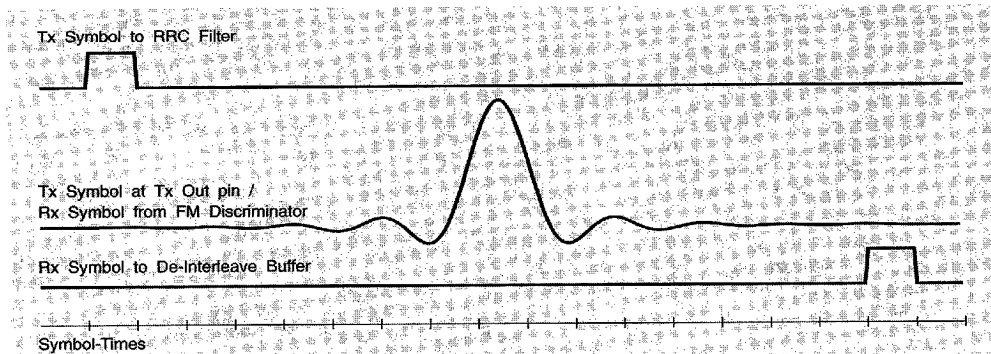


Figure 17 - Examples of Filter Delay Times

Transmit and Receive Task Timing

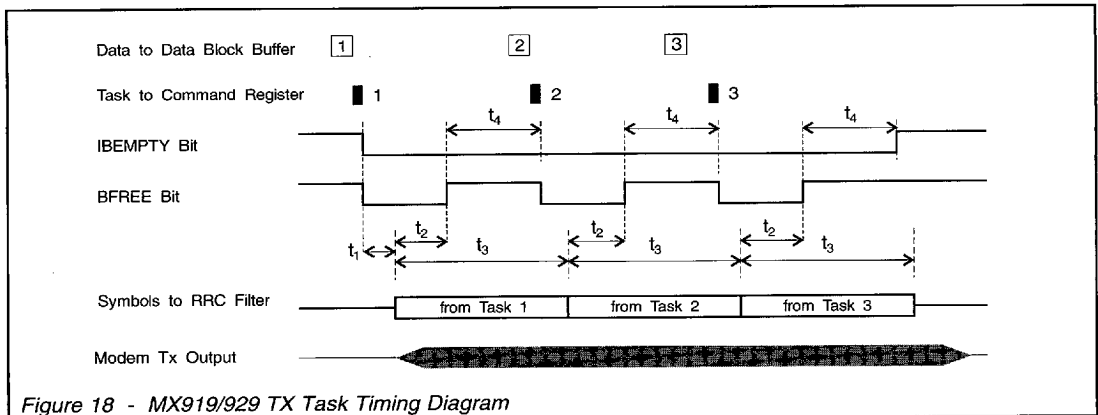


Figure 18 - MX919/929 TX Task Timing Diagram

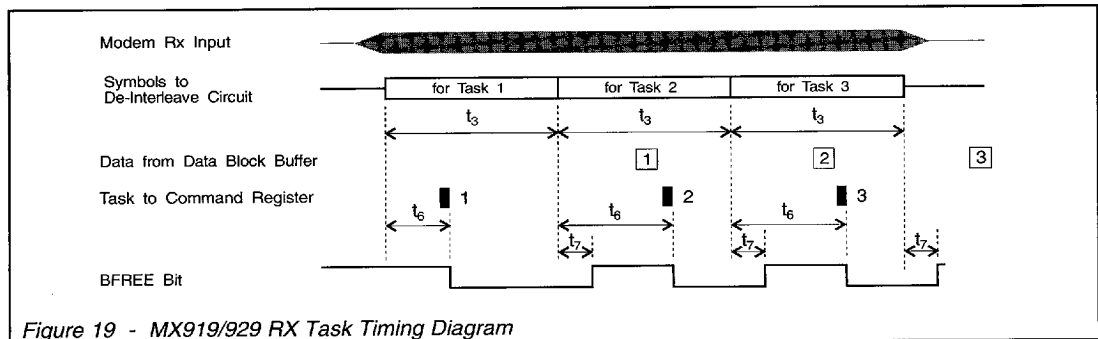


Figure 19 - MX919/929 RX Task Timing Diagram

MX919 Timing			
Timing	Notes	Task	Typical (Symbol) Time
t_1	Modem in idle state. Time from writing first task to the application of the first TX symbol to the RRC Filter.	Any	1
t_2	Time from the application of the first symbol of the task to the RRC Filter until BFREE goes to a logic '1' (high).	T24S/TSID THB/TIB/TLB T4S	5 16 1
t_3	Time to transmit all symbols of the task. or Time to receive all symbols of the task	T24S THB/TIB/TLB RHB/RILB T4S SFS SFSH R4S	24 66 66 4 <24 <90 4
t_4	Maximum time allowed from BFREE going to a logic '1' for the next task (and data) to be written to the modem.	T24S THB/TIB/TLB T4S	18 49 2
t_6	Maximum time between the first symbol of the task entering the de-interleave circuit and the task being written to the modem.	SFSH RHB/RILB SFS R4S	21 49 21 3
t_7	Time from last symbol of task entering the de-interleave circuit to BFREE going to a logic '1'.	Any	1

Table 6 - Typical RX/TX Task Load Timings (MX919)

MX929 Timing			
Timing	Notes	Task	Typical (Symbol) Time
t_1	Modem in idle state. Time from writing first task to the application of the first TX symbol to the RRC Filter.	Any	1
t_2	Time from the application of the first symbol of the task to the RRC Filter until BFREE goes to a logic '1' (high).	T24S/TSID THB/TIB/TLB T4S	5 16 1
t_3	Time to transmit all symbols of the task. or Time to receive all symbols of the task	T24S/TSID THB/TIB/TLB RSID RHB/RILB T4S/R4S SFP SFS	24 69 23 69 4 <48 <25
t_4	Maximum time allowed from BFREE going to a logic '1' for the next task (and data) to be written to the modem.	T24S THB/TIB/TLB TSID T4S	18 52 18 2
t_6	Maximum time between the first symbol of the task entering the de-interleave circuit and the task being written to the modem.	SFP/SFS RHB/RILB RSID R4S	21 51 15 3
t_7	Time from last symbol of task entering the de-interleave circuit to BFREE going to a logic '1'.	Any	1

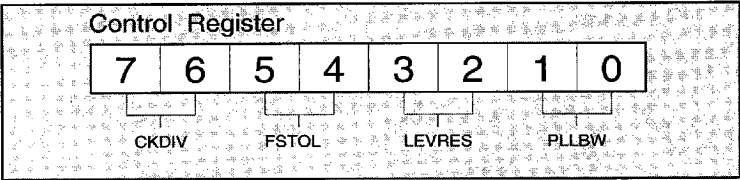
Table 7 - Typical RX/TX Task Load Timings (MX929)

Programming Information

Control Register

This 8-bit write-only register controls the modem's symbol-rate, the response times of the receive clock extraction and signal level measurement circuits and the Frame Sync pattern recognition tolerance.

Figure 20 - The Control Register



Control Register

Table 8 shows how bit-rates of 2400/4800/9600 symbols per second may be obtained from common Xtal/clock frequencies. The values of C_3 and C_4 should be suitable for the frequency of the Xtal X_1 . For $X_1 < 5.0\text{MHz}$, $C_3 = C_4 = 33.0\text{pF}$; for $X_1 > 5.0\text{MHz}$, $C_3 = C_4 = 18.0\text{pF}$.

B7, B6
CKDIV

Clock Division Ratio: These bits control a frequency divider driven from the clock signal present at the Xtal pin; this ratio and Xtal input will determine the nominal bit-rate.

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
			Symbol Rate (symbols/sec.)		
B7	B6	Division Ratio Xtal Freq. Symbol Rate			
0	0	512	4800	9600	
0	1	1024	2400	4800	9600
1	0	2048		2400	4800
1	1	4096			1200

Table 8 - Clock/Data Rates Note that device operation is not guaranteed or specified above 9,600symbols/s or below 2,400symbols/s

B5, B4
FSTOL

Frame Sync Tolerance: For use in the RX mode only; these bits have no effect in the RX mode. These bits define the maximum number of mismatches which will be allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches Allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note that a single 'mismatch' is defined as the difference between two adjacent symbol levels; if the symbol '+1' were expected, then the received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2.

_____	+3	_____
_____	+1	_____
_____	-1	_____
_____	-3	_____

Symbol Levels

Programming Information

Control Register

**B3, B2
LEVRES**

Level Measurement Response Time: These bits are only used in the RX mode and have no effect in the TX mode; they set the 'normal' response time of the RX signal amplitude and dc offset measuring circuits. This setting will be temporarily overridden by the automatic sequencing of an AQLEV command.

For most general-purpose applications using this modem, these bits should normally be set to 'Peak Averaging', except when the μ Controller detects a receive signal fade, when 'Hold' should be selected. The 'Peak Detect' setting is intended for systems where the μ Controller cannot detect signal fades or the start of a received message; this setting allows the modem to respond quickly to fresh messages and recover rapidly after a fade without μ Controller intervention -this however will be at the cost of reduced Bit-Error-Rate vs Signal-to-Noise performance.

The Signal Average setting is a test mode and should not normally be used.

Note that as the measured levels are stored on capacitors C_6 and C_7 via pins Doc 1 and Doc 2, these levels will decay gradually towards V_{BIAS} when the 'Hold' setting is used; the discharge time-constant is approximately 1000 symbol-times.

Table 9 details the bit-setting application.

B3	B2	Setting	Action
0	0	Hold	Keep current values of amplitude and offset
0	1	Peak Averaging	Track input signal using bit peak averaging
1	0	Peak Detect	Track input signal using peak detection
1	1	Signal Average	Measure average signal level

Table 9

**B1, B0
PLLBW**

PLL Bandwidth: For use in the RX mode only (no effect in TX).

In the receive mode these two bits set the 'normal' bandwidth of the RX Clock Extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequence of an AQSC (Command Register Bit 7) command.

B1	B0	PLL Bandwidth ($\pm$ ppm)	Note
0	0	0 (Hold)	For use during signal fades
0	1	30	
1	0	250	
1	1	50,000	

Table 10

The 'Hold' setting is intended for use during signal fades otherwise the minimum bandwidth consistent with the RX and TX modem symbol-rate tolerances should be chosen, i.e. if the Xtals used with both modems have accuracies of ± 100 ppm, the PLLBW bits (B1, B0) should be set to '1', '0'.

The very wide bandwidth ('1', '1') is intended for systems where the μ Controller cannot detect signal fades or the start of a receive message; it allows the modem to respond rapidly to fresh messages and recover rapidly after a fade without μ Controller intervention. This action however is at the expense of reduced Bit-Error-Rate vs Signal-to-Noise performance.

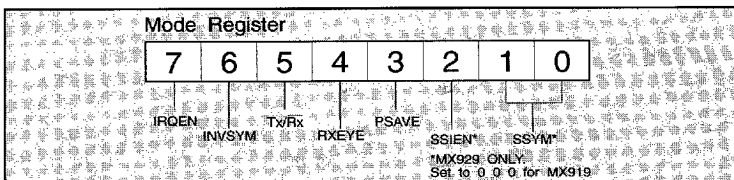
Note that PLL bandwidth figures are intended for 'a reasonably random received signal.'

Programming Information

Mode Register

This 8-bit write-only register controls the basic operating modes of the modem.

Figure 21 - The Mode Register



Mode Register

B7
IRQEN

IRQ Output Enable: When set to a logic '1' the Interrupt Request output will low (logic '0') whenever the IRQ bit (BIT 7) of the Status Register is set by the modem to a logic '1'. When set to a logic '0' the Interrupt Request output will not function and will remain in its high-impedance state (see Pin Functions and Figure 11 - μ Controller Interface).

B6
INVSYM

Invert Symbols: Controls the polarity (sense) inversion of transmitted and received symbol voltages.

B6	Symbol	Signal at TX Out	Signal at RX Feedback
'0'	'+3'	above V_{BIAS}	below V_{BIAS}
'0'	'-3'	below V_{BIAS}	above V_{BIAS}
'1'	'+3'	below V_{BIAS}	above V_{BIAS}
'1'	'-3'	above V_{BIAS}	below V_{BIAS}

B5
TX/RX

TX/RX Mode: When set to a logic '1' places the modem in the Transmit mode; when set to a logic '0' places the modem in the Receive mode. Note that changing between Transmit and Receive modes will cancel any current task.

B4
RX Eye

Show RX Eye: This bit should be set to a logic '0' for normal RX operation and always for TX operation. Setting this bit to a logic '1' in the receive mode configures the modem into a special test mode, in which the input to the TX Output Buffer is connected to the RX Symbol/Clock Extraction circuit at a point which carries the equalized receive signal. This may be monitored with an oscilloscope (at the TX Out pin *before* the external RC filter), to assess the quality of the complete radio channel including the TX and RX modem filters, the TX modulator and the RX IF filters and FM demodulator. The resulting 'eye' diagram (for reasonably random data) should ideally be as shown in Figure 7, with 4 'crisp' and equally spaced crossings.

B3
PSAVE

Powersave: When set to a logic '1' places the modem in its Powersave mode. In this mode the following circuits only are disabled: Internal Filters, RX Symbol and Clock Extraction Circuits and the TX Output Buffer; the TX Out pin is connected to V_{BIAS} through a high-value resistance. Xtal oscillator circuits and the μ Controller Interface logic and the RX Input Amplifier continue to operate. Note that RX clock and levels will be lost if Powersave mode is selected.

Setting to a logic '0' restores power to all of the device circuitry and the modem is in its operational mode. Note that the internal filters -and hence the TX Out pin in the TX mode- will take about 20 symbol-times to settle after this bit is taken from a logic '1' to '0'.

B2
SSIEN
(MX929)

'S' Symbol IRQ Enable (MX929 only): In Receive mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a new 'S' symbol has been received. (The SRDY bit of the Status Register will be set to '1' at the same time, and the SVAL bits updated to reflect the received 'S' symbol.) In Transmit mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever an 'S' symbol has been transmitted. (The SRDY bit of the Status Register will be set to '1' at the same time).

On the MX919, this bit should always be set to a logic '0'.

B1 B0
SSYM
(MX929)

'S' Symbol to be Transmitted (MX929 only): For the MX929, these bits have no effect in RX mode. In Transmit mode, these bits define the next 'S' symbol to be transmitted.

On the MX919, these bits should always be set to a logic '0'.

Programming Information

Status Register

This register may be read by the μ Controller to determine the current state of the modem.

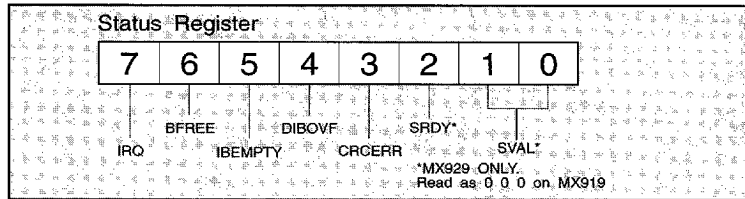


Figure 22 - The Status Register

Status Register

B7
IRQ

Interrupt Request: This bit is set to a logic '1' by:

The Status Register BFREE bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's PSAVE or TX/RX bits.

or

The Status Register IEMPTY bit going from a logic '0' to '1', unless this transition is caused by a RESET Task or by a change to the Mode Register's PSAVE or TX/RX bits.

or

The Status Register DIBOVF bit going from a logic '0' to '1'.

This (IRQ) bit is cleared to a logic '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is a logic '1', the MX919/929 IRQ output pin will be pulled low (to V_{SS}) whenever the Status Register IRQ bit is a logic '1'.

B6
BFREE

Data Block Buffer Free: BFREE reflects the availability of the Data Block Buffer; BFREE is cleared to a logic '0' (*Buffer NOT Free*) whenever a task other than NULL or RESET is written to the Command Register.

In Transmit mode, the BFREE bit will be set to a logic '1' (also setting the Status Register IRQ bit to a logic '1') when the modem is ready for the μ Controller to write new data to the Data Block Buffer and the next task to the Command Register.

In Receive mode, the BFREE bit is set to a logic '1' (also setting the Status Register IRQ bit to a logic '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The μ Controller may then read that data and write the next task to the Command Register.

The BFREE bit is also set to a logic '1' -but without setting the IRQ bit- by a RESET task or when the Mode Register PSAVE or TX/RX bits are changed.

B5
IEMPTY

Interleave Buffer Empty: In Transmit mode, IEMPTY is set to a logic '1' (also setting the IRQ bit) when less than two symbols remain in the Interleave Buffer or the Interleave Buffer is empty. Any transmit task written to the modem after IEMPTY goes to a logic '1' will be too late to avoid a gap in the transmit output signal (see Figure 18 and Tables 6 & 7, TX Task Timing)

IEMPTY is also set to a logic '1' by a RESET task and by a change of the Mode Register PSAVE or TX/RX bits, but in these cases the IRQ bit will not be set.

IEMPTY is cleared to a logic '0' within 1-symbol time after a task other than NULL or RESET is written to the Command Register.

Note that when the modem is in the transmit mode and the Interleave Buffer is empty, a mid-level (half-way between '+1' and '-1') will be fed to the RRCFilter.

In Receive mode this bit is a logic '0'.

Programming Information

Status Register

B4
DIBOVF

De-Interleave Buffer Overflow: In Receive mode DIBOVF is set to a logic '1' (also setting the IRQ bit) when an RHB, RILB, RSID or R4S task is written to the Command Register too late to allow continuous reception (see Figure 19 and Tables 6 & 7, RX Task Timing). DIBOVF is cleared to a logic '0' by reading the Status Register, by writing a RESET task to the Command Register or by changing the PSAVE or TX/RX bits of the Mode Register. In Transmit mode this bit is a logic '0'.

B3
CRCERR

CRC Checksum Error: In Receive mode CRCFEC will be updated at the end of an SFSH, RHB, or RILB task to reflect the result of the receive CRC check. A logic '0' indicates that the CRC was received correctly. A logic '1' indicates that an error is present. Note that this bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received. CRCERR is cleared to a logic '0' by a RESET task, or by changing the PSAVE or TX/RX bits of the Mode Register. In Transmit mode this bit is a logic '0'.

B2
SRDY
(MX929)

'S' Symbol Ready (MX929 only): In Receive mode, this bit is set to '1' whenever an 'S' symbol has been received. The μ C may then read the value of the symbol from the SVAL field of the Status Register. In Transmit mode, this bit is set to '1' whenever an 'S' symbol has been transmitted. The bit is cleared to '0' by a read of the Status Register, by a RESET task or by changing the PSAVE or TXRXN bits of the Mode Register. On the MX919, this bit should always be set to a logic '0'.

B1, B0
SVAL
(MX929)

Received 'S' Symbol Value (MX929 only): In Receive mode, these bits reflect the value of the latest received 'S' symbol. In Transmit mode, these bits will be '0'. On the MX919, these bits should always be set to a logic '0'.

The Data Quality Register

In Receive Mode, the modem continuously measures the quality of the received signal by comparing the actual received waveform over the previous 64 symbol times against an internally generated "ideal". The result is placed into bits 3 to 7 of the Data Quality Register for the μ Controller to read at any time, bits 0 to 2 being always set to '0'. Figure 22 shows how the value (0 to 255) read from the Data Quality Register varies with the received signal-to-noise ratio. In Transmit Mode all bits are set to a logic '0'.

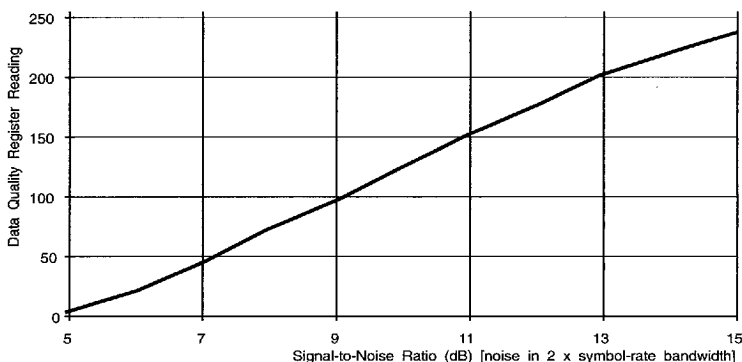
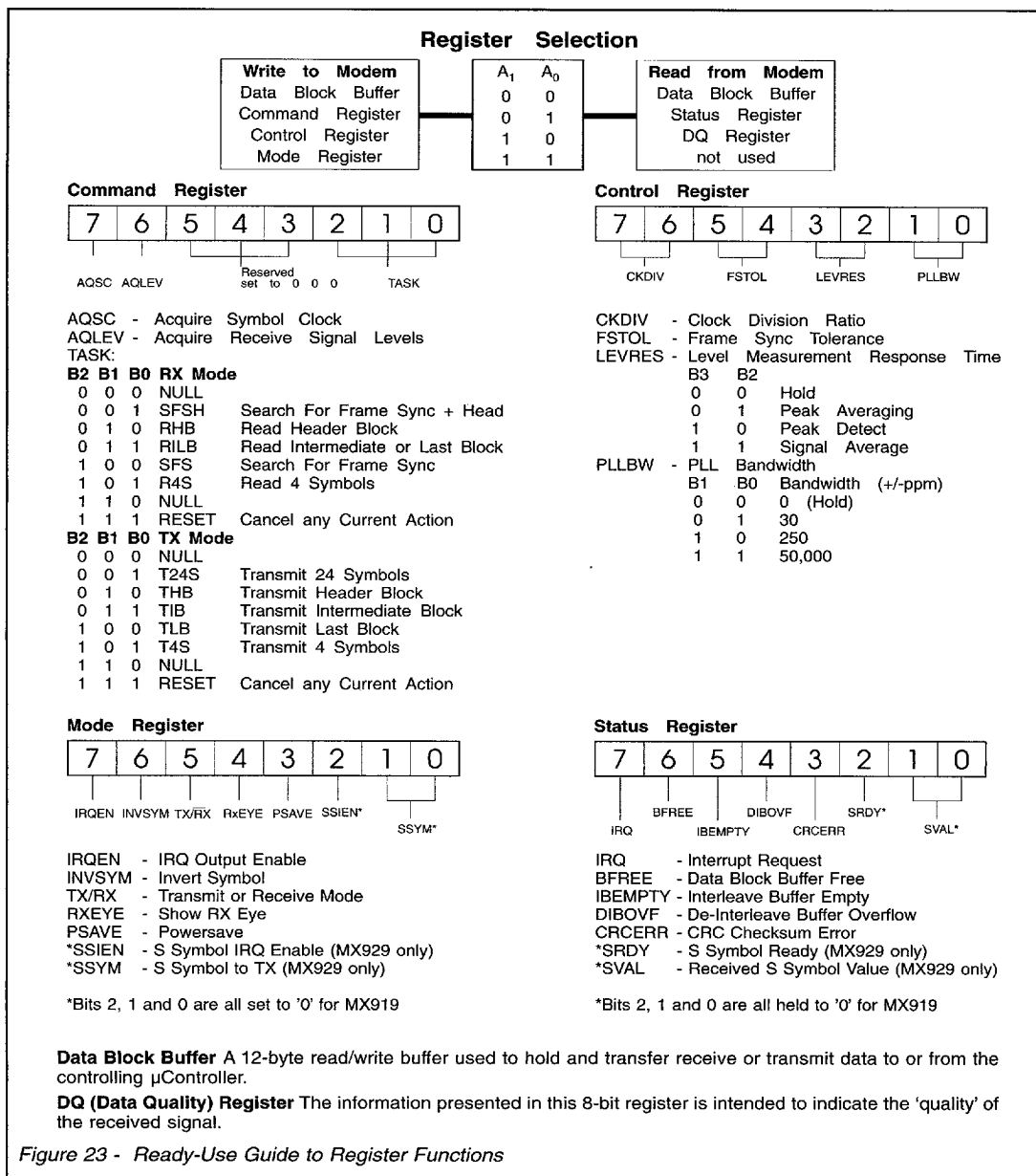


Figure 22 - Typical Data Quality Reading vs RX Signal-to-Noise Ratio

Programming Information

MX919 & MX929 Modem Register Selection

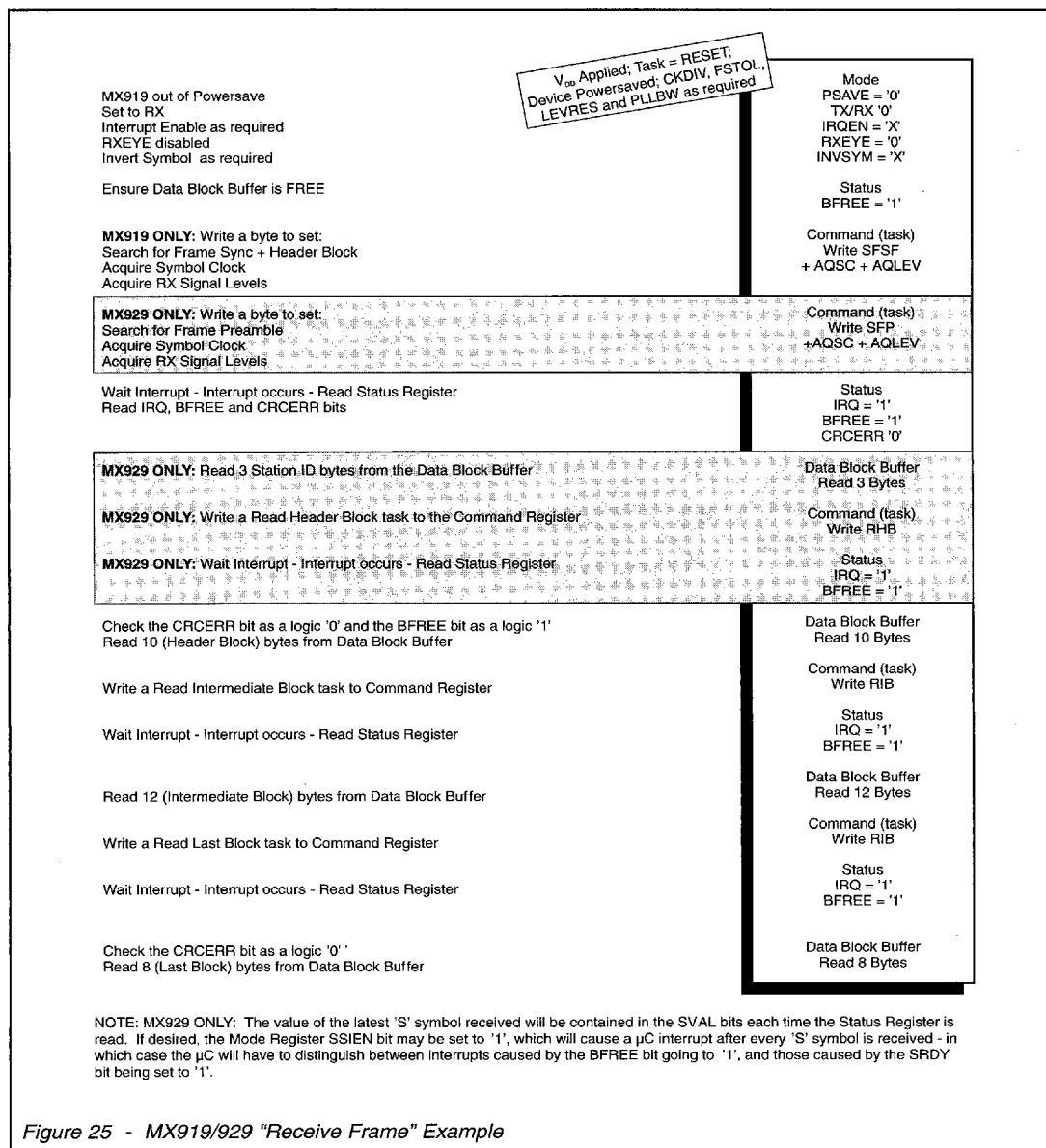
The following diagram is a quick-reference to MX919/MX929 register allocations. The MX919/MX929 modem appears to the programmer as 4 write-only 8-bit registers shadowed by 3 read-only registers. Individual registers are selected by the A_1 and A_0 inputs.



MX919/929 “Transmit Frame” Example

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MX919/929 “Receive Frame” Example



Operational Information**Operation Details****Forward Error Correction****Header/Intermediate/Last Block FEC**

Transmit Mode, the MX919/929 translates the 96 bits of the block (12 bytes) into 66 4-level symbols as follows:

The 12 bytes are divided into 32 groups of three bits each (called tri-bits). An extra tri-bit '000' is added giving a total of 33 tri-bits. The 33 tri-bits are then passed to a Trellis Encoder to give 66 4-level symbols.

Receive Mode, the MX919/929 takes the 66 received signals and decodes them into tri-bits.

Cyclic Redundancy Codes**CRC0 (MX929 only)**

This is a six-bit CRC check code used in the Station ID Block. It is calculated by the modem from the first 24 bits of the block (Bytes 0, 1 & 2) as follows:

The 24 bits are considered as the coefficients of a polynomial $M(x)$ of degree 23, such that the bit (7) of byte 0 is the coefficient of x^{23} , and bit 0 of byte 2 is the coefficient of x^0 .

The polynomial $F(x)$ of degree 5 is calculated as being the remainder of the division

$$x^6 M(x) / (x^6 + x^4 + x^3 + 1)$$

where division is performed modulo-2.

The polynomial $x^5 + x^4 + x^3 + x^2 + x^1 + x^0$ is added (modulo-2) to $F(x)$

The coefficients of $F(x)$ are placed in the 6-bit CRC0 field, such that the coefficient of x^5 corresponds to the MSB of CRC0.

CRC1 (MX919/929)

This is a sixteen-bit CRC check code used in the Header Block. It is calculated by the modem from the first 80 bits of the block (Bytes 0 to 9 inclusive) as follows:

The 80 bits are considered as the coefficients of a polynomial $M(x)$ of degree 79, such that the bit (7) of byte 0 is the coefficient of x^{79} , and bit 0 of byte 9 is the coefficient of x^0 .

The polynomial $F(x)$ of degree 15 is calculated as being the remainder of the division

$$x^{16} M(x) / (x^{16} + x^{12} + x^5 + 1)$$

where division is performed modulo-2.

The polynomial $x^{15} x^{14} \dots + x^4 + x^3 + x^2 + x^1 + x^0$ (all coefficients = 1) is added (modulo-2) to $F(x)$

The coefficients of $F(x)$ are placed in the 16-bit CRC1 field, such that the coefficient of x^{15} corresponds to the MSB of byte 10 of the header block.

CRC2 (MX919/929)

This is a thirty-two-bit CRC check code transmitted at the end of the 'Last' Block. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block as follows:

Let k be the total number of bits in all of the bytes over which the CRC is to be calculated.

These k bits are considered as the coefficients of a polynomial $M(x)$ of degree $(k-1)$, such that the bit (7) of byte 0 is the coefficient of x^{k-1} , and bit 0 of the last byte is the coefficient of x^0 .

The polynomial $F(x)$ of degree 31 is calculated as being the remainder of the division

$$x^{32} M(x) / (x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1)$$

where division is performed modulo-2.

The polynomial $x^{31} x^{30} \dots + x^4 + x^3 + x^2 + x^1 + x^0$ (all coefficients = 1) is added (modulo-2) to $F(x)$

The coefficients of $F(x)$ are placed in the 32-bit CRC2 field, such that the coefficient of x^{31} corresponds to the msb of byte 8 of the 'last' block.

Operational Information

Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission to give protection against noise bursts and short fades.

Interleaving is not performed on the Frame or Symbol Synchronization sequences.

0	1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	17	18
19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
55	56	57	58	59	60	61	62	63	64								

Considering the 66 4-level symbols to be numbered sequentially (as above) before interleaving, then after interleaving the symbols will be transmitted in the sequence shown below:

First

0	1	8	9	16	17	24	25	32	33	40	41	48	49	56	57	64	65
2	3	10	11	18	19	26	27	34	35	42	43	50	51	58	59	4	5
12	13	20	21	28	29	36	37	44	45	52	53	60	61	6	7	14	15
22	23	30	31	38	39	46	47	54	55	-----Last							

The inverse operation (De-Interleaving) is performed in the receive mode.

Operational Information**Received Signal Acquisition****Level Measurement and Clock Extraction**

To achieve reasonable error rates the MX919/929 needs to make accurate measurements of the received signal amplitude, DC offset and symbol timing, and of course accurate measurements -especially in the presence of noise- are best made by averaging over a relatively long time period.

In most cases the modem will be used to receive isolated messages from a distant transmitter that is only turned on for a very short time before the message starts; also, the received baseband signal from the radio's frequency discriminator will have a dc offset due to small differences between the receiver and transmitter reference oscillators and hence their 'carrier' frequencies.

To provide for this situation, AQSC and AQLEV (Acquire Symbol Clock and Level) commands are provided which, when triggered, cause the modem to follow an automatic sequence designed to perform the measurements as quickly as possible. See the section on the Command Register.

Acquire Receive Signal Levels**AQLEV****Command Register**

The Acquire Receive Signal Levels (AQLEV) sequence starts with a measurement of the average signal voltage over a period of 1 symbol-time to provide a reference for the next stage, which is to measure the positive-going and negative-going peaks of the signal.

The attack and decay times used in this 'peak detect' mode are such that a sufficiently accurate measurement can be made within 16 symbols of a '+3 +3 -3 -3 . . .' pattern (i.e the Symbol-Sync sequence) to allow the Symbol-Clock Extraction circuits to operate.

Once the symbol-clock extraction circuits have detected the presence of a sufficiently coherent signal then, provided that the LEVRES bits of the Control Register have been set to the 'Peak Averaging' setting or 'Hold', this measurement will cease after 16 symbol-times, and the final values kept; otherwise the circuits will continue in the 'Peak Averaging' mode.

Acquire Symbol Clock (AQSC) Command Register

The Acquire Symbol Clock (AQSC) sequence follows a similar pattern; starting with a very fast initial estimate of the received symbol timing, then reducing the bandwidth of the Phase Locked Loop as a coherent signal is detected until the limit reached by the (Control Register) PLLBW bits is reached.

A μ Controller is able to detect the received carrier and therefore knows when to issue the AQSC and AQLEV commands. Note that due to a delay through the RRC filter, the AQSC and AQLEV sequences should not be started until about 8-symbol times after the RX carrier has been detected at the discriminator output.

In a system where the controlling μ Controller is not able to detect the RX carrier, the AQSC and AQLEV sequences may be started at any time; possibly when no carrier is being received. However in this case the clock and level acquisition operation will take longer as the circuits will have to recover from the change from a large amplitude noise signal at the output of the frequency discriminator to the wanted signal, probably with a dc offset. In this type of system the time between the turn-on of the transmitter and the start of the Frame Sync pattern should be extended -preferably by extending the Symbol Sync sequence to 32 or even 48 symbols.

Note that the clock extraction circuits work by detecting the timing of changes between opposite polarity symbols, i.e. a change from '+3' to '-3' or '-1' to '+1'. They will eventually fail if only 1 symbol is transmitted continuously. Similarly, the level measuring circuits require '+3' and '-3' symbols to be received at reasonably frequent intervals.

LEVRES Peak Detect and Peak Averaging

**Further information on this subject is currently
unavailable in this "Advance Information"
Document**

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref $V_{SS}=0V$)	-0.3 to ($V_{DD} + 0.3V$)
Sink/Source Current (supply pins)	$\pm 30mA$
(other pins)	$\pm 20mA$
Total Device Dissipation (@ $T_{AMB}=25^{\circ}C$)	800mW max.
Derating	10 mW/ $^{\circ}C$
Operating Temperature	-40 $^{\circ}C$ to +85 $^{\circ}C$
Storage Temperature	-55 $^{\circ}C$ to +125 $^{\circ}C$

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

$$V_{DD} = 5.0V$$

$$T_{AMB} = 25^{\circ}C$$

Symbol Rate = 4800 symbols/sec

Xtal/Clock = 4.9152 MHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	-	5.5	V
Supply Current (powersaved)	1	-	1.0	1.5	mA
Supply Current (not powersaved)	1	-	11.0	16.0	mA
Symbol Rate		2400	-	9600	symbols/sec
TX Output					
Impedance (not powersaved)	2	-	1.0	2.5	k Ω
Impedance (powersaved)	2	-	500	-	k Ω
Signal Level	3	0.8	1.0	1.2	Vp-p
RX Input					
Impedance (RX In pin)			10.0	-	M Ω
RX Input Amp Voltage Gain			500	-	V/V
Input Signal Level	4	0.7	1.0	1.3	Vp-p
Input dc Offset (wrt $V_{DD}/2$)	4	-0.5		0.5	V
Xtal/Clock Input					
'High' pulse width	5	40.0			ns
'Low' pulse width	5	40.0	-		ns
Input Impedance		10.0	-		M Ω
Inverter Gain (I/P = 1mV rms @ 1kHz)		20.0	-		dB
Xtal/Clock Frequency		2.0	-	10.0	MHz
μController Interface					
Input logic '1' level	6, 7	$V_{DD} - 1.5$	-	-	V
Input Logic '0' level	6, 7	-	-	1.5	V
Input Leakage Current ($V_{IN} = 0V$ to V_{DD})	6, 7	-5.0		+5.0	μA
Input Capacitance	6, 7	-	10.0		pF
Output Logic '1' Level ($I_{OH} = 120\mu A$)	7	$V_{DD} - 0.4$			V
Output Logic '0' Level ($I_{OL} = 360\mu A$)	7, 8	-	-	0.4	V
'Off' State Leakage Current ($V = V_{DD}$)	8	-	-	10	μA

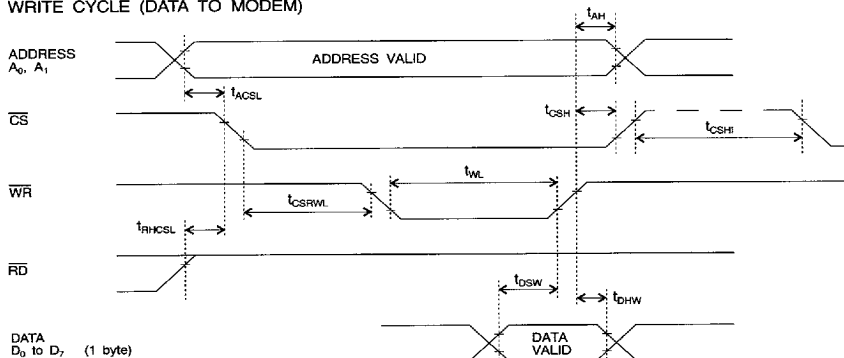
Specifications

Modem Read/Write Load Timing

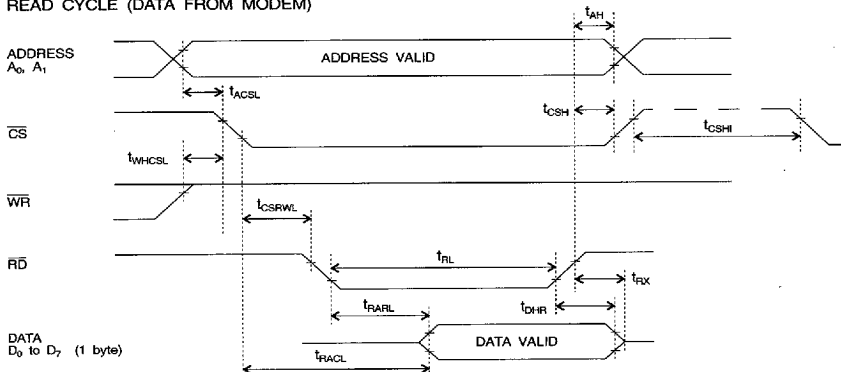
Conditions: $V_{DD} = 4.5$ to $5.5V$; $T_{OP} = -40^{\circ}C$ to $+85^{\circ}C$; with a maximum load of $30pF$ to V_{SS} on pins D_0 to D_7 .

Description	Note	Min.	Typ.	Max.	Unit
t_{ACSL} "Address Valid" to "CS Low" time		0	-	-	ns
t_{AH} "Address Hold" time		0	-	-	ns
t_{CSH} "CS Hold" time		0	-	-	ns
t_{CSH1} "CS High" time		6.0	-	-	Xtal/Clock Cycles
t_{CSRWL} "CS" to "WR" or "RD" Low time		0	-	-	ns
t_{DHR} "Read-Data Hold" time		0	-	-	ns
t_{DHW} Write-Data Hold time		0	-	-	ns
t_{DSW} Write-Data Set-Up time		90.0	-	-	ns
t_{RHCSL} "RD High" to "CS Low" time (write cycle)		0	-	-	ns
t_{RACL} "Read Access" time from "CS Low"		-	-	175	ns
t_{RARL} "Read Access" time from "RD Low"		-	-	145	ns
t_{RL} "RD" Low time		200	-	-	ns
t_{RX} "RD High" to " D_0 - D_7 3-State" time		-	-	50.0	ns
t_{WHCSL} "WR High" to "CS Low" time (read cycle)		0	-	-	ns
t_{WL} "WR" Low time		200	-	-	ns

WRITE CYCLE (DATA TO MODEM)



READ CYCLE (DATA FROM MODEM)

Figure 26 - MX919/929 - μ Processor Read/Write Timing

Specification Notes:

1. $V_{DD} = 5.0V$, $T_{OP} = 25^{\circ}C$; not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance (dynamic measurement) at 1kHz.
3. Measured after the external CR filter, for a '+3 +3 -3 -3 +3 -3 -3 ...' symbol sequence; at $V_{DD} = 5.0V$ (output level is proportional to V_{DD}).
4. For optimum performance, measured at the RX Feedback pin, for a '+3 +3 -3 -3 +3 +3 -3 -3 ...' symbol sequence.
5. Timing for an external input to the Xtal/Clock pin.
6. WR , RD , CS , A_0 and A_1 pins.
7. D_0 - D_7 pins.
8. IRQ pin.

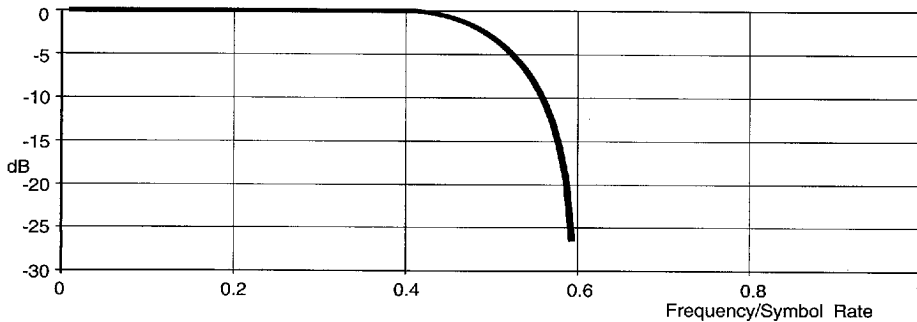


Figure 27 - RRC Filter Response

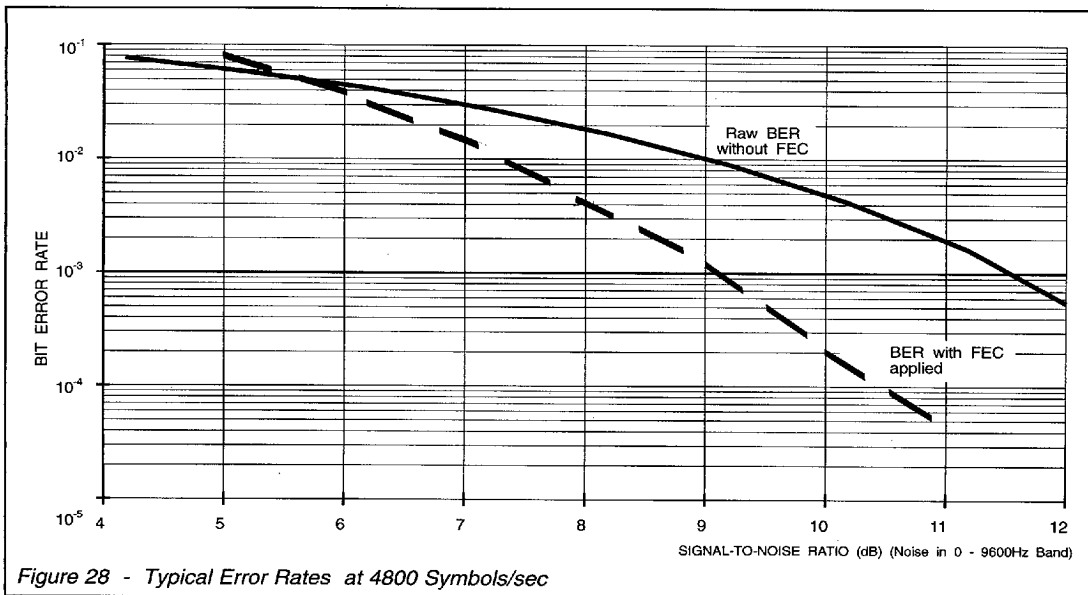
Signal-to-Noise Performance

Figure 28 - Typical Error Rates at 4800 Symbols/sec