MV6639

POCSAG DECODER

(Supersedes November 1992 edition - DS2464 - 3.3)

The MV6639 POCSAG decoder is capable of operating at 512 or 1200 baud. This device together with a suitable receiver, provides the major components for a POCSAG pager.

POCSAG is the acronym for Post Office Code Standardisation Advisory Group. The POCSAG code is the most accepted radio paging standard, (CCIR RPC No.1) and provides for over 2 million pager IDs, two of which may be held in this device. The POCSAG code format is shown in figure 3.

The design is optimised for very low power, low voltage use. Advanced features allow the decoder to be used in a wide range of applications.

The pinout and architecture are shown in figures 1 and 2.

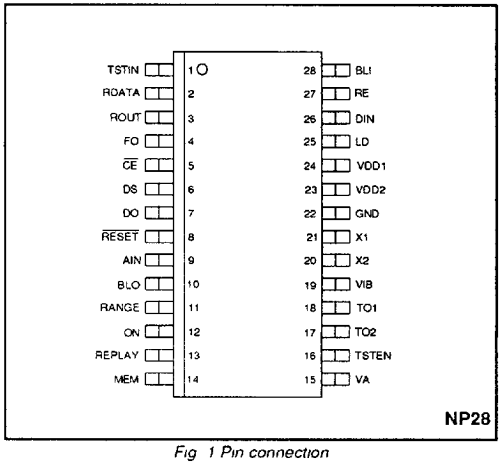


Fig 1 Pin connection
(top view - not to scale)

FEATURES

- Low voltage supply (1V min, 3.5V max)
- Low current consumption (Typically 15μA)
- Voltage doubler for radio receiver or μP and Display
- True 2 bit CRC error correction
- Tone only and/or messaging pager at 512 or 1200 baud using a single 32768Hz crystal
- Silent call storage
- Directly drives tone transducer
- Programmable tone generator output frequency (2048 or 2731 Hz)
- Interface to SL6609 radio receiver chip
- Low battery alert

APPLICATIONS

- Wrist watch pager
- Message display pager
- Tone only pager
- Data receivers

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD2 - GND)	-0.5V to 5V
Voltage on any pin	-0.3V to VDD2 + 0.3V
Operating temperature	-20°C to + 70°C
Storage temperature	-55°C to +125°C

ORDERING INFORMATION

MV6639/KG/NPDS - devices in anti-static sticks
MV6639/KG/NPDE - devices in tape & reel

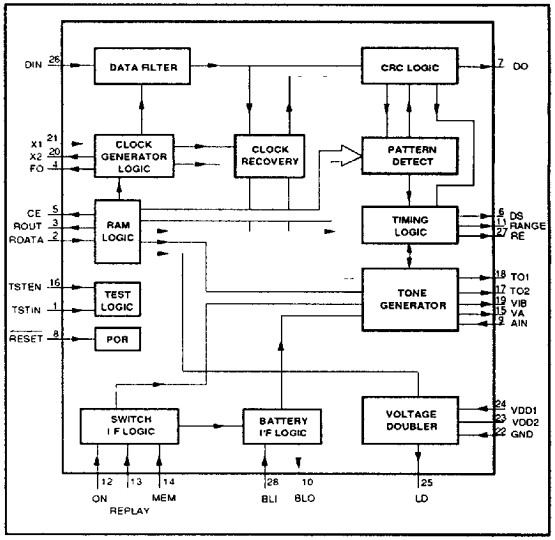


Fig 2 MV6639 Block Diagram

Pin Description.

Pin No	Pin Name	Pin Description
1	TSTIN	Test input Held low for normal operation
2	RDATA	Data input from external E²PROM
3	ROUT	Reset to external E²PROM
4	FO	Crystal frequency divided by two clock output. Mainly used for reading data from an external E²PROM into the internal memory
5	$\overline{CE}$	Chip enable signal for external E²PROM
6	DS	Data Strobe. This output goes active high prior to each bit of valid message data being transmitted on DO
7	DO	Data Output Valid address and message data is output on this pin
8	$\overline{RESET}$	This pin is used to activate the power on reset circuit A capacitor between this pin and GND sets the reset time when powered up. The device may also be externally reset from this input
9	AIN	Alert in One of two inputs to the tone generator circuit This input when high produces a continuous tone at the two tone outputs
10	BLO	Battery level output This goes high if battery level input (BLI) is high for 8ms
11	RANGE	If no preamble or sync word is detected for 60 batches, the range output goes high.
12	ON	Decoder is switched 'ON' by holding this pin high.
13	REPLAY	Pulsed high to cancel tones or replay calls
14	MEM	Decoder is switched to 'MEM' (memory or 'silent' mode) by holding this pin high
15	VA	Visual alert Pulses high to indicate incoming call when in silent mode Can be used to drive an LED
16	TSTEN	Test input active high Hold low during normal operation
17	TO2	The beep codes and alerts are output on this pin The output configuration and tone output frequencies are programmable
18	TO1	The beep codes and alerts are output on this pin The output configuration and tone output frequencies are programmable
19	VIB	Output to external bipolar vibrator driver when in silent mode
20	X2	Crystal oscillator output
21	X1	Crystal oscillator input
22	GND	Negative supply input
23	VDD2	Positive supply, doubled if voltage doubler active, otherwise connected to VDD1
24	VDD1	Positive supply input (1V min)
25	LD	Connect external inductor and diode for voltage doubler if required
26	DIN	This is the serial data input to the device 512 or 1200 baud non-inverted POCSAG data.
27	RE	Receiver Enable This output when low powers down or disables the receiver to save power
28	BLI	Battery level input from receiver Normally low The high level indicates battery flat and triggers a tone if high for 8ms

DECODER APPLICATIONS

The MV6639 can be used in either a "Tone Only" or a "Tone and Message" pager. When used in tone only applications, the only additional IC requirements are a receiver (such as the SL6609) and a small E²PROM (primarily for holding the pager identification). A full tone and message pager can be implemented with the addition of a simple microprocessor/LCD driver.

THE POCSAG CODE

A transmission of POCSAG code consists of at least 576 bits of preamble, i.e. alternate 1010s, followed by batches of codewords, each batch starting with a synchronisation codeword (SC) followed by 8 frames of data. (see figure 3a).

Each frame consists of 2 codewords, where the pager ID's 3 least significant bits correspond to the frame number in the batch.

Each codeword consists of 32 bits as shown in figure 3b. There are two types of codeword, address and message.

The SC and IC are special cases of address codewords. Bits 20-21 of the address codeword transmitted determine the tone cadence pattern to be output by the decoder.

Message codewords immediately follow their particular address and are only displaced by the SC. An idle codeword (IC) is transmitted in the absence of an address or message codeword. In a message sequence, the end of the message is denoted by another address or idle codeword.

The format of message data output by the decoder is shown in figure 3d.

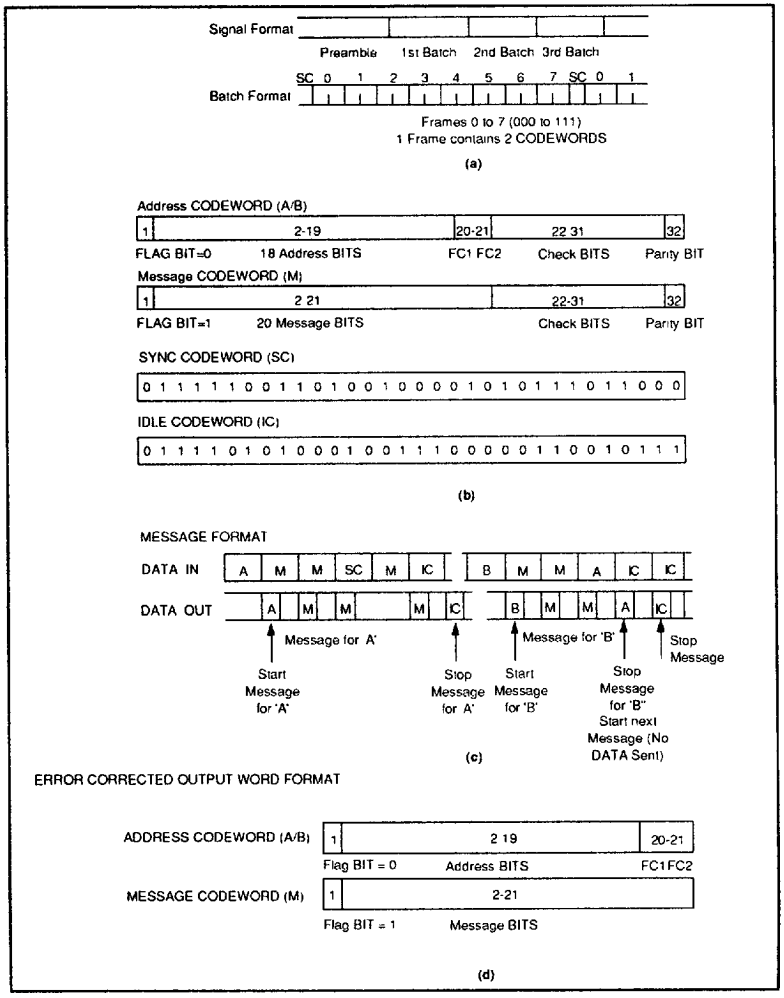


Fig 3 POCSAG Data Format

POCSAG CODE SYNCHRONISATION

After the decoder has been powered up and the 2 ID's programmed, synchronisation to the incoming POCSAG data is performed. Once bit synchronisation is achieved by the clock recovery circuit, the data stream is checked bitwise for the sync codeword (SC).

When the SC is found, the receiver is disabled until the frame in which either of the two ID's occurs. The receiver (RX), is then turned on to look for an ID and any valid message is decoded.

If SC is not found, a search procedure is initiated. The receiver is enabled for one frame in 9 to search for either SC or preamble. If, after 60 such search cycles, SC or preamble have not been detected, the out of range (RANGE) signal goes active high. RANGE is reset if SC or preamble is detected or the decoder is switched to STANDBY.

DESCRIPTION OF DECODER CIRCUITS

CLOCK GENERATOR LOGIC

Most of the required clock signals for the chip are produced by the clock generator circuit, from the 32768Hz crystal controlled oscillator. These are as follows:-

32.768 kHz for clock recovery
16.384 kHz clock ref. output (FO)
2048/2731 Hz (programmble) for the tone generator
16 Hz to control tone cadencing

Clocks will be disabled as required depending on the mode of operation of the device.

An external clock may be applied to X1 if X2 is left open circuit. Note that X1 has non-standard input thresholds.

CLOCK RECOVERY

The clock recovery circuit produces a clock signal correctly synchronised to the incoming data. The circuit is similar in operation to a digital phase locked loop. This circuit together with the timing logic monitors and maintains bit sync.

DATA FILTER

The data filter digitally cleans up the incoming data as shown in figure 4 and works with the clock recovery circuit to synchronise the internal clocks to the incoming data. The circuits minimise the effects of edge jitter and "drop-outs" in the data, which can occur at low signal levels.

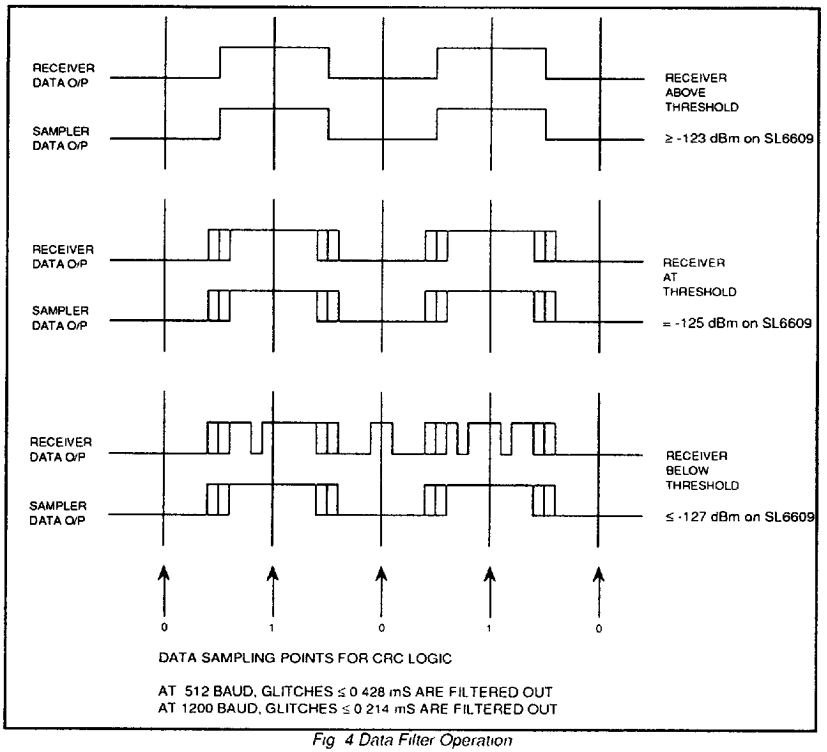


Fig 4 Data Filter Operation

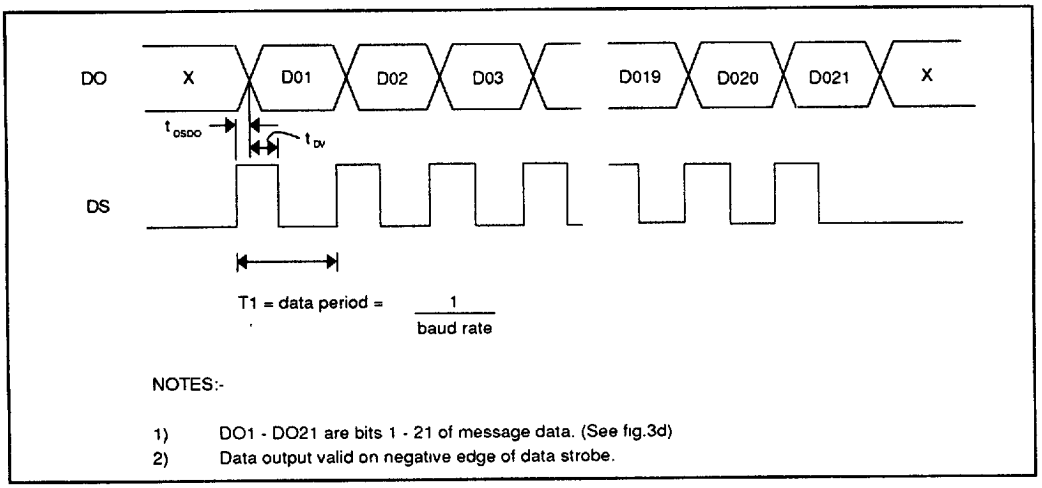


Fig 5 Data Output Timing

CRC LOGIC

This circuit receives the incoming serial data and performs 2 bit CRC error correction according to the POCSAG standard on all incoming data. Together with the timing logic and pattern detector, this circuit maintains word sync and outputs corrected message data clocked on a positive edge of data strobe (DS) as shown in figure 5. If more than two errors are detected, no attempt is made at corrections and the data is outputed uncorrected with no indication of error.

PATTERN DETECTOR

This circuit operates on checked and corrected data. It receives data and checks for SC, IC or either of the two programmed pager addresses.

TIMING LOGIC

This logic provides the bit, word and batch frame sync in conjunction with the pattern detector, CRC logic and clock recovery circuit. The timing logic also generates the receiver enable (RE), data strobe (DS) and out-of-range (RANGE), output signals. RE goes active one word at 1200 baud, half word at 512 baud, before the address is expected to allow time for the receiver to power up.

RAM LOGIC

The RAM stores 48 control bits which are automatically read from an external E²PROM on power up. The first 18 bits are address A (A0-17) which is read in LSB first. This is followed by 3 frame position bits (AF2-0) which tell the device which frame to look in for address A. These are read in MSB first. These values are followed by address B and its frame position bits. The last 6 bits are function bits which are used to configure the device. FB1 is read first. If addresses are expected in only one particular frame, the AF and BF bits should be set to the same value to conserve power. The function bits are used for programming silent override of selected pager ID's, 512/1200 baud operation, voltage doubler enable/disable and tone generator operation. Figure 6 shows the function bit allocation. The decoder RAM and E²PROM timing is shown in figure 7.

	Function Bit		Feature
FB 1	Data rate select	0:	1200 baud.
		1:	512 baud.
FB 2	Voltage Doubler	0:	Disabled.
		1:	Enabled.
FB 3	Silent Override on addr 'A'.	0:	Enabled.
		1:	Disabled.
FB 4	Silent Override on addr 'B'.	0:	Enabled.
		1:	Disabled.
FB 5	Tone Gen Freq	0:	2048Hz
		1:	2731Hz
FB 6	Tone output configuration	0:	Two Tone Levels
		1:	Single Tone Level

Fig 6 Function BIT Allocation

Fig. 7a. Power Up Sequence

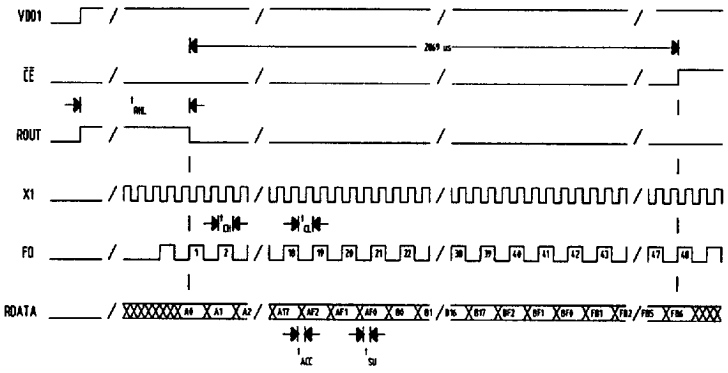
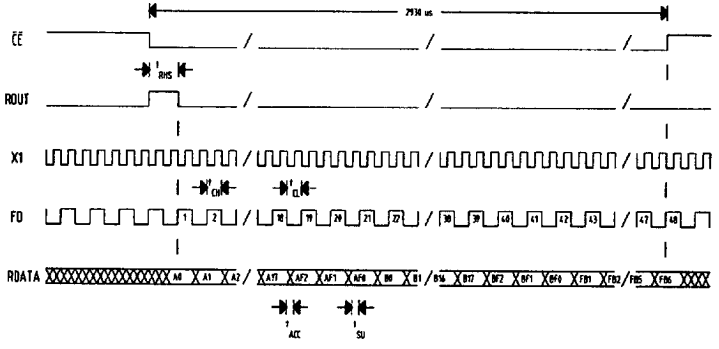


Fig. 7b. Sequence During Refresh or Status Change



N.B. X1 is an "idealized" representation of the signal, if the on board oscillator is used then the signal will be more like a sawtooth waveform than a logic signal

Represents "Don't Care" signal may be high, low or changing

Fig 7 E²PROM Read Operation

On power up, a reset pulse is generated from the charging of a capacitor connected to the decoder $\overline{\text{RESET}}$ pin. This pulse sets the decoder in a defined state and initiates the loading of the E²PROM contents into the decoder's internal memory. The reset pulse ROUT is high for approximately 3 seconds. This extended period is to allow the on chip voltage doubler (if enabled) to attain its correct doubled output voltage. The E²PROM used may only operate down to a minimum supply of 2V, thus any attempt to read data from the memory before this voltage is available from the doubler may result in corrupt data being loaded into the decoder. Even an E²PROM operating down to 1V supply could give a faulty read output if the ROUT hold off pulse is short as the limited voltage out of the doubler at power up is below VDD1 (battery) voltage. Fig.7a shows the E²PROM read operation for the power up sequence. CE is low and a reset pulse is output to the external memory device. Then data is clocked into the MV6639 on positive edges of the 16384 Hz output pin 'FO'. After 48 bits have been written into chip memory,CE goes high to disable the external memory and the programming sequence is terminated.

Mechanical shock can cause a temporary disconnection of the pager power supply. To guard against the decoder RAM contents being corrupted, the RAM is automatically reloaded every four minutes. If the pager is receiving at the 4 minute refresh time, the reload is delayed until the receiver is disabled. In addition, a reload operation is performed whenever the status of the decoder is switched from STANDBY to ON or MEM modes.

For the automatic and change of status reloads, the doubler (if enabled) will already have achieved its correct output voltage and it is unneccessary to provide a long holdoff ROUT pulse to the E²PROM. The memory read sequence for the 4 minute refresh or status change is shown in Fig.7b.

BATTERY INTERFACE LOGIC

The decoder will accept a 'battery low' flag from a radio receiver on the BLI pin. The decoder samples the state of this pin at 256 Hz when the receiver is enabled, as shown in figure 8. The tone generator will output a 16 second continuous signal if BLI input is high (battery fail condition) for 3 or more consecutive samples. In addition, a battery low flag is output on the BLO pin. Note that any active tone generator and BLO output can be cancelled by pulsing the REPLAY/CANCEL input pin. The low battery detection circuit will be re-armed whenever decoder status is changed from STANDBY to ON or MEM.

TEST LOGIC

Test logic is included as required to supplement the inherent testability and fault coverage of the device during manufacture.

POWER ON/OFF AND SWITCH INTERFACE LOGIC

There are three operating modes for the decoder, STANDBY, ON and MEM (memory). When the decoder is required to be OFF it is preferable to disconnect the battery supply to the decoder, as shown in figure 14, to conserve battery power. If STANDBY mode is used the crystal oscillator and voltage doubler (if programmed ON) continue to operate but FO output is disabled.

MEM or 'Silent' mode is selected if the user wishes to store incoming calls rather than producing alert tones immediately the pager recognises a valid address. MEM mode is activated with a logic '1' on the MEM pin. The tone outputs TO1, TO2 are inhibited and the vibrator (VIB) and Visual Alert (VA) outputs enabled. The silent mode can be overriden on either address A or B by setting the appropriate silent overide bit read into the internal RAM (see figure 6). In the MEM mode up to four incoming calls can be stored.

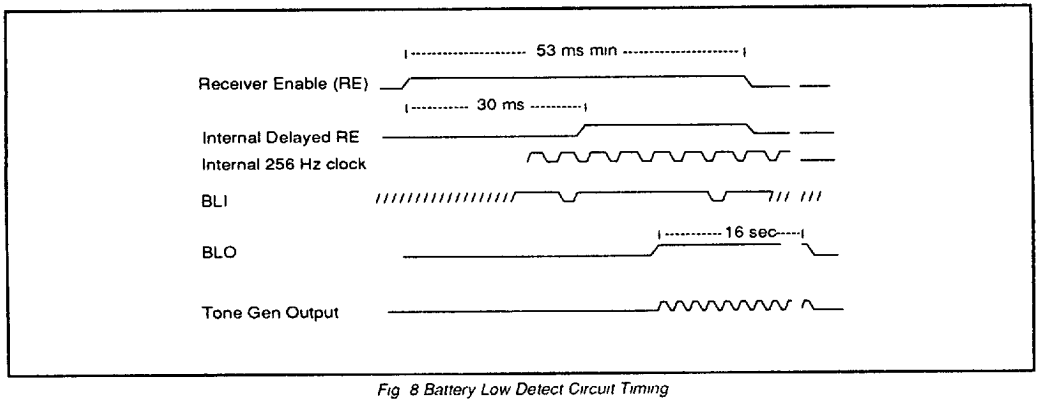


Fig 8 Battery Low Detect Circuit Timing

The Switch Interface logic truth table is shown in figure 9 below:

ON	MEM	REPLAY	Decoder Status
0	0	0	Decoder off. No messages received. (STANDBY mode)
1	0	0	Decoder active Messages received and decoded. (ON mode)
X	1	0	Decoder active and in silent / store call mode. (MEM mode)
1	0	⎍	Replay stored calls / cancel current tones.
X	1	⎍	Cancel current tones or Vibrator and Visual Alert outputs

Fig. 9 Decoder Status Truth Table

In ON mode pulsing REPLAY to a logic '1' replays stored call(s). Pulsing the REPLAY input will also cancel any current tone, vibrator or visual alert outputs.

Further details on the MEM and REPLAY tone vibrator and visual alert output cadences are covered in the next section.

Different tone patterns are generated when changing the status of the pager (eg from 'ON' to 'MEM'). These too are covered in the tone generation section.

Contact debouce circuitry is included in all switch and push button interfaces.

TONE VIBRATOR AND VISIBLE ALERT SIGNAL GENERATION

The tone generator block produces audio or low frequency vibrator signals in response to the state of the pager, messages, or battery level (if low). Four paging tone cadence patterns are provided and also the ability to output a continuous alert tone. Two volume levels are available and the tone generator frequency and output drive configuration is programmable.

TONE AND VIBRATOR GENERATOR OUTPUT CONFIGURATION

The internal tone generator circuit feeds an external beeper via the TO1 and TO2 pins. Figures 10 (a) and (b) show the two common methods of beeper interface. Fig 10 (a) shows a high efficiency resonant drive circuit with one fixed volume level. In this configuration the TO1 and TO2 outputs are push - pull, switching in anti - phase. Fig 10 (b) shows a more flexible drive network which delivers two different power levels to the transducer. This mode is selected by clearing bit 6 of the function register low (Figure 6). When an alert tone is output, TO2 stays low for the first six seconds and TO1 switches in accordance with the cadence pattern, producing a low level tone. For the next ten seconds TO2 also switches, producing a high tone level.

The vibrator output VIB drives an external bipolar transistor with vibrator alerter as shown in figure10(c).

TONE FREQUENCY

This can be customer specified at either 2048Hz or 2731Hz. The control bit FB5 which determines which frequency is used, is set in the external E²PROM and read into the decoder memory (see figure 6).

PAGING TONE CADENCES

Four different paging tone cadence patterns are available and these are shown in Figure 12. The particular cadence output is determined by the FC1 and FC2 bits which form part of the address codeword (Figure 3).

ALERT OVERIDE TONE

Direct input of cadence patterns is possible via the AIN pin. A high input on this pin will gate the selected tone frequency to the TO1 and TO2 outputs. Both TO1 and TO2 outputs are active when AIN is high and function register bit 6 is set high, to deliver maximum power to the external beeper.

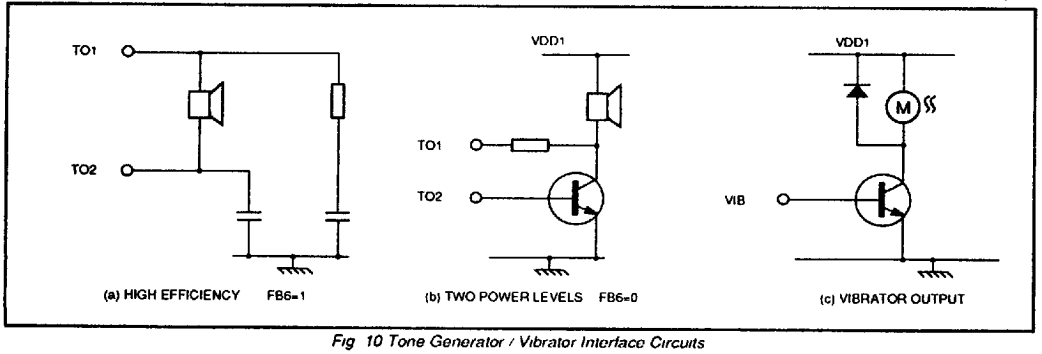


Fig 10 Tone Generator / Vibrator Interface Circuits

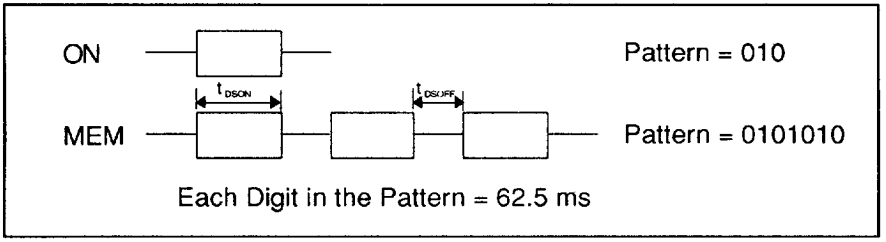


Fig 11 Decoder Status Tones

PAGER STATUS TONE GENERATION

The decoder produces tones to acknowledge a change in its status. When ON is selected the decoder will output a single short tone as shown in figure 11. In the ON, (or active) mode the decoder is able to receive and decode messages. Received calls are compared with the two user addresses assigned to the pager These are programmed into the external E²PROM and read into the decoders internal memory.

Setting the decoder to the MEM (or SILENT) state is indicated by three short tones. This operating mode is similar to the ON condition except that audio alert tones (cadences) are inhibited. Instead, the external vibrator alerter is activated by providing an 8Hz drive signal out of the VIB pin (see figure 10). A visible alert can be generated by feeding the VA output into the external buffer transistor and LED. VA is pulsed high as shown in figure 13. Up to four alert cadence calls can be stored in the decoder and these calls can be successively replayed by switching from MEM to ON and supplying pulses to the REPLAY input. When the vibrator output is active after receiving a message in the MEM mode, the device can be switched to ON mode to hear the remainder of the 16 second tone The tone is also stored for REPLAY at a more convenient time Pulsing REPLAY before the 16 second tone cadence has been completed will automatically cancel the current tone and replay the next tone as shown in figure 13 Whatever the pager status, a tone output, vibrator or visible alert can be cancelled by pulsing the REPLAY input.

Priority messages can be programmed to overide the silent mode. Two of the six 'Function bits' (figure 6) programmed into the external E²PROM, control the silent overide for address A and B

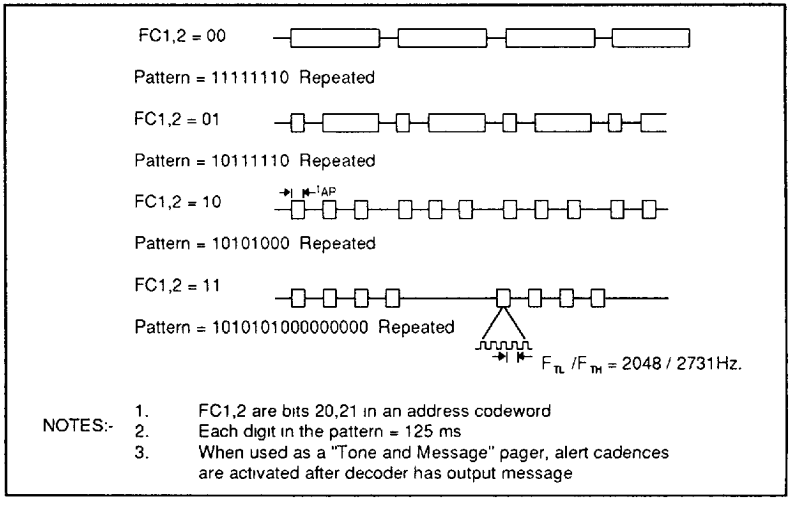


Fig 12 Alert Cadences

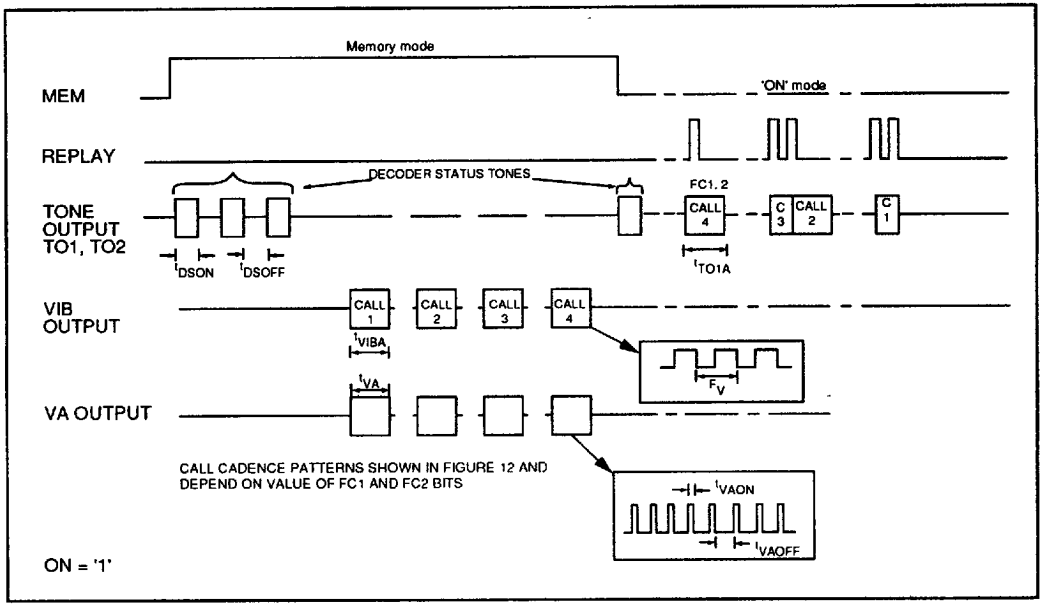


Fig 13 Recall / Cancel of Stored Calls

VOLTAGE DOUBLER

The decoder is capable of operating with a supply between 1 and 3.5V. Other devices in the pager, for example the receiver, may require a higher voltage than 1V. The voltage doubler enables these devices to be used without additional circuitry.

The voltage conversion is performed by charging an inductor, then discharging it through a diode onto a reservoir capacitor on the output. To maximise the efficiency the resistance of the inductor and the forward voltage drop of the diode should be as low as possible. The diode should therefore be a schottky diode. The inductor used in the test and evaluation circuits has a DC resistance of less than 20 ohms.

The voltage on VDD2 should not exceed 3.5V, so VDD1 should be less than 1.75V if the doubler is enabled. If the doubler is not used VDD1 and VDD2 should be shorted together and the LD pin left open circuit.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 1V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler disabled. VDD2 = VDD1

Parameters	Symbol	Min	Typ	Max	Units	Comments
SUPPLY CURRENT						
Decoder on	I_{VDD}		10	14	µA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	0.90			V	
BLI, DIN	V_{IH}	0.70			V	
NRESET	V_{IH}	0.90			V	
X1	V_{IH}	0.90			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0.20	V	
BLI, DIN	V_{IL}			0.30	V	
NRESET	V_{IL}			0.30	V	
X1	V_{IL}			0.20	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}		0.01	1	µA	Note 1. $V_{IH} = V_{VDD1}$
AIN, NRESET	I_{IH}		0.13	1	µA	Note 1. $V_{IH} = V_{VDD1}$
BLI, DIN, RDATA, X1	I_{ILH}		0.01	1	µA	$V_{IH} = V_{VDD1}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}		-0.01	-1	µA	$V_{IL} = 0V$
NRESET	I_{IL}		-5.48	-10	µA	$V_{IL} = 0V$ internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	0.90	0.99		V	$I_{LOAD} = 10µA$
TO1, TO2, VIB	V_{OH}	0.90	0.98		V	$I_{LOAD} = 10µA$
OUTPUT LEVELS LOW						
All outputs	V_{OL}		0.03	0.10	V	$I_{LOAD} = -10µA$
OUTPUT CURRENTS LOW						
TO1	I_{OL}	1.50			mA	$V_{OUT} = {}^{VDD1}/_{2}$
TO2, VIB, VA	I_{OL}	0.30			mA	$V_{OUT} = {}^{VDD1}/_{2}$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB	I_{OH}	0 30			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VA	I_{OH}	0.20			mA	$V_{OUT} = {}^{VDD1}/_{2}$

NOTES
1. These inputs have internal pullup or pulldown resistors

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 1.5V. Tamb = -20 to +70°C. All outputs open circuit Voltage doubler disabled VDD2 = VDD1

Parameters	Symbol	Min	Typ	Max	Units	Comments
SUPPLY CURRENT						
Decoder on	I_{VDD}		14	22	µA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	1 2			V	
BLI, DIN	V_{IH}	1 0			V	
NRESET	V_{IH}	1 2			V	
X1	V_{IH}	0 9			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0 3	V	
BLI, DIN	V_{IL}			0.5	V	
NRESET	V_{IL}			0.5	V	
X1	V_{IL}			0.2	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}		0 01	1	µA	Note 1. $V_{IH} = V_{VDD1}$
AIN, NRESET	I_{IH}		0 6	5	µA	Note 1. $V_{IH} = V_{VDD1}$
BLI, DIN, RDATA, X1	I_{ILH}		0 01	1	µA	$V_{IH} = V_{VDD1}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}		0 01	-1	µA	$V_{IL} = 0V$
NRESET	I_{IL}		-20	-40	µA	$V_{IL} = 0V$ internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	1 3	1 5		V	$I_{LOAD} = 10µA$
TO1, TO2, VIB	V_{OH}	1.3	1 5		V	$I_{LOAD} = 10µA$
OUTPUT LEVELS LOW						
All outputs	V_{OL}		0 03	0.15	V	$I_{LOAD} = -10µA$
OUTPUT CURRENTS LOW						
TO1	I_{OL}	5			mA	$V_{OUT} = V_{DD1}/_2$
TO2, VIB, VA	I_{OL}	1			mA	$V_{OUT} = V_{DD1}/_2$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB	I_{OH}	1.5			mA	$V_{OUT} = V_{DD1}/_2$
VA	I_{OH}	1			mA	$V_{OUT} = V_{DD1}/_2$

NOTES
1 These inputs have internal pullup or pulldown resistors

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 3.5V. Tamb = -20 to +70°C. All outputs open circuit Voltage doubler disabled. VDD2 = VDD1

Parameters	Symbol	Min	Typ	Max	Units	Comments
SUPPLY CURRENT						
Decoder on	I_{VDD}		41	71	µA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	2 8			V	
BLI, DIN	V_{IH}	2 0			V	
NRESET	V_{IH}	3.0			V	
X1	V_{IH}	0.9			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0.8	V	
BLI, DIN	V_{IL}			1.2	V	
NRESET	V_{IL}			1.5	V	
X1	V_{IL}			0.2	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}		0.1	1	µA	Note 1. $V_{IH} = V_{VDD1}$
TSTIN, TSTEN, AIN, NRESET	I_{IH}		5.5	10	µA	Note 1. $V_{IH} = V_{VDD1}$
BLI, DIN, RDATA, X1	I_{ILH}		0 05	1	µA	$V_{IH} = V_{VDD1}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}		-0 05	-1	µA	V_{IL} = 0V
NRESET	I_{IL}		-180	-300	µA	V_{IL} = 0V internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	3 2	3 5		V	I_{LOAD} = 10µA
TO1, TO2, VIB	V_{OH}	3 2	3 4		V	I_{LOAD} = 10µA
OUTPUT LEVELS LOW						
All outputs	V_{OL}		0 05	0.3	V	I_{LOAD} = -10µA
OUTPUT CURRENTS LOW						
TO1	I_{OL}	10			mA	$V_{OUT} = V_{DD1}/2$
TO2, VIB, VA	I_{OL}	2			mA	$V_{OUT} = V_{DD1}/2$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB	I_{OH}	2			mA	$V_{OUT} = V_{DD1}/2$
VA	I_{OH}	1			mA	$V_{OUT} = V_{DD1}/2$

NOTES
1 These inputs have internal pullup or pulldown resistors

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 1V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler ON.

Parameters	Symbol	Min	Typ	Max	Units	Comments
VOLTAGE DOUBLER						
VDD2 (Doubled Voltage) no ext. load	V_{VDD2}		1 95		V	
VDD2 (Doubled Voltage) 1.2mA ext. load	V_{VDD2}	1 80			V	
Max external load at VDD2 = 1.8 x VDD1	I_{VDD1}	1.20			mA	
SUPPLY CURRENT						
Decoder	I_{VDD1}			143	µA	
Decoder 1.2mA ext. doubler load	I_{VDD1}			4.1	mA	
Decoder Max ext. doubler load	I_{VDD1}			5.4	mA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	V_{VDD2}-0.4			V	
BLI, DIN	V_{IH}	V_{VDD2}-0.5			V	
NRESET	V_{IH}	V_{VDD2}-0.3			V	
X1	V_{IH}	1 0			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0.4	V	
BLI, DIN	V_{IL}			0.6	V	
NRESET	V_{IL}			0.5	V	
X1	V_{IL}			0.2	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}			1	µA	Note 1. $V_{IH} = V_{VDD2}$
AIN, NRESET	I_{IH}			6	µA	Note 1. $V_{IH} = V_{VDD2}$
BLI, DIN, RDATA, X1	I_{ILH}			1	µA	$V_{IH} = V_{VDD2}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}			-1	µA	V_{IL} = 0V
NRESET	I_{IL}			-150	µA	V_{IL} = 0V, internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	V_{VDD2}-0 2			V	I_{LOAD} = 10µA
TO1, TO2, VIB	V_{OH}	0 9			V	I_{LOAD} = 10µA
OUTPUT LEVELS LOW						
All outputs	V_{OL}			0.20	V	I_{LOAD} = -10µA
OUTPUT CURRENTS LOW						
TO1	I_{OL}	7 0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
TO2, VIB, VA	I_{OL}	1 5			mA	$V_{OUT} = {}^{VDD1}/_{2}$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB (current source)	I_{OH}	1.2			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VA (current source)	I_{OH}	1.0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VOLTAGE DOUBLER FREQUENCY						
	F_{VD}	8	11	15	kHz	Note 3 VD Load = 0
	F_{VD}	44	68	108	kHz	Note 3 VD Load = 550µA
	F_{VD}	96	140	196	kHz	Note 3 VD Load = 1.2mA
	F_{VD}	130	166	214	kHz	Note 2, 3 VD Load = Max

NOTES
1. These inputs have internal pullup or pulldown resistors
2. VD Load = Max is load current such that VDD2 = 1 8 x VDD1
3. Not production tested

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 1.5V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler ON.

Parameters	Symbol	Min	Typ	Max	Units	Comments
VOLTAGE DOUBLER						
VDD2 (Doubled Voltage) no ext. load	V_{DD2}		2.90		V	
VDD2 (Doubled Voltage) 1.2mA ext. load	V_{DD2}	2.75			V	
Max external load at VDD2 = 1.8 x VDD1	I_{VDD1}	2.00			mA	
SUPPLY CURRENT						
Decoder	I_{VDD1}			240	µA	
Decoder 1.2mA ext. doubler load	I_{VDD1}			3.8	mA	
Decoder Max ext. doubler load	I_{VDD1}			8.6	mA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	V_{VDD2}-0.6			V	
BLI, DIN	V_{IH}	V_{VDD2}-0 8			V	
NRESET	V_{IH}	V_{VDD2}-0.4			V	
X1	V_{IH}	1 0			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0 60	V	
BLI, DIN	V_{IL}			0 80	V	
NRESET	V_{IL}			1.50	V	
X1	V_{IL}			0.20	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}			1	µA	Note 1. $V_{IH} = V_{VDD2}$
AIN, NRESET	I_{IH}			8	µA	Note 1. $V_{IH} = V_{VDD2}$
BLI, DIN, RDATA, X1	I_{ILH}			1	µA	$V_{IH} = V_{VDD2}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}			-1	µA	V_{IL} = 0V
NRESET	I_{IL}			-250	µA	V_{IL} = 0V, internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	V_{VDD2}-0 3			V	I_{LOAD} = 10µA
TO1, TO2, VIB	V_{OH}	1 35			V	I_{LOAD} = 10µA
OUTPUT LEVELS LOW						
All outputs	V_{OL}			0 30	V	I_{LOAD} = -10µA
OUTPUT CURRENTS LOW						
TO1	I_{OL}	10 0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
TO2, VIB, VA	I_{OL}	2 0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB (current source)	I_{OH}	2.0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VA (current source)	I_{OH}	1 0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VOLTAGE DOUBLER FREQUENCY						
	F_{VD}	8	11	17	kHz	Note 3 VD Load = 0
	F_{VD}	27	38	54	kHz	Note 3 VD Load = 550µA
	F_{VD}	56	77	116	kHz	Note 3 VD Load = 1.2mA
	F_{VD}	119	154	206	kHz	Note 2, 3 VD Load = Max

NOTES
1 These inputs have internal pullup or pulldown resistors
2 VD Load = Max is load current such that VDD2 = 1 8 x VDD1
3 Not production tested

AC ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1= 1 to 3.5V, VDD1 < = VDD2 < = 3.5V, Tamb = -20 to +70°C.

Parameters		Symbol	Min	Typ	Max	Units	Comments
Crystal Frequency		F_C		32768		Hz	
Freq Reference Output		F_O		16384		Hz	
SYSTEM INPUTS TO DECODER							
Input Data Rate	(Low Speed)	F_D		512		baud	Selectable
	(High Speed)			1200			See Fig 6
Preamble Time	(512 baud)	t_{PA}	1.125			s	
	(1200 baud)		0.48			s	
Batch Time	(512 baud)	t_B		1.0625		s	
	(1200 baud)			0.4533		s	
TONE GENERATOR							
Output Frequency		F_{TL}		2048		Hz	Selectable
		F_{TH}		2731		Hz	See Fig 6
Vibrator Output Freq.		F_V		8		Hz	Fig 13
Vibrator Alert Period		t_{VIBA}		16		s	Fig 13
Visible Alert Period		t_{VA}		16		s	Fig 13
Visible Alert LED ON time		t_{VAON}		0.25		s	Fig 13
Visible Alert LED OFF time		t_{VAOFF}		1.75		s	Fig 13
TO1 Alert Period		t_{TO1A}		16		s	Fig 13
TO2 Alert Period		t_{TO2A}		10		s	
TO1, TO2 Alert Pulse Time		t_{AP}		125		ms	Fig 12
Decoder Status TO1, TO2 on		t_{DSON}		62.5		ms	Fig 11
Decoder Status TO1, TO2 off		t_{DSOFF}		62.5		ms	Fig 11
REPLAY pulse width		t_{rep}	80			ms	
Decoder RAM / E²PROM Timing							
E²PROM Reset Pulse Rout		t_{RHL}		3		s	Fig 7, Note 1
E²PROM Reset Pulse Rout		t_{RHS}		61		µs	Fig 7, Note1
Clock High Level Time		t_{CH}		30.5		µs	Fig 7
Clock Low Level Time		t_{CL}		30 5		µs	Fig 7
E²PROM Access Time RDATA		t_{ACC}			20.5	µs	Fig 7
Data Setup Time RDATA		t_{SU}	10			µs	Fig 7
Data Strobe To Data Output Delay		t_{DSDO}			50	µs	Fig 5
Data Valid To Negative Strobe Edge		t_{DV}	783			µs	Fig 5
Power On $\overline{\text{RESET}}$ capacitor		C_{RS}		10		nF	
Voltage Doubler Output Ripple		V_D			1	mV p-p	Note 2

NOTES

1. A 3 second reset pulse is generated when power is applied to the MV6639. This allows time for the voltage doubler output (if enabled) to stabilise. A shorter (61µs) reset pulse is generated for the automatic 4 minute reload.
2. VDD2 decoupling capacitor 100µF. Output current 10µA - 1 2mA.

APPLICATION EXAMPLE: 1 VOLT PAGER SYSTEM

A typical 1 Volt pager system, suitable as a wrist watch application is shown in figures 14 & 15. Only 3 chips are required. GPS's SL6609 Direct Conversion Receiver, MV6639 POCSAG Decoder and a 1 Volt E²PROM (e g. EPSON SPM28C51).

Note that EPSON trades as SEKIO EPSON in Japan and S-MOS in Amercia.

A 32KHz watch crystal is used as the reference frequency to the decoder The SL6609 receives and demodulates the data, and monitors the battery voltage. The interface between the decoder and receiver consists of only 3 connections excluding the supplies.

The decoder voltage doubler output V_{VDD2} is available to power not only the receiver, but alternative higher voltage E²PROM and a microprocessor / LCD driver for a full tone and message pager

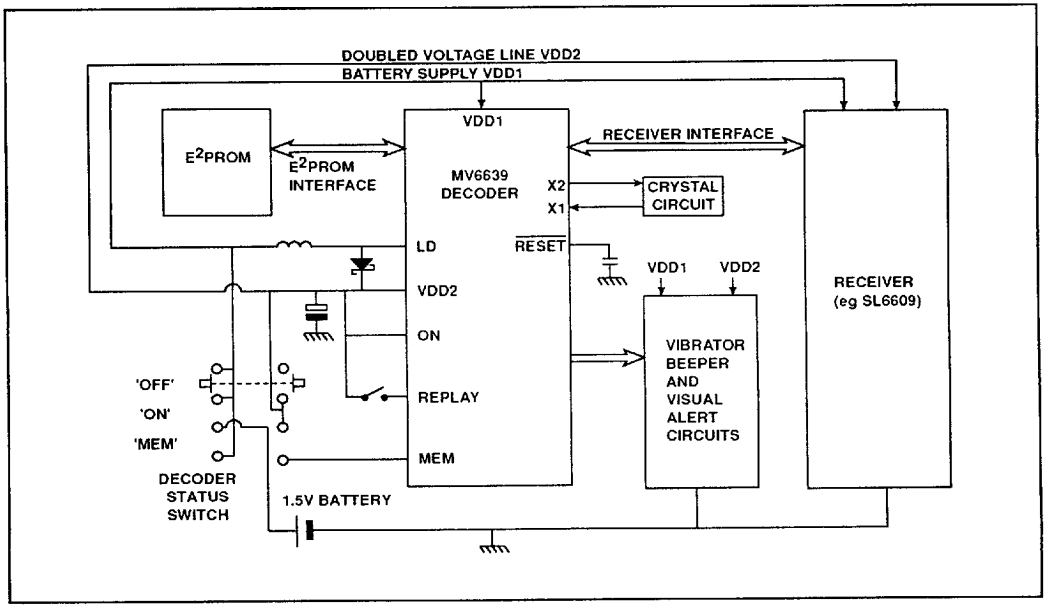


Fig 14 Tone Pager applications example showing interface with SL6609 receiver

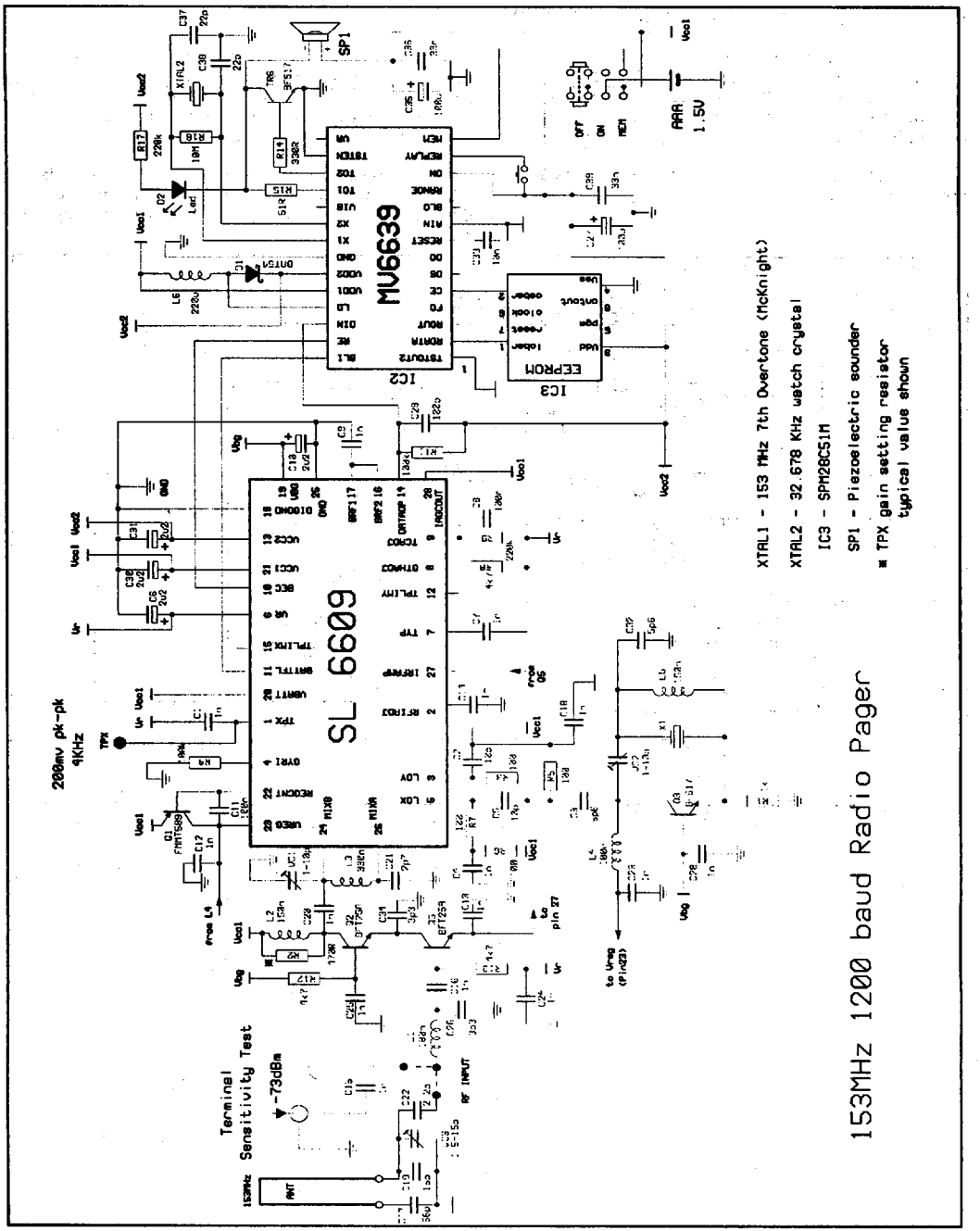


Fig.15

MV6639 DEMONSTRATION CIRCUIT

Fig.16 shows a simple demonstration circuit to allow the decoder to be evaulated.

The E²PROM is pre-programmed with the necessary addresses plus frame position and function bits which will be read into the MV6639 on power up.

The circuit will demonstrate the voltage doubler, tone outputs and tone cancel

The required component values together with a suitable printed circuit layout (Fig.17) are shown below.

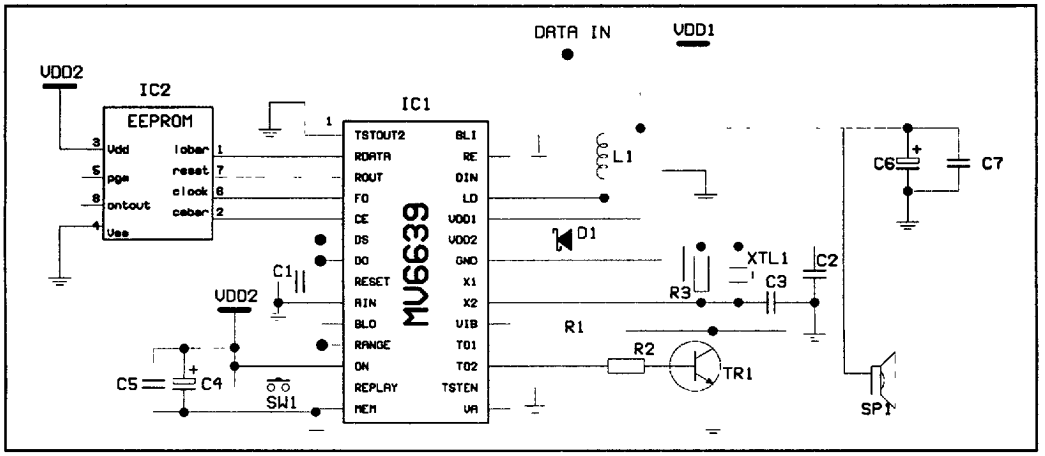


Fig 16 MV6639 Evaluation Circuit

COMPONENT LIST

R1	51R	L1	220uH
R2	360R	XTL1	32768Hz Watch Crystal
R3	10M	TR1	BFS17
C1	10nF	D1	ZC2811E schottky diode
C2	22pF	SP1	Miniature Sounder CB-09AP
C3	22pF	SW1	Push Button Switch
C4	100uF	IC1	MV6639
C6	100uF	IC2	SPM28C51M
C5, C7	33nF		

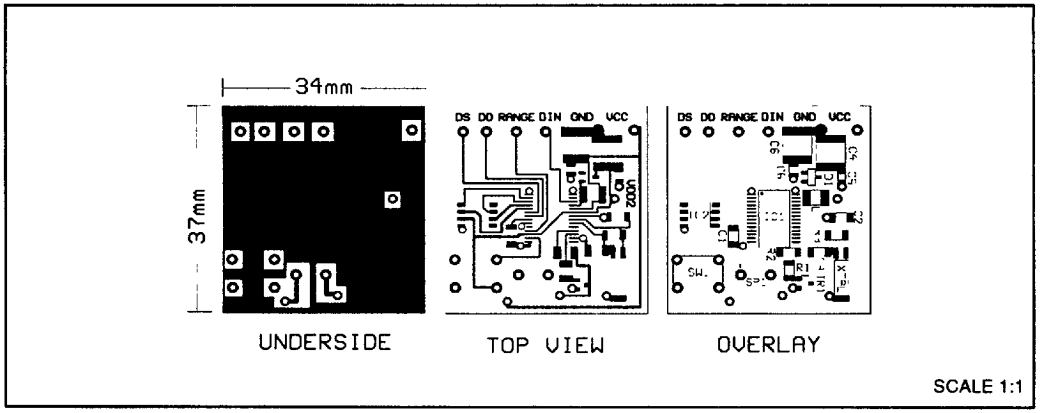


Fig 17 Printed Circuit Details