

MN4017B / MN4017BS

5-Stage Johnson Counters

Description

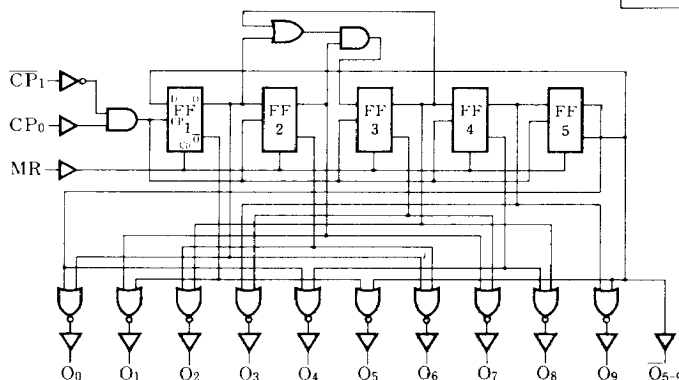
The MN4017B/S are 5-stage Johnson decade counters constructed with five D-type flip-flops. One of the outputs ($O_0 \sim O_9$) becomes High level according to the number of counter pulses applied to CP_0 or $\overline{CP}_1$. The counter is advanced by either a positive going edge of CP_0 while $\overline{CP}_1$ is Low or a negative going edge of $\overline{CP}_1$ while CP_0 is High. A High on the reset input (MR) resets the counter to zero ($O_0 = \overline{O}_{5-9} = \text{High}$, $O_1 \sim O_9 = \text{Low}$) independent of the clock inputs (CP_0 , $\overline{CP}_1$). These are equivalent to MOTOROLA MC14017B and RCA CD4017B.

Truth Table

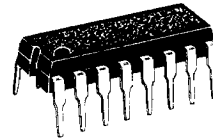
MR	CP_0	$\overline{CP}_1$	Mode
H	X	X	$O_0 = \overline{O}_{5-9} = \text{H}$, $O_1 \sim O_9 = \text{L}$
L	H		Counter Advances
L		L	
L	L	X	No Change
L	X	H	
L	H		
L		L	

Note) X : don't care

Logic Diagram



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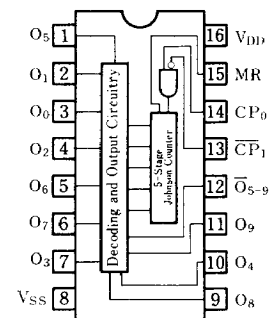
16-Pin • Plastic DIL Package

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16-Pin • Pinnaflat Package (SO-16D)

Pin Configuration



Pin Explanation

CP_0 : Positive clock input ()
 $\overline{CP}_1$: Negative clock input ()
 MR : Reset input
 $O_0 \sim O_9$: Output (10 Bits)

Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	$-0.5 \sim +18$	V
Input Voltage	V_I	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage	V_O	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current	$\pm I_I$	max. 10	mA
Power Dissipation (per package)	$T_a = -40 \sim +60^\circ\text{C}$ $T_a = +60 \sim +85^\circ\text{C}$	max. 400	mW
		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)	P_D	max. 100	mW
Operating Ambient Temperature	T_{opr}	$-40 \sim +85$	°C
Storage Temperature	T_{stg}	$-65 \sim +150$	°C

* $V_{DD} + 0.5\text{V}$ should be under 18V

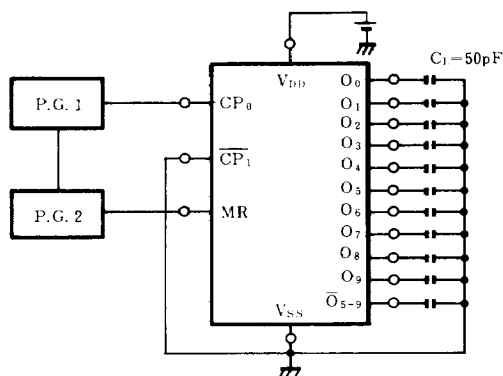
DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Sym- bol	Conditions	Ta = -40°C		Ta = 25°C		Ta = 85°C		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I_{DD}	$V_I = V_{SS}$ or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	$V_I = V_{SS}$ or V_{DD} $ I_O < 1\mu\text{A}$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_I = V_{SS}$ or V_{DD} $ I_O < 1\mu\text{A}$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$ I_O < 1\mu\text{A}$ $V_O = 0.5\text{V}$ or 4.5V $V_O = 1\text{V}$ or 9V $V_O = 1.5\text{V}$ or 13.5V	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$ I_O < 1\mu\text{A}$ $V_O = 0.5\text{V}$ or 4.5V $V_O = 1\text{V}$ or 9V $V_O = 1.5\text{V}$ or 13.5V	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	$V_O = 0.4\text{V}, V_I = 0$ or 5V	0.52	—	0.44	—	0.36	—	mA
	10		$V_O = 0.5\text{V}, V_I = 0$ or 10V	1.3	—	1.1	—	0.9	—	
	15		$V_O = 1.5\text{V}, V_I = 0$ or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O = 4.6\text{V}, V_I = 0$ or 5V	0.52	—	0.44	—	0.36	—	mA
	10		$V_O = 9.5\text{V}, V_I = 0$ or 10V	1.3	—	1.1	—	0.9	—	
	15		$V_O = 13.5\text{V}, V_I = 0$ or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O = 2.5\text{V}, V_I = 0$ or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	$V_I = 0$ or 15V	—	0.3	—	0.3	—	1	μA

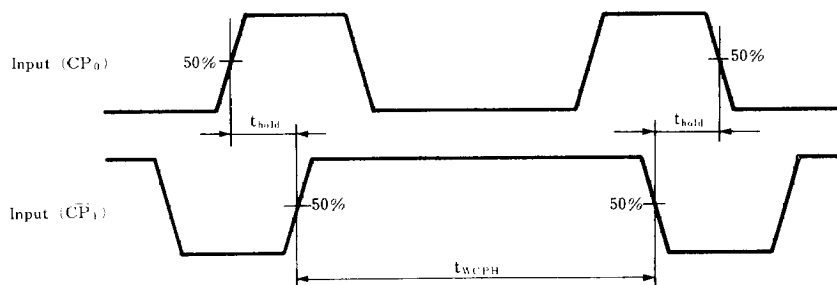
■ Switching Characteristics (Ta = 25°C, V_{SS} = 0V, C_L = 50pF)

Item	V _{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t _{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t _{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP ₀ , $\overline{\text{CP}}_1 \rightarrow \text{O}_0$ to O_9 (H→L)	5	t _{PHL}	—	195	585	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time CP ₀ , $\overline{\text{CP}}_1 \rightarrow \text{O}_0$ to O_9 (L→H)	5	t _{PLH}	—	245	735	ns
	10		—	95	285	
	15		—	60	180	
Propagation Delay Time CP ₀ , $\overline{\text{CP}}_1 \rightarrow \overline{\text{O}}_{5-9}$ (H→L)	5	t _{PHL}	—	245	735	ns
	10		—	90	270	
	15		—	60	180	
Propagation Delay Time CP ₀ , $\overline{\text{CP}}_1 \rightarrow \overline{\text{O}}_{5-9}$ (L→H)	5	t _{PLH}	—	190	570	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time MR→O ₁ to O ₉ (H→L)	5	t _{PHL}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time MR→ $\overline{\text{O}}_{5-9}$ (L→H)	5	t _{PLH}	—	110	330	ns
	10		—	45	135	
	15		—	35	105	
Propagation Delay Time MR→O ₀ (L→H)	5	t _{PLH}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Hold Time CP ₀ → $\overline{\text{CP}}_1$	5	t _{hold}	—	70	210	ns
	10		—	25	75	
	15		—	15	45	
Hold Time $\overline{\text{CP}}_1$ →CP ₀	5	t _{hold}	—	85	255	ns
	10		—	30	90	
	15		—	20	60	
Minimum Clock Pulse Width	5	t _{WCP}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Minimum Reset Pulse Width	5	t _{WMRH}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Reset Recovery Time	5	t _{RMR}	—	25	75	ns
	10		—	10	40	
	15		—	10	30	
Maximum Clock Frequency	5	f _{max}	3	6	—	ns
	10		8	16	—	
	15		12	24	—	
Input Capacitance		C _i	—	—	7.5	pF

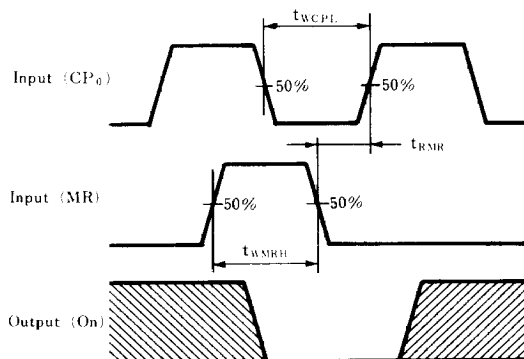
1. Switching Time Test Circuit



2. Waveforms



Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0 .
Hold times are shown as positive values, but may be specified as negative values.



Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths
Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition;
 t_{wCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

■ Timing Diagram

