MC100EP210S

2.5V 1:5 Dual Differential LVDS Compatible Clock Driver

The MC100EP210S is a low skew 1–to–5 dual differential driver, designed with LVDS clock distribution in mind. The LVDS or LVPECL input signals are differential and the signal is fanned out to five identical differential LVDS outputs.

The EP210S specifically guarantees low output–to–output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

Two internal 50 Ω resistors are provided across the inputs. For LVDS inputs, VTA and VTB pins should be unconnected. For LVPECL inputs, VTA and VTB pins should be connected to the V_{TT} (V_{CC}–2.0 V) supply.

Designers can take advantage of the EP210S performance to distribute low skew LVDS clocks across the backplane or the board.

Special considerations are required for differential inputs under No Signal conditions to prevent instability.

- 20 ps Typical Output–to–Output Skew
- 85 ps Typical Device–to–Device Skew
- 550 ps Typical Propagation Delay
- The 100 Series Contains Temperature Compensation
- Maximum Frequency >1 GHz Typical
- Operating Range: V_{CC} = 2.375 V to 2.625 V with V_{EE} = 0 V
- Internal 50 Ω Input Termination Resistors
- LVDS Input/Output Compatible

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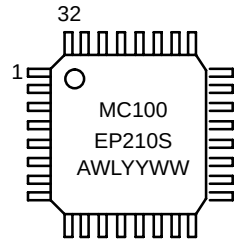
TQFP–32
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EP210SFA	TQFP–32	250 Units/Tray
MC100EP210SFAR2	TQFP–32	2000 Tape & Reel

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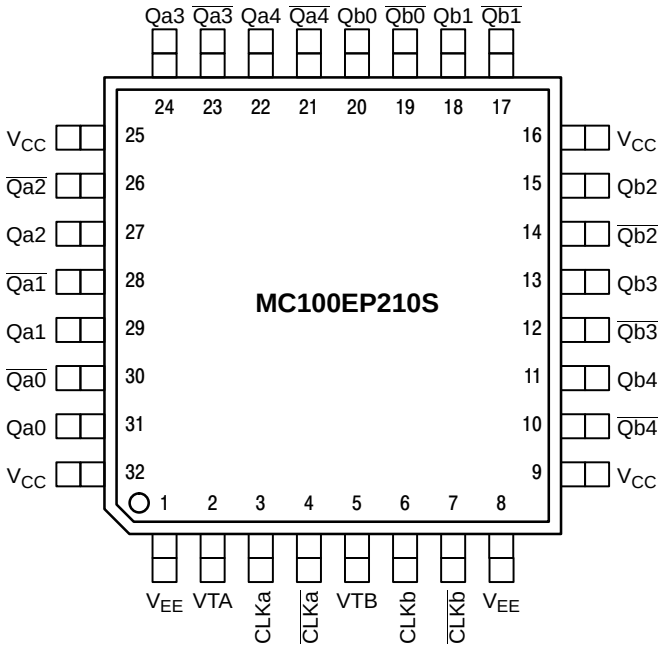


Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32–Lead TQFP Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
CLKn, $\overline{CLKn}$	LVDS, LVPECL CLK Inputs
Qn0:4, $\overline{Qn0:4}$	LVDS Outputs
VTA	50 Ohm Termination Resistors
VTB	50 Ohm Termination Resistors
V_{CC}	Positive Supply
V_{EE}	Ground

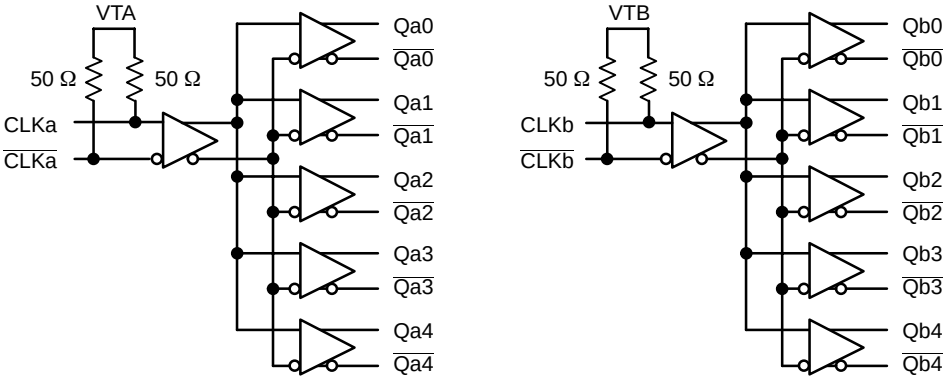


Figure 2. Logic Diagram

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		N/A
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV
Moisture Sensitivity (Note 1)		Level 2
Flammability Rating Oxygen Index		UL–94 code V–0 A 1/8” 28 to 34
Transistor Count		461 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, refer to Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Power Supply	V_{EE} = 0 V		6	V
V_{EE}	Power Supply (GND)	V_{CC} = 2.5 V		–6	V
V_I	LVDS, LVPECL Input Voltage	V_{EE} = 0 V	$V_I \leq V_{CC}$	6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	32 TQFP 32 TQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	32 TQFP	12 to 17	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

DC CHARACTERISTICS V_{CC} = 2.5 V, V_{EE} = 0 V (Note 3)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		150	200		150	200		150	200	mA
V_{OH}	Output HIGH Voltage (Note 4)	1250	1400	1550	1250	1400	1550	1250	1400	1550	mV
V_{OL}	Output LOW Voltage (Note 4)	800	950	1100	800	950	1100	800	950	1100	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_T	Internal Termination Resistor	43		57	43	50	57	43		57	Ω
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}.
4. All loading with 100 ohms across LVDS differential outputs.
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CC} = 2.375 to 2.625 V, V_{EE} = 0 V (Note 6)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
$f_{maxLVDS/LVPECL}$	Maximum Frequency (See Figure 3. F_{max}/JITTER)		> 1			> 1			> 1		GHz
t_{PLH} t_{PHL}	Propagation Delay	425	525	625	450	550	650	475	575	675	ps
t_{skew}	Within–Device Skew (Note 7) Device–to–Device Skew (Note 8) Duty Cycle Skew (Note 9)		20 85 80	25 160 100		20 85 80	25 160 100		20 85 80	35 160 100	ps
t_{JITTER}	Cycle–to–Cycle Jitter (See Figure 3. F_{max}/JITTER)		.2	< 1		.2	< 1		.2	< 1	ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	50	130	200	75	150	225	80	160	230	ps

6. Measured with 400 mV source, 50% duty cycle clock source. All loading with 100 ohms across differential outputs.
7. Skew is measured between outputs under identical transitions of similar paths through a device.
8. Device–to–Device skew for identical transitions at identical V_{CC} levels.
9. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.

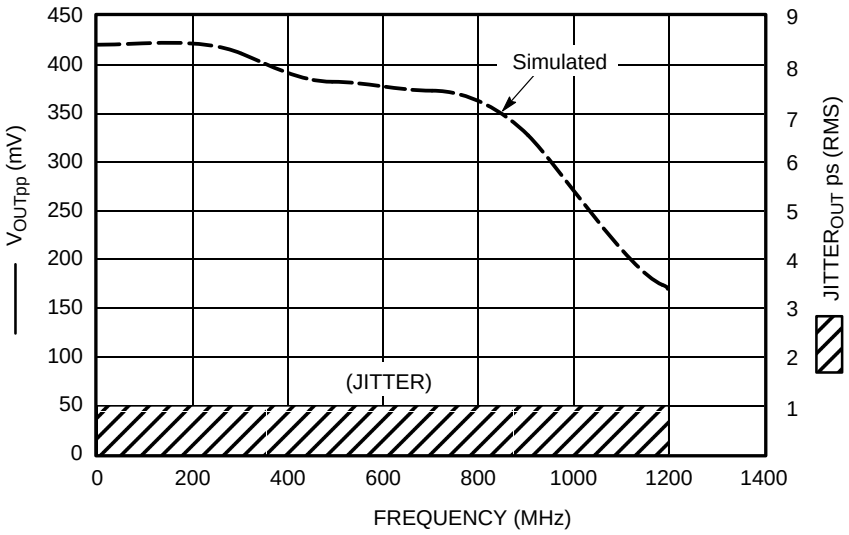


Figure 3. F_{max}/Jitter

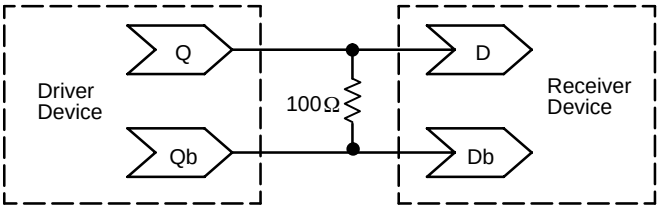
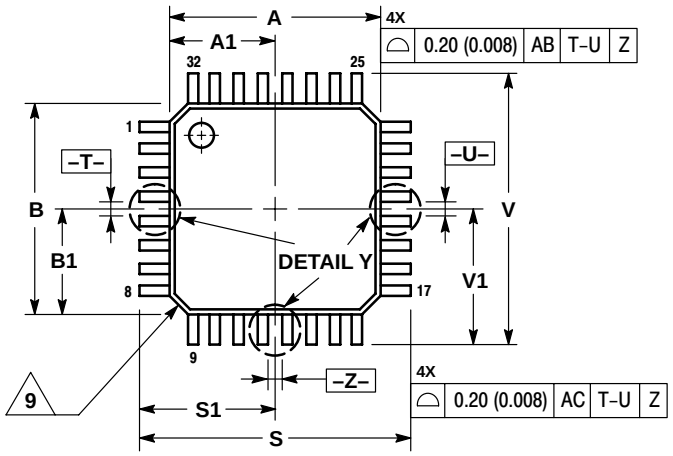
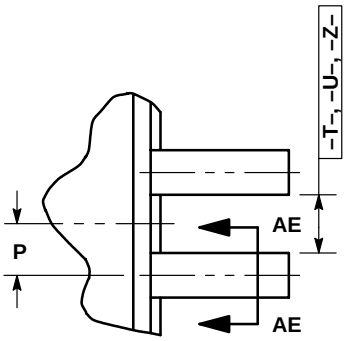


Figure 4. Typical Termination for Output Driver and Device Evaluation

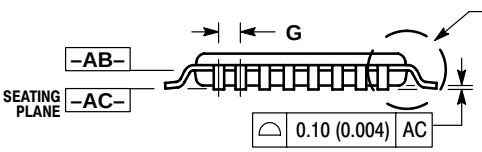
PACKAGE DIMENSIONS

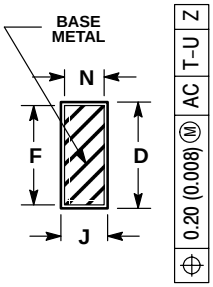
TQFP
FA SUFFIX
32–LEAD PLASTIC PACKAGE
CASE 873A–02
ISSUE A



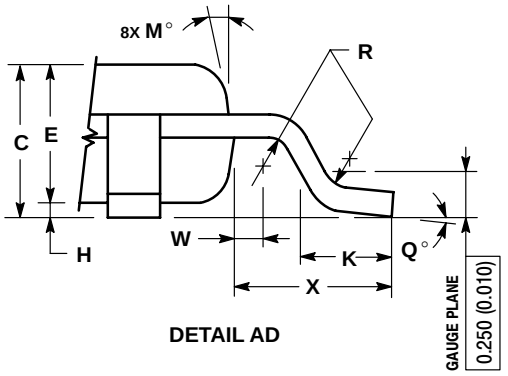


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Notes

Notes

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