



Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (128K x 8-BIT)

IDT71024

FEATURES:

- 128K x 8 advanced high-speed CMOS static RAM
- Equal access and cycle times
 - Military: 15/17/20/25ns
 - Commercial: 12/15/17/20ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 32-pin Ceramic DIP, Plastic DIP, 300 and 400 mil Plastic SOJ, and LCC packages
- Military product compliant to MIL-STD-883, Class B

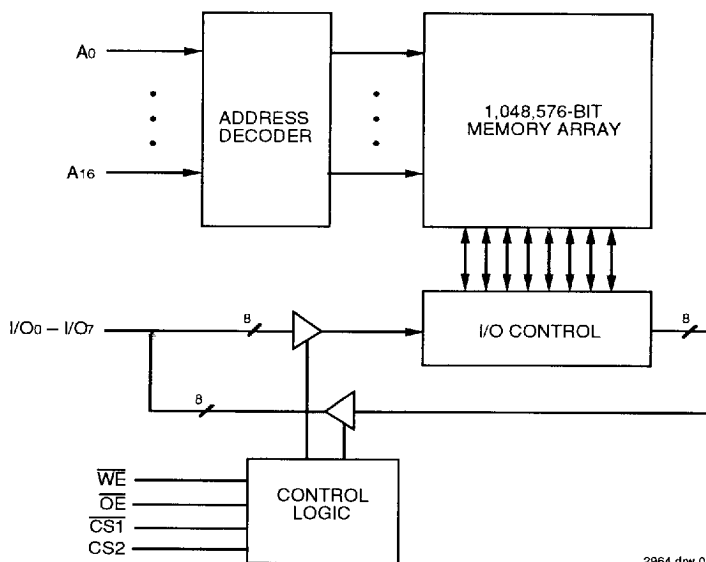
DESCRIPTION:

The IDT71024 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71024 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71024 is packaged in 32-pin 400 mil Ceramic DIP, 32-pin 400 mil Plastic DIP, 32-pin 300 mil Plastic SOJ, 32-pin 400 mil Plastic SOJ, and 32-pin 400 x 820 mil LCC packages.

FUNCTIONAL BLOCK DIAGRAM



The IDT Logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1994

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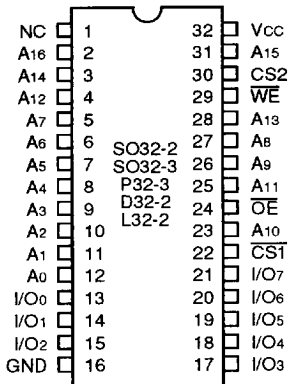
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PIN CONFIGURATION



2964 drw 02

DIP/SOJ/LCC
TOP VIEWABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.25	1.25	W
IOUT	DC Output Current	50	50	mA

NOTES:

- 1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2 VTERM must not exceed VCC + 0.5V.

TRUTH TABLE^(1,2)

INPUTS				I/O	FUNCTION
WE	CS1	CS2	OE		
X	H	X	X	High-Z	Deselected—Standby (ISB)
X	VHC ⁽³⁾	X	X	High-Z	Deselected—Standby (ISB1)
X	X	L	X	High-Z	Deselected—Standby (ISB)
X	X	VLC ⁽³⁾	X	High-Z	Deselected—Standby (ISB1)
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

NOTES:

1. H = VIH, L = VIL, X = Don't care.
2. VLC = 0.2V, VHC = VCC - 0.2V.
3. Other inputs ≥ VHC or ≤ VLC.

2964 tbl 01

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	8	pF
CIO	I/O Capacitance	VOUT = 3dV	8	pF

NOTE:

- 1 This parameter is guaranteed by device characterization, but is not production tested.

2964 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC + 0.5	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

- 1 VIL (min) = -1.5V for pulse width less than 10ns, once per cycle.

2964 tbl 04

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71024		Unit
			Min.	Max.	
ILI	Input Leakage Current	VCC = Max., VIN = GND to VCC	—	5	μA
ILO	Output Leakage Current	VCC = Max., CS1 = VIH, CS2 = VIL, VOUT = GND to VCC	—	5	μA
VOL	Output LOW Voltage	IOL = 8mA, VCC = Min.	—	0.4	V
VOH	Output HIGH Voltage	IOH = -4mA, VCC = Min	2.4	—	V

2964 tbl 05

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

($V_{CC} = 5.0V \pm 10\%$, $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$)

Symbol	Parameter	71024S12 ⁽³⁾		71024S15		71024S17		71024S20		71024S25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC}	Dynamic Operating Current, CS2 $\geq V_{IH}$ and CS2 $\geq V_{IH}$ and CS1 $\leq V_{IL}$, Outputs Open, $V_{CC} = \text{Max}$, $f = f_{MAX}$ ⁽²⁾	160	—	155	180	150	170	140	160	—	145	mA
I _{SB}	Standby Power Supply Current (TTL Level) CS1 $\geq V_{IH}$ or CS2 $\leq V_{IL}$, Outputs Open, $V_{CC} = \text{Max}$, $f = f_{MAX}$ ⁽²⁾	35	—	35	40	35	40	35	40	—	35	mA
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS1 $\geq V_{HC}$, or CS2 $\leq V_{LC}$ Outputs Open, $V_{CC} = \text{Max}$, $f = 0$ ⁽²⁾ , $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	15	—	10	15	10	15	10	15	—	15	mA

NOTES:

- 1 All values are maximum guaranteed values
- 2 $f_{MAX} = 1/t_{RC}$ (all address inputs are cycling at f_{MAX}), $f = 0$ means no address input lines are changing.
- 3 12ns specification is preliminary

2964 tbi 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2964 tbi 07

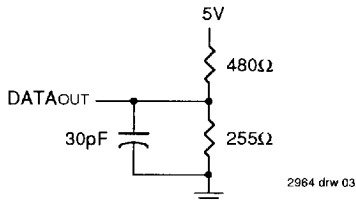
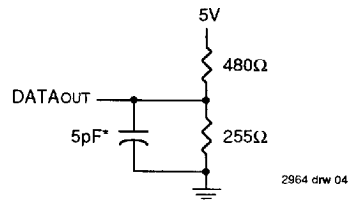


Figure 1. AC Test Load



*Including jig and scope capacitance

Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

		71024S12 ⁽¹⁾		71024S15		71024S17		71024S20		71024S25 ⁽²⁾		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t _{RC}	Read Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
t _{AA}	Address Access Time	—	12	—	15	—	17	—	20	—	25	ns
t _{ACS}	Chip Select Access Time	—	12	—	15	—	17	—	20	—	25	ns
t _{CLZ} ⁽³⁾	Chip Select to Output in Low-Z	3	—	3	—	3	—	3	—	3	—	ns
t _{CHZ} ⁽³⁾	Chip Deselect to Output in High-Z	0	6	0	7	0	8	0	8	0	10	ns
t _{OE}	Output Enable to Output Valid	—	6	—	7	—	8	—	8	—	10	ns
t _{OLZ} ⁽³⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t _{OHZ} ⁽³⁾	Output Disable to Output in High-Z	0	5	0	5	0	6	0	7	0	10	ns
t _{OH}	Output Hold from Address Change	4	—	4	—	4	—	4	—	4	—	ns
t _{PU} ⁽³⁾	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t _{PD} ⁽³⁾	Chip Deselect to Power-Down Time	—	12	—	15	—	17	—	20	—	25	ns
Write Cycle												
t _{WC}	Write Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
t _{AW}	Address Valid to End-of-Write	10	—	12	—	13	—	15	—	15	—	ns
t _{CW}	Chip Select to End-of-Write	10	—	12	—	13	—	15	—	15	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	10	—	12	—	13	—	15	—	15	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End-of-Write	7	—	8	—	9	—	9	—	10	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t _{OW} ⁽³⁾	Output Active from End-of-Write	3	—	3	—	3	—	4	—	4	—	ns
t _{WHZ} ⁽³⁾	Write Enable to Output in High-Z	0	5	0	5	0	7	0	8	0	9	ns

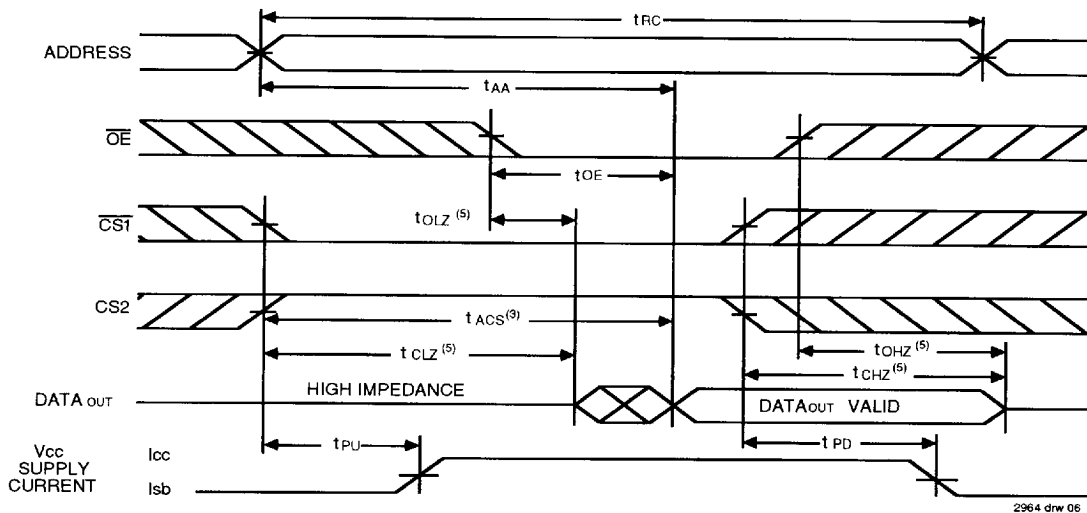
NOTES:

- 0°C to +70°C temperature range only 12ns specification is preliminary
- 55°C to +125°C temperature range only
- This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

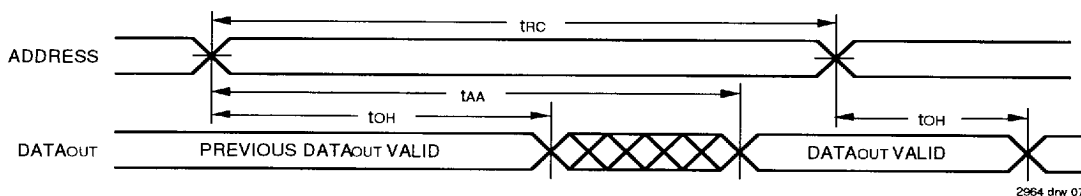
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TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



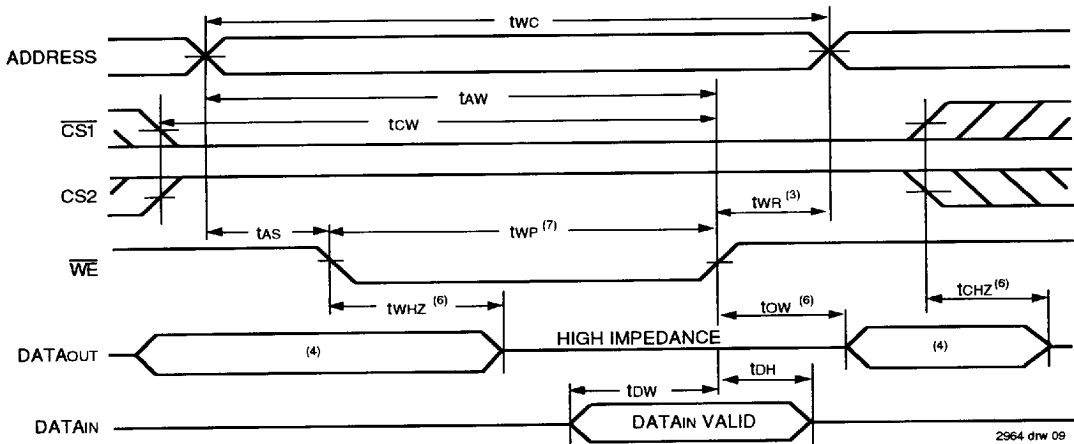
TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



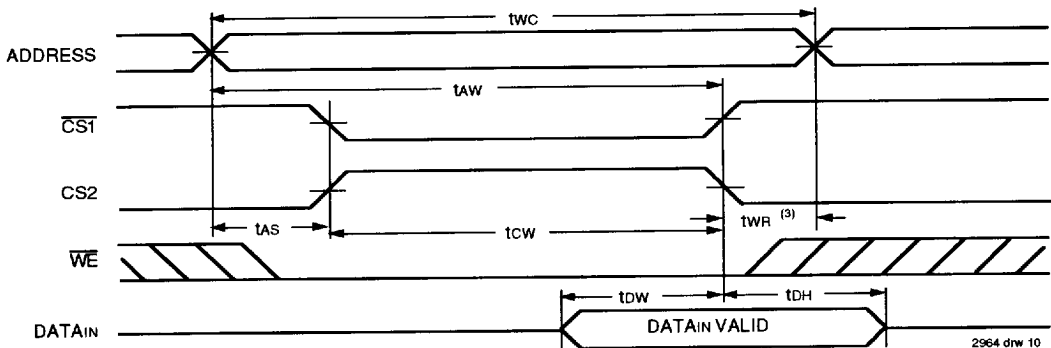
NOTES:

- 1 WE is HIGH for Read Cycle
- 2 Device is continuously selected, $\overline{CS1}$ is LOW, CS2 is HIGH
- 3 Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise tAA is the limiting parameter
- 4 OE is LOW
- 5 Transition is measured $\pm 200\text{mV}$ from steady state

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)^(1, 2, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS1}$ AND CS2 CONTROLLED TIMING)^(1, 2, 5)



NOTES:

1. $\overline{WE}$ must be HIGH, $\overline{CS1}$ must be HIGH, or CS2 must be LOW during all address transitions
2. A write occurs during the overlap of a LOW $\overline{CS1}$, HIGH CS2, and a LOW $\overline{WE}$
3. t_{WR} is measured from the earlier of either $\overline{CS1}$ or $\overline{WE}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied
5. If the $\overline{CS1}$ LOW transition or the CS2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS1}$ and CS2 must both be active during the t_{CW} write period.
6. Transition is measured $\pm 200mV$ from steady state
7. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{OW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}

ORDERING INFORMATION

