



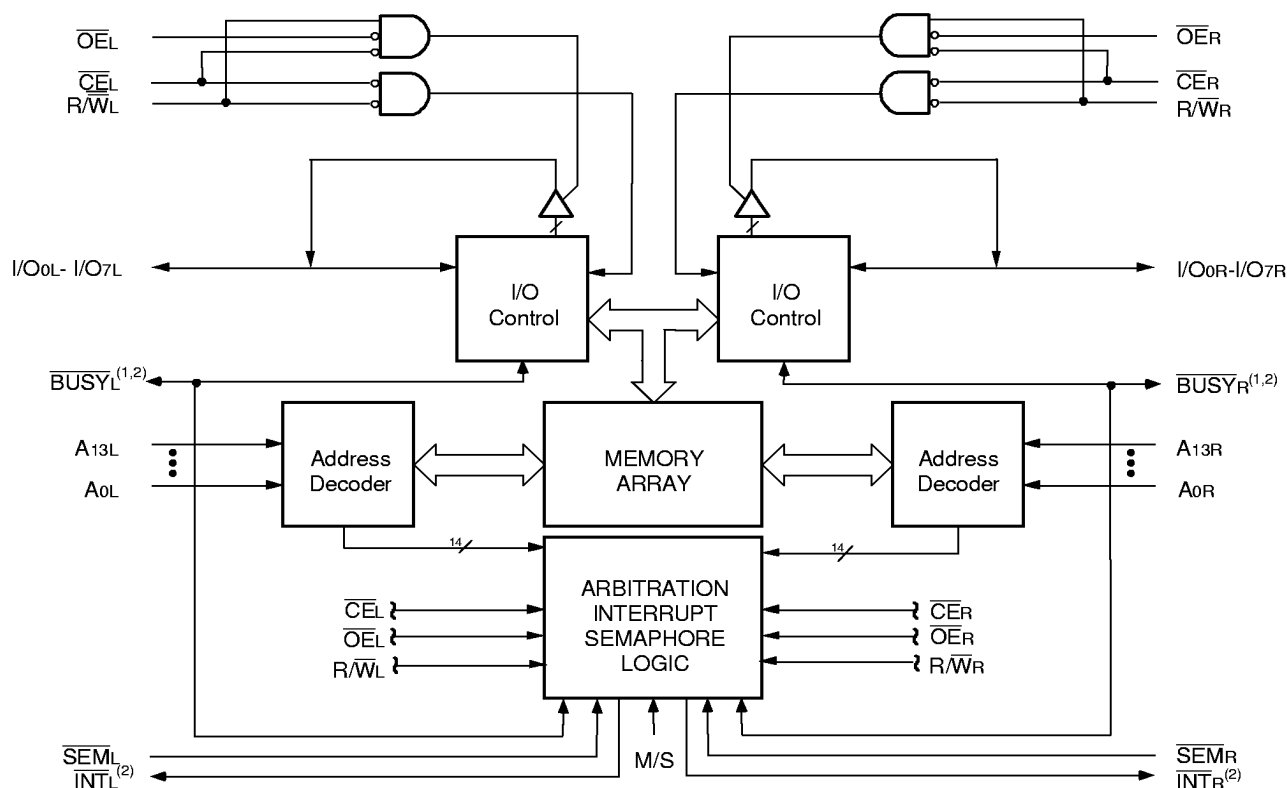
HIGH-SPEED 16K x 8 DUAL-PORT STATIC RAM

IDT7006S/L

Features

- ♦ True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- ♦ High-speed access
 - Military: 20/25/35/55/70ns (max.)
 - Industrial: 55ns (max.)
 - Commercial: 15/17/20/25/35/55ns (max.)
- ♦ Low-power operation
 - IDT7006S
 - Active: 750mW (typ.)
 - Standby: 5mW (typ.)
 - IDT7006L
 - Active: 700mW (typ.)
 - Standby: 1mW (typ.)
- ♦ IDT7006 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- ♦ $\overline{M/\overline{S}} = H$ for \overline{BUSY} output flag on Master, $\overline{M/\overline{S}} = L$ for \overline{BUSY} input on Slave
- ♦ Busy and Interrupt Flags
- ♦ On-chip port arbitration logic
- ♦ Full on-chip hardware support of semaphore signaling between ports
- ♦ Fully asynchronous operation from either port
- ♦ Devices are capable of withstanding greater than 2001V electrostatic discharge
- ♦ Battery backup operation—2V data retention
- ♦ TTL-compatible, single 5V ($\pm 10\%$) power supply
- ♦ Available in 68-pin PGA, quad flatpack, PLCC, and a 64-pin TQFP
- ♦ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds

Functional Block Diagram



2739 drw 01

NOTES:

1. (MASTER): \overline{BUSY} is output; (SLAVE): \overline{BUSY} is input.
2. \overline{BUSY} outputs and \overline{INT} outputs are non-tri-stated push-pull.

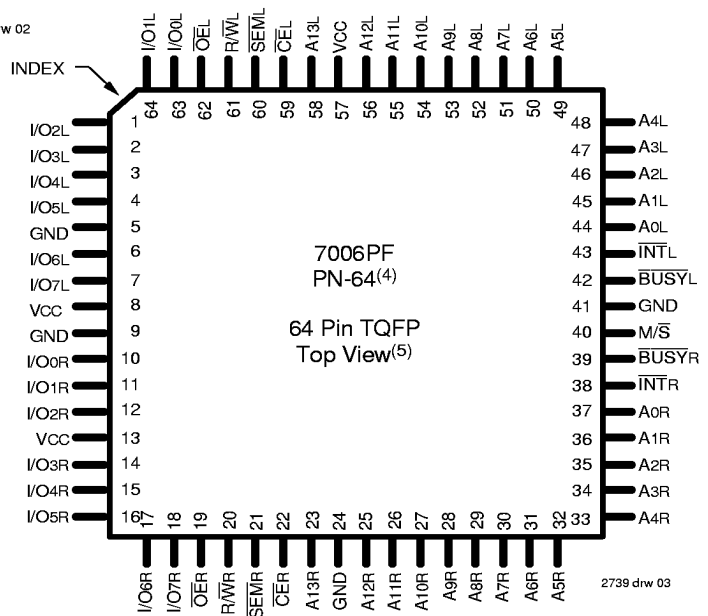
JUNE 1999

The IDT7006 is a high-speed 16K x 8 Dual-Port Static RAM. The IDT7006 is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

a very low standby power mode.

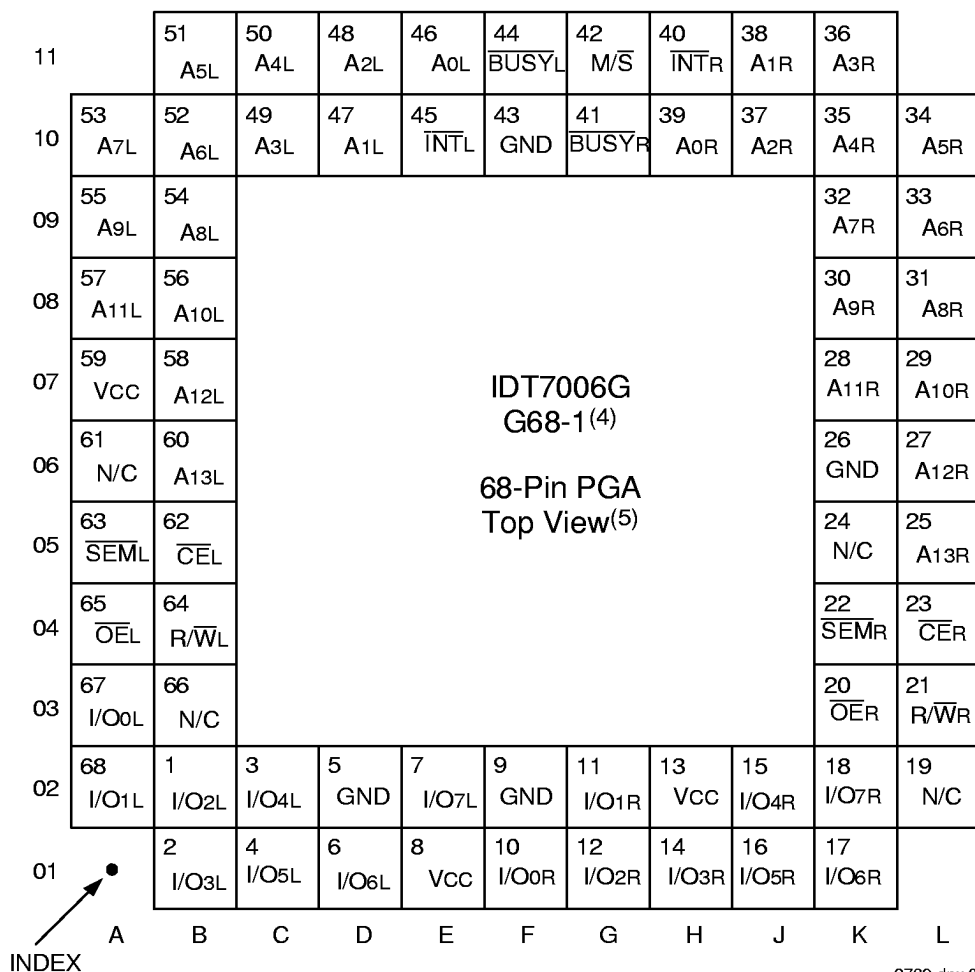
The IDT7006 is packaged in a ceramic 68-pin PGA, an 68-pin quad flatpack, a PLCC, and a 64-pin thin quad flatpack, TQFP. Military grade products manufactured in compliance with the latest revision of MIL-PRF-38535 QML, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pinout diagram for the 68 Pin PLCC / Flatpack (Top View). The diagram shows a square package with pins numbered 1 to 68. The top edge (pins 1-16) includes I/O2L, I/O3L, I/O4L, I/O5L, GND, I/O6L, I/O7L, VCC, GND, I/O0R, I/O1R, I/O2R, VCC, I/O3R, I/O4R, I/O5R, and I/O6R. The right edge (pins 17-32) includes A5L, A4L, A3L, A2L, A1L, A0L, INTL, BUSYL, GND, M/S, BUSYR, INTR, A0R, A1R, A2R, A3R, and A4R. The bottom edge (pins 33-48) includes I/OTR, N/C, OER, RWR, SEMR, N/C, A13R, GND, A12R, A11R, A10R, A9R, A8R, A7R, A6R, and A5R. The left edge (pins 49-68) includes I/O1L, I/O0L, N/C, IOEL, RWL, ISEL, ICEL, N/C, A13L, VCC, A12L, A11L, A10L, A9L, A8L, A7L, and A6L. The diagram is labeled "68 Pin PLCC / Flatpack Top View(5)" and "IDT7006J or F J68-1(4) F68-1(4)". The drawing number "2739 drw 02" is at the bottom right.



1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. J68-1 package body is approximately .95 in x .95 in. x .17 in.
F68-1 package body is approximately .97 in x .97 in x .08 in.
PN64-1 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking

Pin Configurations^(1,2,3) (con't.)



2739 drw 04

NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 1.18 in x 1.18 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking

Pin Names

Left Port	Right Port	Names
\overline{CE}_L	\overline{CE}_R	Chip Enable
R/\overline{WL}	R/\overline{WR}	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
A0L - A13L	A0R - A13R	Address
I/O0L - I/O7L	I/O0R - I/O7R	Data Input/Output
\overline{SEM}_L	\overline{SEM}_R	Semaphore Enable
\overline{INT}_L	\overline{INT}_R	Interrupt Flag
\overline{BUSY}_L	\overline{BUSY}_R	Busy Flag
M/S		Master or Slave Select
Vcc		Power
GND		Ground

2739 tbi 01

Truth Table I: Non-Contention Read/Write Control

Inputs ⁽¹⁾				Outputs	Mode
\overline{OE}	R/W	\overline{OE}	\overline{SEM}	I/O ₀₋₇	
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATA _{IN}	Write to Memory
L	H	L	H	DATA _{OUT}	Read Memory
X	X	H	X	High-Z	Outputs Disabled

NOTE:

1. A_{0L} – A_{13L} is not equal to A_{0R} – A_{13R}

2739 tbl 02

Truth Table II: Semaphore Read/Write Control⁽¹⁾

Inputs ⁽¹⁾				Outputs	Mode
\overline{OE}	R/W	\overline{OE}	\overline{SEM}	I/O ₀₋₇	
H	H	L	L	DATA _{OUT}	Read in Semaphore Flag Data Out
H	↑	X	L	DATA _{IN}	Write I/O ₀ into Semaphore Flag
L	X	X	L	—	Not Allowed

NOTE:

1. There are eight semaphore flags written to via I/O₀ and read from I/O₀ - I/O₇. These eight semaphores are addressed by A₀ - A₂.

2739 tbl 03

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I _{OUT}	DC Output Current	50	50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≤ V_{CC} + 10%.

2739 tbl 04

Capacitance⁽¹⁾ (T_A = +25°C, f = 1.0mhz)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	9	pF
C _{OUT}	Output Capacitance	V _{OUT} = 3dV	10	pF

NOTES:

1. These parameters are determined by device characterization, but are not production tested (TQFP Package Only).
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

2739 tbl 05

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTES:

1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{CC} + 10%.

2739 tbl 06

Maximum Operating Temperature and Supply Voltage^(1,2)

Grade	Ambient Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	40°C to +85°C	0V	5.0V ± 10%

NOTES:

1. This is the parameter T_A.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

2739 tbl 07

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	7006S		7006L		Unit
			Min.	Max.	Min.	Max.	
$ I_L $	Input Leakage Current ⁽¹⁾	$V_{CC} = 5.5V, V_{IN} = 0V \text{ to } V_{CC}$	—	10	—	5	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE} = V_{IH}, V_{OUT} = 0V \text{ to } V_{CC}$	—	10	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = 4mA$	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4	—	2.4	—	V

NOTE:

1. At $V_{CC} \leq 2.0V$ input leakages are undefined.

2739 tbl 08

Data Retention Characteristics Over All Temperature Ranges (L Version Only) ($V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V$)

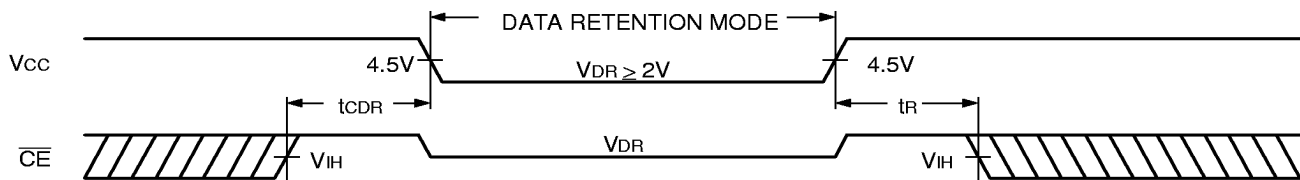
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = 2V$	2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	Mil. & Ind. —	100	4000	μA
		$V_{IN} \geq V_{HC} \text{ or } \leq V_{LC}$	Com'l. —	100	1500	
$t_{CDR}^{(3)}$	Chip Deselect to Data Retention Time	$\overline{SEM} \geq V_{HC}$	0	—	—	ns
$t_R^{(3)}$	Operation Recovery Time		$t_{RC}^{(2)}$	—	—	ns

NOTES:

1. $T_A = +25^\circ C$, $V_{CC} = 2V$, and are not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed by characterization, but is not production tested.

2739 tbl 09

Data Retention Waveform



2739 drw 05

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,6) (V_{CC} = 5.0V ± 10%)

					7006X15 Com'1 Only		7006X17 Com'1 Only		7006X20 Com'1 & Military		7006X25 Com'1 & Military		
Symbol	Parameter	Test Condition	Version		Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Unit
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$, Outputs Open $SEM = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L	S	170	310	170	310	160	290	155	265	mA
				L	160	260	160	260	150	240	145	220	
			MIL & IND	S	—	—	—	—	160	370	155	340	
				L	—	—	—	—	150	320	145	280	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $SEMR = SEML = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L	S	20	60	20	60	20	60	16	60	mA
				L	10	50	10	50	10	50	10	50	
			MIL & IND	S	—	—	—	—	20	90	16	80	
				L	—	—	—	—	10	70	10	65	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(5)}$ Active Port Outputs Open, $f = f_{MAX}^{(3)}$ $SEMR = SEML = V_{IH}$	COM'L	S	105	190	105	190	95	180	90	170	mA
				L	95	160	95	160	85	150	80	140	
			MIL & IND	S	—	—	—	—	95	240	90	215	
				L	—	—	—	—	85	210	80	180	
ISB3	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(4)}$ $SEMR = SEML \geq V_{CC} - 0.2V$	COM'L	S	1.0	15	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	0.2	5	
			MIL & IND	S	—	—	—	—	1.0	30	1.0	30	
				L	—	—	—	—	0.2	10	0.2	10	
ISB4	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{CC} - 0.2V^{(5)}$ $SEMR = SEML \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Open $f = f_{MAX}^{(3)}$	COM'L	S	100	170	100	170	90	155	85	145	mA
				L	90	140	90	140	80	130	75	120	
			MIL & IND	S	—	—	—	—	90	225	85	200	
				L	—	—	—	—	80	200	75	170	

2739 tbl 10

Symbol	Parameter	Test Condition	Version	7006X35 Com'1 & Military		7006X55 Com'1, Ind & Military		7006X70 Military Only		Unit	
				Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.		
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$, Outputs Open $SEM = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L	S L	150 140	250 210	150 140	250 210	— —	— —	mA
			MIL & IND	S L	150 140	300 250	150 140	300 250	140 130	300 250	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $SEMR = SEML = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L	S L	13 10	60 50	13 10	60 50	— —	— —	mA
			MIL & IND	S L	13 10	80 65	13 10	80 65	10 8	80 65	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(5)}$ Active Port Outputs Open, $f = f_{MAX}^{(3)}$ $SEMR = SEML = V_{IH}$	COM'L	S L	85 75	155 130	85 75	155 130	— —	— —	mA
			MIL & IND	S L	85 75	190 160	85 75	190 160	80 70	190 160	
ISB3	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(4)}$ $SEMR = SEML \geq V_{CC} - 0.2V$	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5	— —	— —	mA
			MIL & IND	S L	1.0 0.2	30 10	1.0 0.2	30 10	1.0 0.2	30 10	
ISB4	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{CC} - 0.2V^{(5)}$ $SEMR = SEML \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Open $f = f_{MAX}^{(3)}$	COM'L	S L	80 70	135 110	80 70	135 110	— —	— —	mA
			MIL & IND	S L	80 70	175 150	80 70	175 150	75 65	175 150	

2739 tbl 11

NOTES:

- 'X' in part numbers indicates power rating (S or L)
- V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CC} DC = 120mA (typ)
- At f = f_{MAX}, address and I/O's are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- f = 0 means no address or control lines change.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- Industrial temperature: for other speeds, packages and powers contact your sales office.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2739 tbl 12

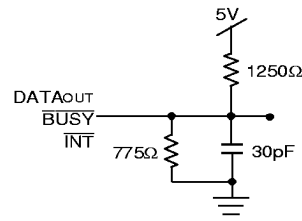
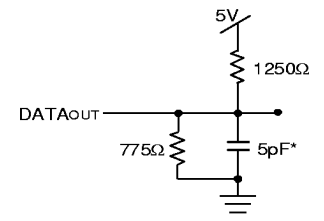


Figure 1. AC Output Test Load



2739 drw 06

Figure 2. Output Test Load
(5pF for tLZ, tHZ, tWZ, tOW)
*Including scope and jig.

AC Electrical Characteristics Over the Operating temperature and Supply Voltage Range^(4,5)

Symbol	Parameter	7006X15 Com'l Only		7006X17 Com'l Only		7006X20 Com'l & Military		7006X25 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	15	—	17	—	20	—	25	—	ns
tAA	Address Access Time	—	15	—	17	—	20	—	25	ns
tACE	Chip Enable Access Time ⁽⁶⁾	—	15	—	17	—	20	—	25	ns
tAOE	Output Enable Access Time	—	10	—	10	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time ^(1,2)	3	—	3	—	3	—	3	—	ns
tHZ	Output High-Z Time ^(1,2)	—	10	—	10	—	12	—	15	ns
tPU	Chip Enable to Power Up Time ^(2,5)	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time ^(2,5)	—	15	—	17	—	20	—	25	ns
tSOP	Semaphore Flag Update Pulse (\overline{OE} or \overline{SEM})	10	—	10	—	10	—	10	—	ns
tSAA	Semaphore Address Access Time	—	15	—	17	—	20	—	25	ns

2739 tbl 13a

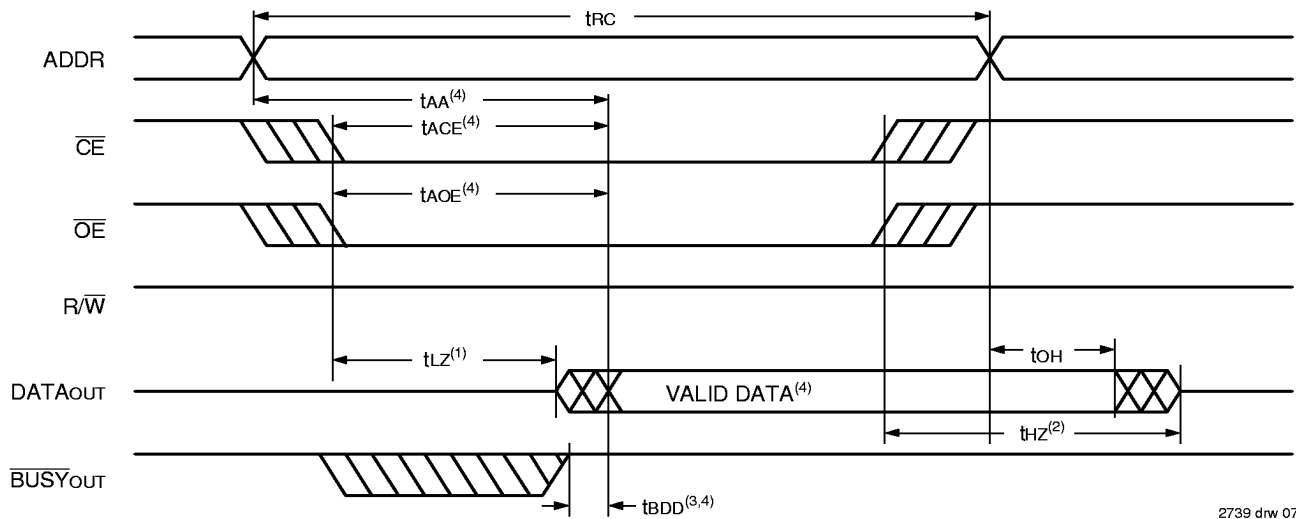
Symbol	Parameter	7006X35 Com'l & Military		7006X55 Com'l, Ind & Military		7006X70 Military Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	35	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	55	—	70	ns
tACE	Chip Enable Access Time ⁽³⁾	—	35	—	55	—	70	ns
tAOE	Output Enable Access Time	—	20	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time ^(1,2)	3	—	3	—	3	—	ns
tHZ	Output High-Z Time ^(1,2)	—	15	—	25	—	30	ns
tPU	Chip Enable to Power Up Time ^(2,5)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time ^(2,5)	—	35	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse (\overline{OE} or \overline{SEM})	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	55	—	70	ns

2739 tbl 13b

NOTES:

1. Transition is measured $\pm 500\text{mV}$ from Low or High-impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE} = V_{IL}$ and SEM = V_{IH} . To access semaphore, $\overline{CE} = V_{IH}$ and SEM = V_{IL} .
4. 'X' in part numbers indicates power rating (S or L).
5. Industrial temperature: for other speeds, packages and powers contact your sales office.

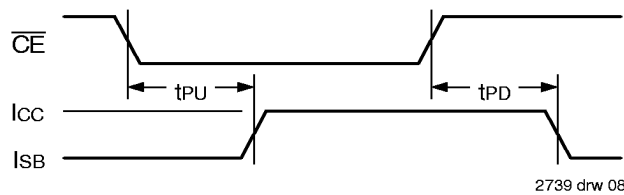
Waveform of Read Cycles⁽⁵⁾



NOTES:

1. Timing depends on which signal is asserted last, \overline{OE} or \overline{CE} .
2. Timing depends on which signal is de-asserted first \overline{CE} or \overline{OE} .
3. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations \overline{BUSY} has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{AOE} , t_{ACE} , t_{AA} or t_{BDD} .
5. $SEM = V_{IH}$.

Timing of Power-Up Power-Down



AC Electrical Characteristics Over the Operating Temperature and Supply Voltage^(5,6)

Symbol	Parameter	7006X15 Com'l Only		7006X17 Com'l Only		7006X20 Com'l & Military		7006X25 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	15	—	17	—	20	—	25	—	ns
tEW	Chip Enable to End-of-Write ⁽³⁾	12	—	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	12	—	12	—	15	—	20	—	ns
tAS	Address Set-up Time ⁽³⁾	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	10	—	10	—	15	—	15	—	ns
tHZ	Output High-Z Time ^(1,2)	—	10	—	10	—	12	—	15	ns
tDH	Data Hold Time ⁽⁴⁾	0	—	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z ^(1,2)	—	—	—	—	—	12	—	15	ns
tOW	Output Active from End-of-Write ^(1,2,4)	0	—	0	—	0	—	0	—	ns
tSWRD	SEM Flag Write to Read Time	5	—	5	—	5	—	5	—	ns
tSPS	SEM Flag Contention Window	5	—	5	—	5	—	5	—	ns

2739 tbl 14a

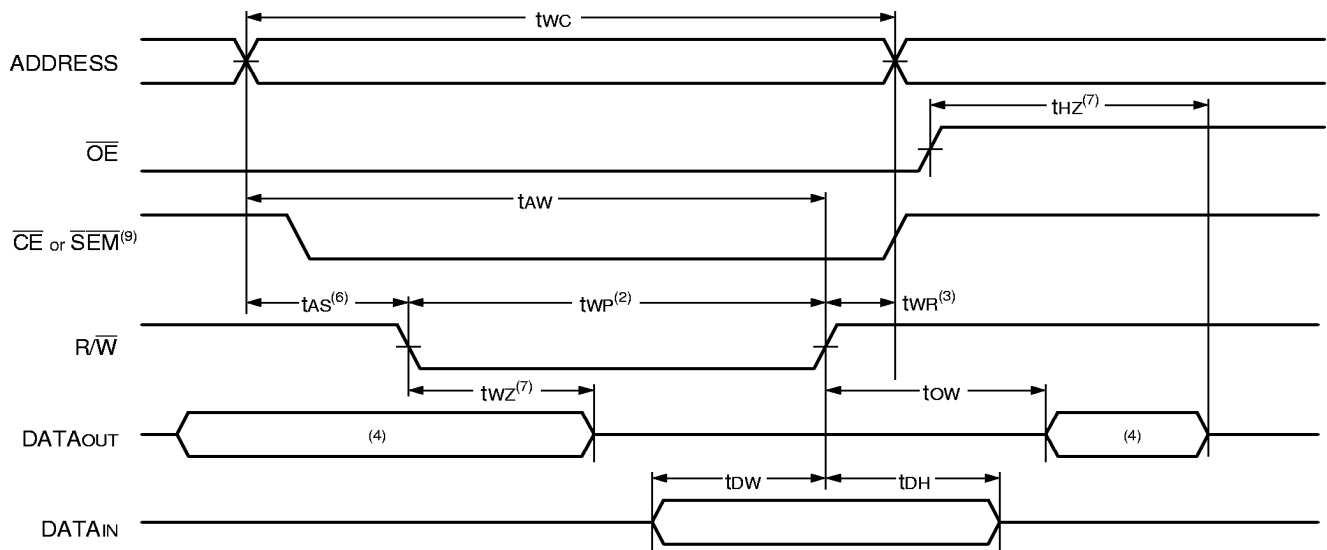
Symbol	Parameter	7006X35 Com'l & Military		7006X55 Com'l, Ind & Military		7006X70 Military Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	35	—	55	—	70	—	ns
tEW	Chip Enable to End-of-Write ⁽³⁾	30	—	45	—	50	—	ns
tAW	Address Valid to End-of-Write	30	—	45	—	50	—	ns
tAS	Address Set-up Time ⁽³⁾	0	—	0	—	0	—	ns
tWP	Write Pulse Width	25	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	30	—	40	—	ns
tHZ	Output High-Z Time ^(1,2)	—	15	—	25	—	30	ns
tDH	Data Hold Time ⁽⁴⁾	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z ^(1,2)	—	15	—	25	—	30	ns
tOW	Output Active from End-of-Write ^(1,2,4)	0	—	0	—	0	—	ns
tSWRD	SEM Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	SEM Flag Contention Window	5	—	5	—	5	—	ns

2739 tbl 14b

NOTES:

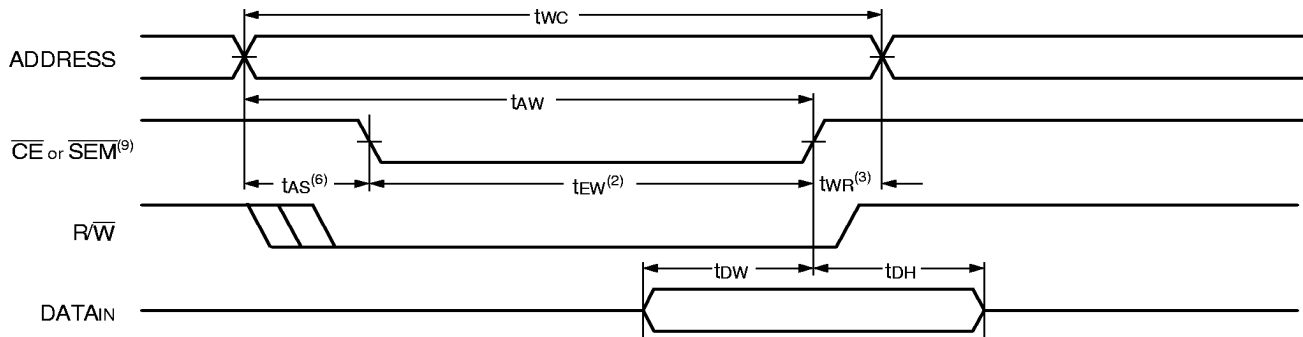
1. Transition is measured $\pm 500\text{mV}$ from Low or High-impedance voltage with load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested but not tested.
3. To access RAM, $\overline{\text{CE}} = \text{V}_{\text{IL}}$, $\overline{\text{SEM}} = \text{V}_{\text{IH}}$. To access semaphore, $\overline{\text{CE}} = \text{V}_{\text{IH}}$ and $\overline{\text{SEM}} = \text{V}_{\text{IL}}$. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 'X' in part numbers indicates power rating (S or L).
6. Industrial temperature: for other speeds, packages and powers contact your sales office.

Timing Waveform of Write Cycle No. 1, $\overline{R/\overline{W}}$ Controlled Timing^(1,5,8)



2739 drw 09

Timing Waveform of Write Cycle No. 2, \overline{CE} Controlled Timing^(1,5)

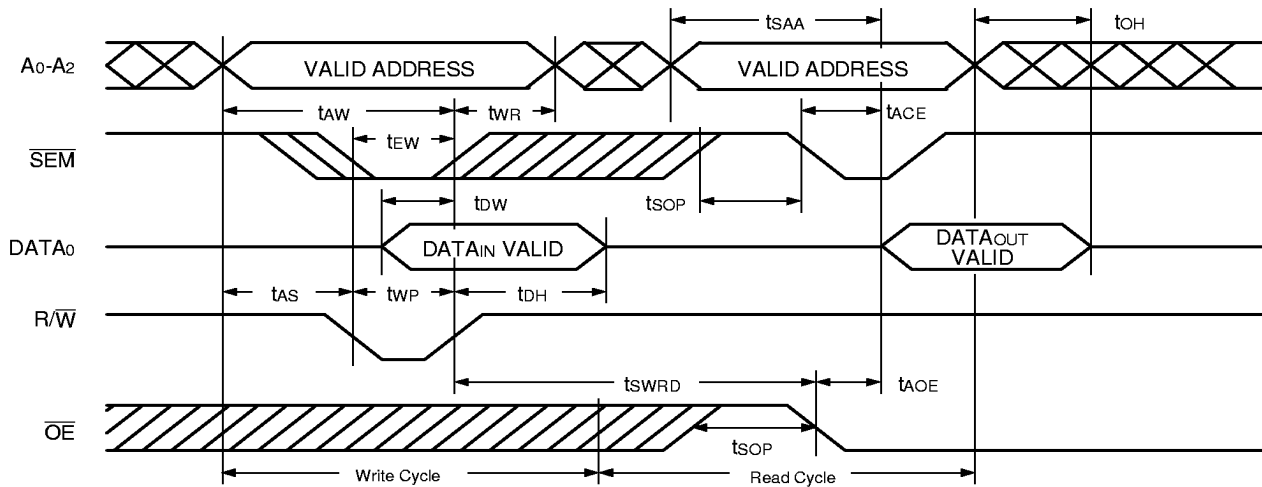


2739 drw 10

NOTES:

1. $\overline{R/\overline{W}}$ or \overline{CE} must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a LOW \overline{CE} and a LOW $\overline{R/\overline{W}}$ for memory array writing cycle.
3. t_{WR} is measured from the earlier of \overline{CE} or $\overline{R/\overline{W}}$ (or \overline{SEM} or $\overline{R/\overline{W}}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the \overline{CE} or \overline{SEM} LOW transition occurs simultaneously with or after the $\overline{R/\overline{W}}$ low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, \overline{CE} or $\overline{R/\overline{W}}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured by $\pm 500\text{mV}$ from steady state with the Output Test Load (Figure 2).
8. If \overline{OE} is LOW during $\overline{R/\overline{W}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{OW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If \overline{OE} is HIGH during an $\overline{R/\overline{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .
9. To access RAM, $\overline{CE} = V_{IL}$ and $\overline{SEM} = V_{IH}$. To access semaphore $\overline{CE} = V_{IH}$ and $\overline{SEM} = V_{IL}$. t_{EW} must be met for either condition.

Timing Waveform of Semaphore Read after Write Timing, Either Side⁽¹⁾

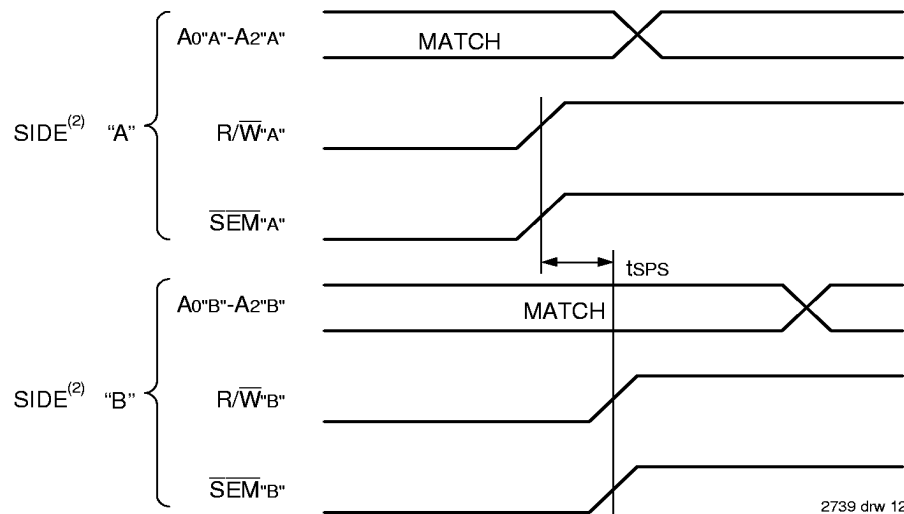


2739 drw 11

NOTE:

1. $\overline{CE} = V_{IH}$ for the duration of the above timing (both write and read cycle).

Timing Waveform of Semaphore Write Contention^(1,3,4)



2739 drw 12

NOTES:

1. $D_{OR} = D_{OL} = V_{IL}$, $\overline{CE}_R = \overline{CE}_L = V_{IH}$, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from $R/\overline{W}\cdot A$ or $\overline{SEM}\cdot A$ going HIGH to $R/\overline{W}\cdot B$ or $\overline{SEM}\cdot B$ going HIGH.
4. If t_{SPS} is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(6,7)

Symbol	Parameter	7006X15 Com'l Only		7006X17 Com'l Only		7006X20 Com'l & Military		7006X25 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/S=VIH)										
tBAA	BUSY Access Time from Address Match	—	15	—	17	—	20	—	20	ns
tBDA	BUSY Disable Time from Address Not Matched	—	15	—	17	—	20	—	20	ns
tBAC	BUSY Access Time from Chip Enable Low	—	15	—	17	—	20	—	20	ns
tBDC	BUSY Access Time from Chip Enable High	—	15	—	17	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time ⁽²⁾	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data ⁽³⁾	—	18	—	18	—	30	—	30	ns
tWH	Write Hold After BUSY ⁽⁶⁾	12	—	13	—	15	—	17	—	ns
BUSY TIMING (M/S=VIL)										
tWB	BUSY Input to Write ⁽⁴⁾	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY ⁽⁶⁾	12	—	13	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING										
tWDD	Write Pulse to Data Delay ⁽¹⁾	—	30	—	30	—	45	—	50	ns
tDD	Write Data Valid to Read Data Delay ⁽¹⁾	—	25	—	25	—	35	—	35	ns

2739 tbl 15a

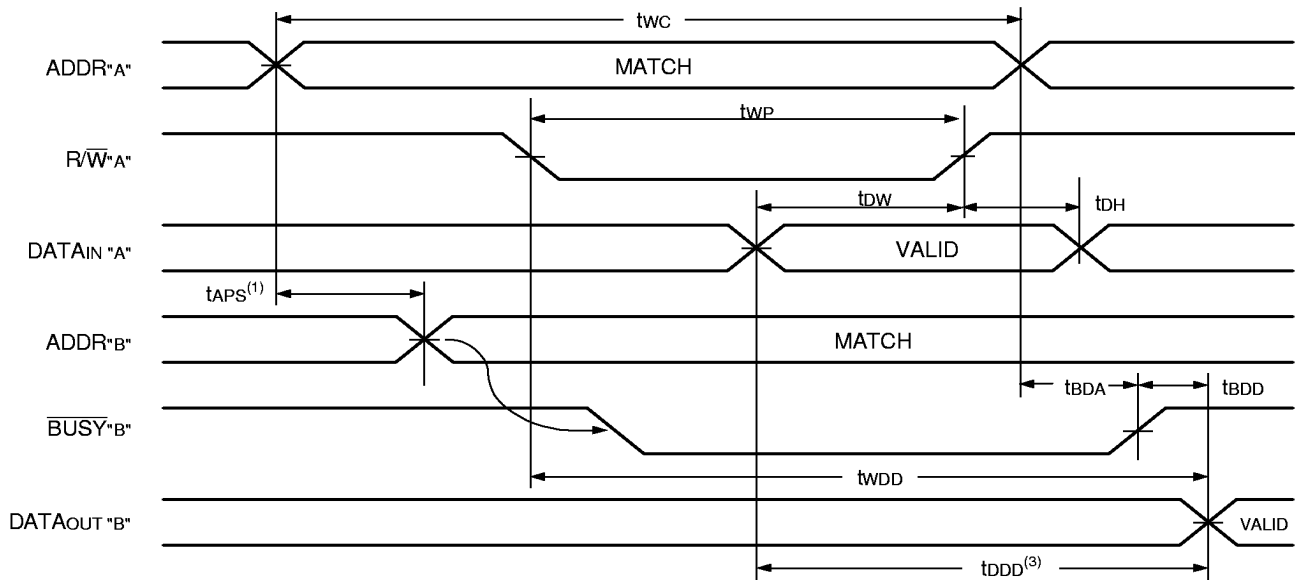
Symbol	Parameter	7006X35 Com'l & Military		7006X55 Com'l, Ind & Military		7006X70 Military Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/S=VIH)								
tBAA	BUSY Access Time from Address Match	—	20	—	45	—	45	ns
tBDA	BUSY Disable Time from Address Not Matched	—	20	—	40	—	40	ns
tBAC	BUSY Access Time from Chip Enable Low	—	20	—	40	—	40	ns
tBDC	BUSY Access Time from Chip Enable High	—	20	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time ⁽²⁾	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data ⁽³⁾	—	35	—	40	—	45	ns
tWH	Write Hold After BUSY ⁽⁵⁾	25	—	25	—	25	—	ns
BUSY TIMING (M/S=VIL)								
tWB	BUSY Input to Write ⁽⁴⁾	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY ⁽⁵⁾	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay ⁽¹⁾	—	60	—	80	—	95	ns
tDD	Write Data Valid to Read Data Delay ⁽¹⁾	—	45	—	65	—	80	ns

NOTES:

2739 tbl 15b

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\bar{B}USY$ ".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} – t_{WP} (actual) or t_{DD} – t_{OW} (actual).
4. To ensure that the write cycle is inhibited with port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention with port "A".
6. 'X' is part numbers indicates power rating (S or L).
7. Industrial temperature: for other speeds, packages and powers contact your sales office.

Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}^{(2,5)}$ ($M/\overline{S} = V_{IH}$)⁽⁴⁾

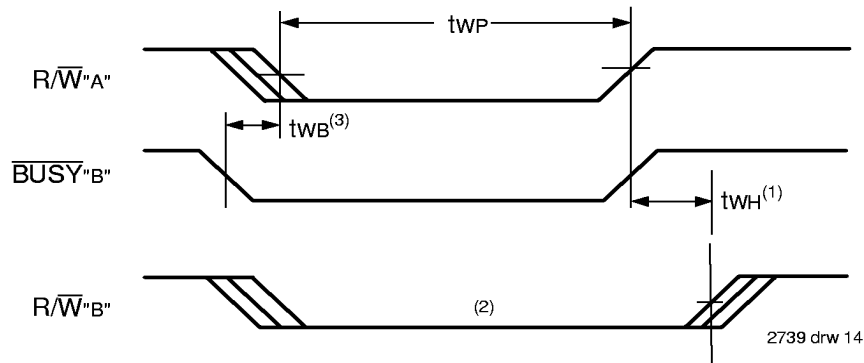


NOTES:

1. To ensure that the earlier of the two ports wins, t_{APS} is ignored for $M/\overline{S} = V_{IL}$ (SLAVE).
2. $\overline{CE_L} = \overline{CE_R} = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. If $M/\overline{S} = V_{IL}$ (slave) then \overline{BUSY} is input ($\overline{BUSY}_A = V_{IH}$) and $\overline{BUSY}_B =$ "don't care", for this example.
5. All timing is the same for left and right port. Port "A" may be either left or right port. Port "B" is the port opposite from Port "A".

2739 drw 13

Timing Waveform of Write with \overline{BUSY}

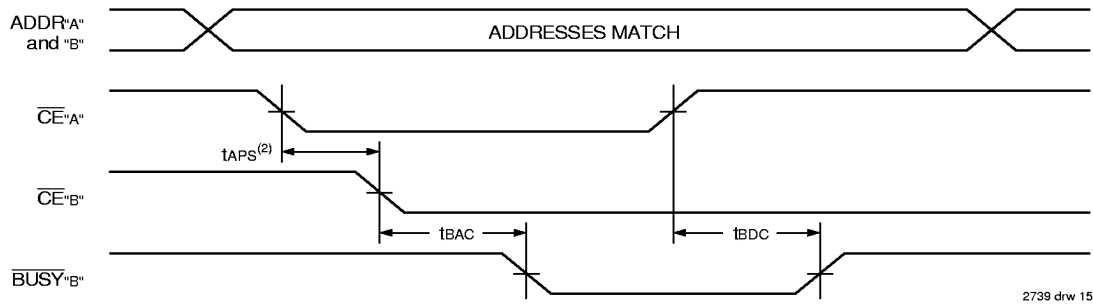


2739 drw 14

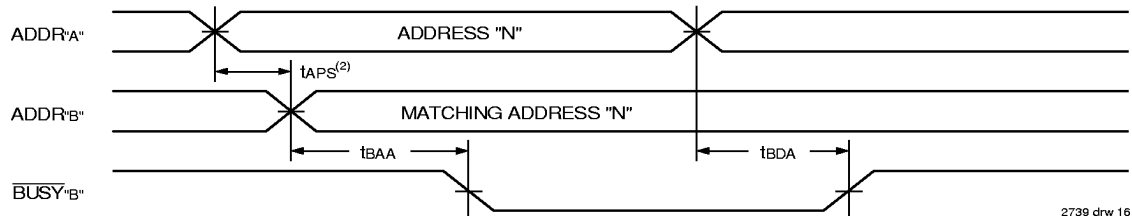
NOTES:

1. t_{WH} must be met for both \overline{BUSY} input (slave) and output (master).
2. \overline{BUSY} is asserted on Port "B", blocking R/\overline{W}_B , until \overline{BUSY}_B goes HIGH.
3. t_{wB} is only for the 'Slave' Version.

Waveform of \overline{BUSY} Arbitration Controlled by \overline{CE} Timing⁽¹⁾ ($M/\overline{S} = V_{IH}$)



Waveform of \overline{BUSY} Arbitration Cycle Controlled by Address Match Timing⁽¹⁾ ($M/\overline{S} = V_{IH}$)



NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the \overline{BUSY} signal will be asserted on one side or another but there is no guarantee on which side \overline{BUSY} will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,2)

Symbol	Parameter	7006X15 Com'l Only		7006X17 Com'l Only		7006X20 Com'l & Military		7006X25 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING										
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	15	—	20	—	20	ns
tNR	Interrupt Reset Time	—	15	—	15	—	20	—	20	ns

2739 tbl 16a

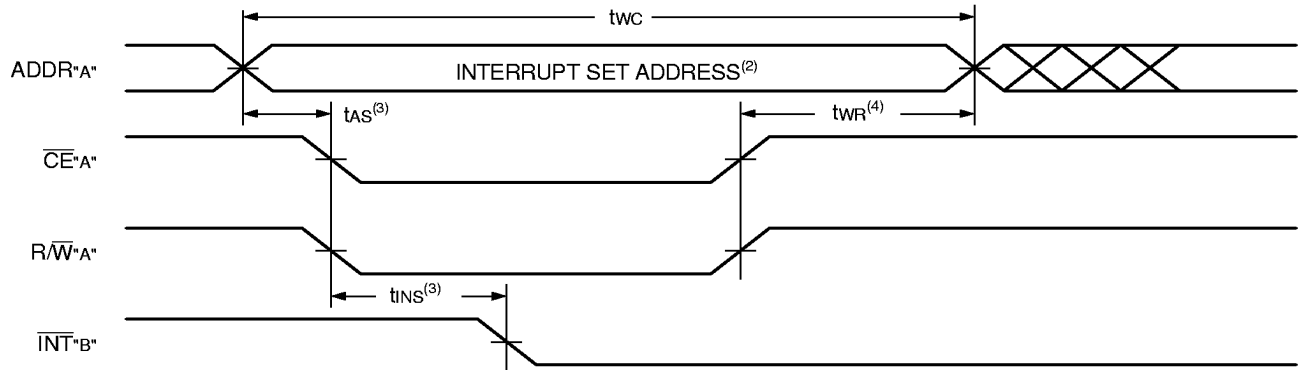
Symbol	Parameter	7006X35 Com'l & Military		7006X55 Com'l, Ind & Military		7006X70 Military Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	40	—	50	ns
tNR	Interrupt Reset Time	—	25	—	40	—	50	ns

2739 tbl 16b

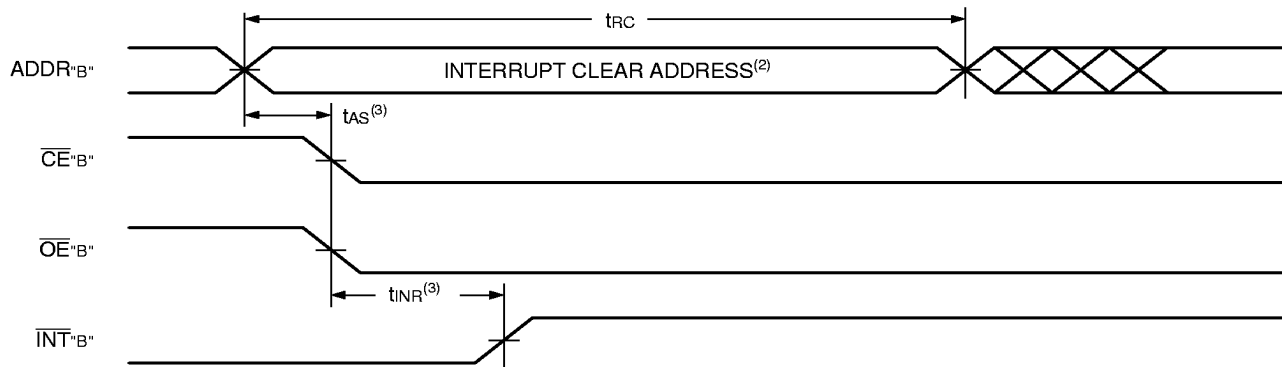
NOTES:

1. 'X' in part numbers indicates power rating (S or L).
2. Industrial temperature: for other speeds, packages and powers contact your sales office.

Waveform of Interrupt Timing⁽¹⁾



2739 drw 17



2739 drw 18

NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. See Interrupt Truth Table III.
3. Timing depends on which enable signal (\overline{CE} or R/\overline{W}) is asserted last.
4. Timing depends on which enable signal (\overline{CE} or R/\overline{W}) is de-asserted first.

Truth Tables

Truth Table III — Interrupt Flag^(1,4)

Left Port					Right Port					Function
R/ \overline{W} L	\overline{CE} L	\overline{OE} L	A13L-A0L	\overline{INT} L	R/ \overline{W} R	\overline{CE} R	\overline{OE} R	A13R-A0R	\overline{INT} R	
L	L	X	3FFF	X	X	X	X	X	L ⁽²⁾	Set Right \overline{INT} R Flag
X	X	X	X	X	X	L	L	3FFF	H ⁽³⁾	Reset Right \overline{INT} R Flag
X	X	X	X	L ⁽³⁾	L	L	X	3FFF	X	Set Left \overline{INT} L Flag
X	L	L	3FFE	H ⁽²⁾	X	X	X	X	X	Reset Left \overline{INT} L Flag

2739 tbl 17

NOTES:

1. Assumes \overline{BUSY} L = \overline{BUSY} R = VIH.
2. If \overline{BUSY} L = VIL, then no change.
3. If \overline{BUSY} R = VIL, then no change.
4. \overline{INT} R and \overline{INT} L must be initialized at power-up.

Truth Table IV — Address $\overline{\text{BUSY}}$ Arbitration

Inputs			Outputs		Function
$\overline{\text{CE}}$	$\overline{\text{CE}}_R$	A0L-A13L A0R-A13R	$\overline{\text{BUSY}}_L^{(1)}$	$\overline{\text{BUSY}}_R^{(1)}$	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit ⁽³⁾

2739 tbl 18

NOTES:

1. Pins $\overline{\text{BUSY}}_L$ and $\overline{\text{BUSY}}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{\text{BUSY}}_x$ outputs on the IDT7006 are push pull, not open drain outputs. On slaves the $\overline{\text{BUSY}}_x$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{\text{BUSY}}_L$ or $\overline{\text{BUSY}}_R$ = LOW will result. $\overline{\text{BUSY}}_L$ and $\overline{\text{BUSY}}_R$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{\text{BUSY}}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{\text{BUSY}}_R$ outputs are driving LOW regardless of actual logic level on the pin.

Truth Table V — Example of Semaphore Procurement Sequence^(1,2,3)

Functions	D0 - D7 Left	D0 - D7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

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NOTES:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7006.
2. There are eight semaphore flags written to via I/O₀ and read from all I/O's. These eight semaphores are addressed by A₀ - A₇.
3. $\overline{\text{CE}} = \text{V}_{IH}$, $\text{SEM} = \text{V}_{IL}$ to access the semaphores. Refer to the Semaphore Read/Write Control Truth Table.

Functional Description

The IDT7006 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7006 has an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{\text{CE}}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

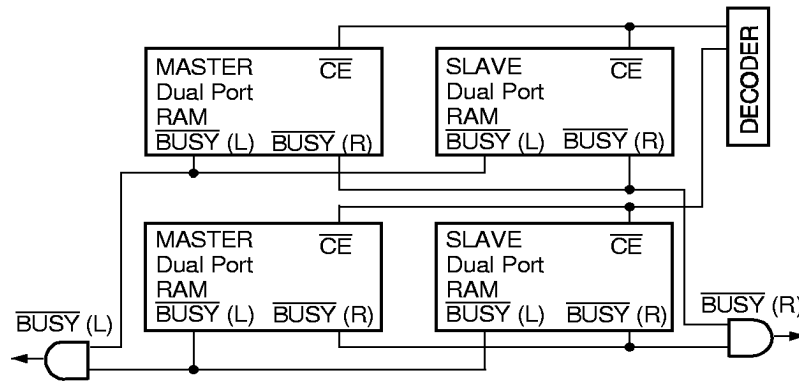
Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{\text{INT}}_L$) is asserted when the right port writes to memory location 3FFE (HEX) where a write is defined as $\overline{\text{CE}} = \text{R}/\overline{\text{W}} = \text{V}_{IL}$ per the Truth Table.

The left port clears the interrupt by reading address location 3FFE access when $\overline{\text{CE}}_R = \text{OER} = \text{V}_{IL}$, R/W is a "don't care". Likewise, the right port interrupt flag ($\overline{\text{INT}}_R$) is asserted when the left port writes to memory location 3FFF (HEX) and to clear the interrupt flag ($\overline{\text{INT}}_R$), the right port must read the memory location 3FFF. The message (8 bits) at 3FFE or 3FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM



2739 drw 19

Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7006 RAMs.

have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The $\overline{\text{BUSY}}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{\text{BUSY}}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{\text{BUSY}}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{\text{BUSY}}$ outputs together and use any $\overline{\text{BUSY}}$ indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of $\overline{\text{BUSY}}$ logic is not desirable, the $\overline{\text{BUSY}}$ logic can be disabled by placing the part in slave mode with the $\overline{\text{M/S}}$ pin. Once in slave mode the $\overline{\text{BUSY}}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{\text{BUSY}}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{\text{BUSY}}$ pin for that port LOW.

The $\overline{\text{BUSY}}$ outputs on the IDT 7006 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the $\overline{\text{BUSY}}$ indication for the resulting array requires the use of an external AND gate.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT7006 RAM array in width while using $\overline{\text{BUSY}}$ logic, one master part is used to decide which side of the RAMs array will receive a $\overline{\text{BUSY}}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the $\overline{\text{BUSY}}$ signal as a write inhibit signal. Thus on the IDT7006 RAM the $\overline{\text{BUSY}}$ pin is an output if the part is used as a master ($\overline{\text{M/S}}$ pin = V_{IH}), and the $\overline{\text{BUSY}}$ pin is an input if the part used as a slave ($\overline{\text{M/S}}$ pin = V_{IL}) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating $\overline{\text{BUSY}}$ on one side of the array and another master indicating $\overline{\text{BUSY}}$ on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{\text{BUSY}}$ arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In

a master/slave array, both address and chip enable must be valid long enough for a $\overline{\text{BUSY}}$ flag to be output from the master before the actual write pulse can be initiated with the R/W signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7006 is an extremely fast Dual-Port 16K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{\text{CE}}$, the Dual-Port RAM enable, and $\overline{\text{SEM}}$, the semaphore enable. The $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table I where $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ are both HIGH.

Systems which can best use the IDT7006 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7006s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7006 does not use its semaphore flags to control

any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7006 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a LOW input on the \overline{SEM} pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, \overline{OE} , and R/\overline{W}) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0–A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table V). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select (\overline{SEM}) and output enable (\overline{OE}) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must

cause either signal (\overline{SEM} or \overline{OE}) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Truth Table V). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7006's Dual-Port RAM. Say the 16K x 8 RAM was to be divided into two 8K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used

to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can

even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices have determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

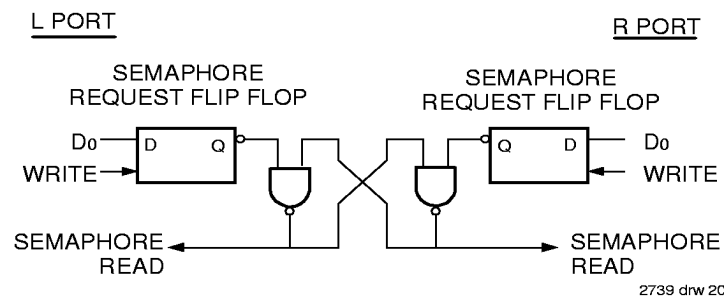
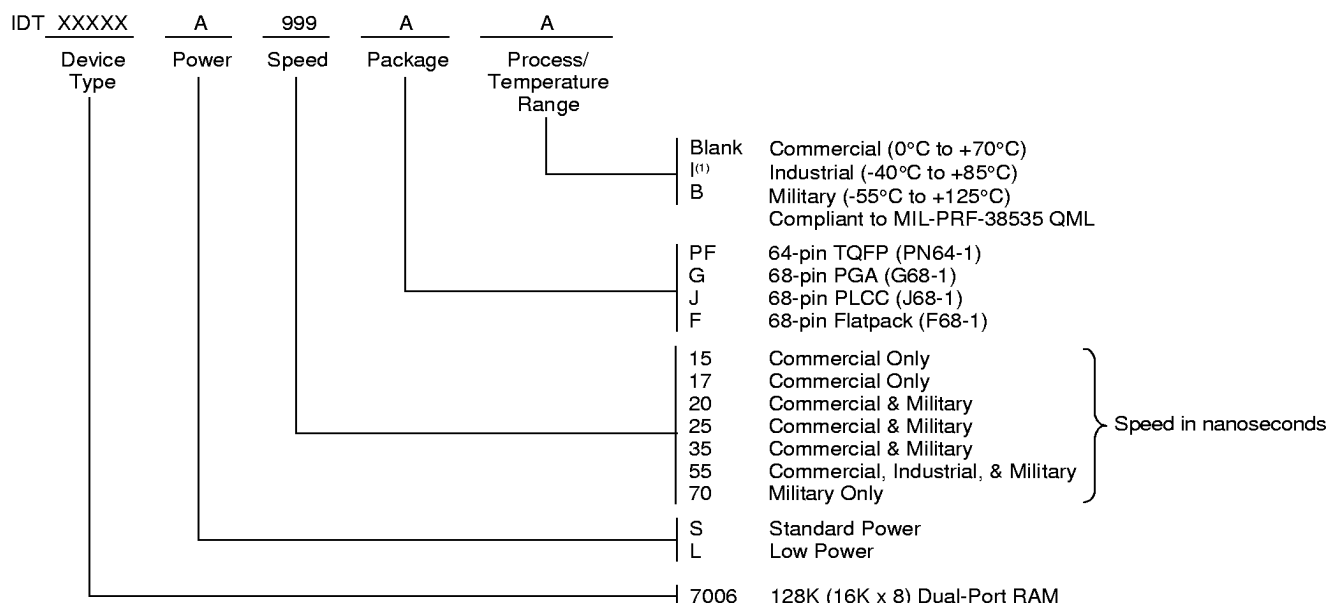


Figure 4. IDT7006 Semaphore Logic

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