HT80232

Ethernet Controller/PCI (ECON-PCI)

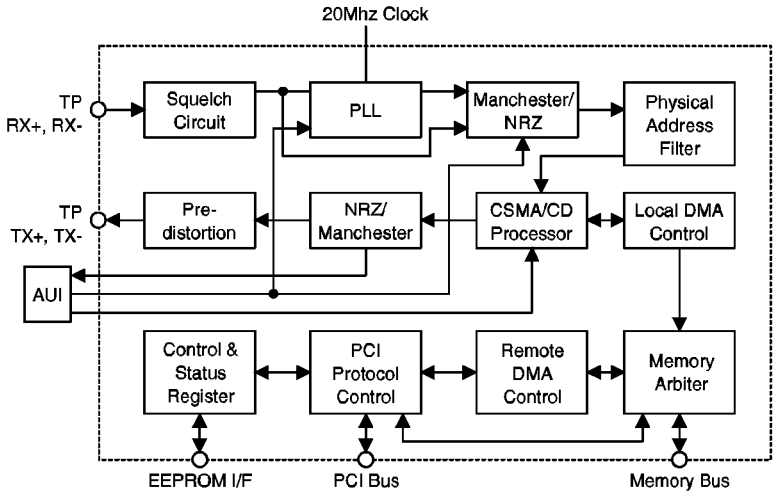
Features

- Single chip Ethernet controller for PCI bus interface
- Register compatible with NE2000
- External 15ns access time SRAM for data transfer
- Integrated 10BaseT TP interface
  - Smart squelch circuit with programmable threshold for receiver
  - Built-in transmitter pre-equalization circuitry
- Direct drive LED status indicators for transmitting, receiving, collision, and BNC
  - Flashing LED for packet transmitting status
  - Flashing LED for packet receiving status
  - LED normally on for TP link up
  - LED normally in active for collision status
  - LED normally off for 10Base2 selection and indication
- Integrated TP interface function
  - Link integrity test
  - Automatic selection between TP and AUI
  - Automatic polarity detection and correction
- Full IEEE 802.3 AUI
  - Meets 10Base5 and 10Base2 standards
  - Thin-net or Thick-net enable signal
- Jumperless configuration with programming interface to EEPROM
- Support Boot ROM for diskless operation
- Optional Full duplex operation with speed up to 20Mbps
- Early interrupt (cut through) mode allows parallel processing of packet data during reception
- Software controllable power down feature
- Single +5V supply, standard CMOS technology
- 100-pin QFP package

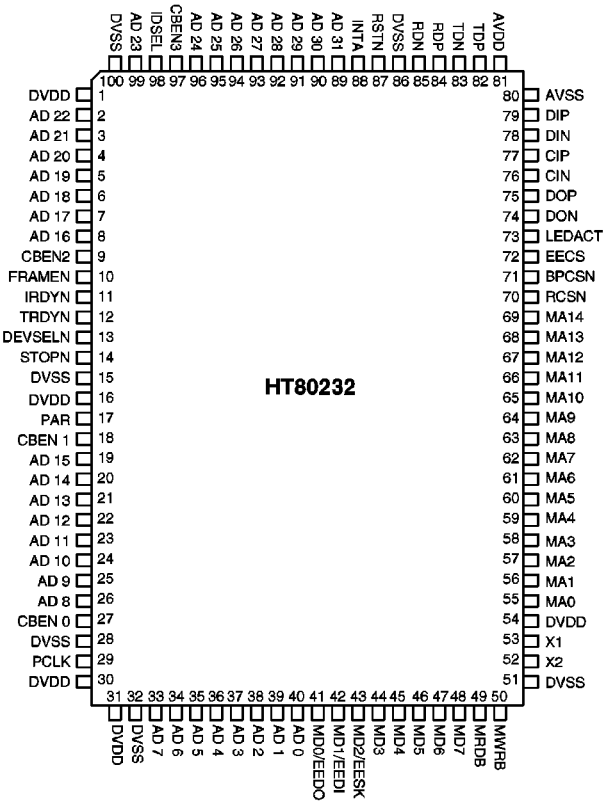
General Description

The HT80232 ECON-PCI is a 10MBPS Ethernet Controller for the PCI bus. Integrating twisted-pair interface and AUI, the ECON-PCI provides an easy way to implement a single chip network adapter for the PCI bus. In addition, the ECON-PCI provides better data transfer performance than traditional NE2000 Ethernet adapters by supporting a better interrupt handling scheme and remote DMA data pre-fetch architecture. Complying with PCI specification 2.1, the ECON-PCI utilizes the auto-loading function to support PCI "plug and play" function and to prevent the adapter card from conflicting with other resources. The I/O pre-fetch function allows the host to speed up remote DMA , boosting the bus efficiency. By programming the ECON-PCI to run in early interrupt mode, the host can improve the remote DMA performance. The UTP/AUI auto-switching function provides the user with an easy-to-use medium selection. Built-in smart squelch circuit eliminates noise, preventing the receiver from misinterpreting abnormal data signals.

Block Diagram



Pin Diagram



Pin Description

PCI bus interface

Pin No.	Pin Name	I/O	Description
89~96 99, 2~8 19~26 33~40	AD[31:0] AD31~AD24 AD23, AD22~AD16 AD15~AD8 AD7~AD0	I/O	PCI address and data bus: Multiplexed PCI address/data bus pins. A bus transaction begins with an address phase followed by one or several data phases. During the address phase, the AD bus contains the physical address. During the data phase the AD bus contains the data.
97, 9, 18, 27	CBEN[3:0]	I	Bus command and byte enable : Multiplexed bus command and byte enable signals. During the address phase the bus command is presented on these pins. During the data phase these pins indicate the byte enable signal issued by the bus initiator.
10	FRAMEN	I	Bus cycle frame: This signal is driven by the initiator to indicate the beginning of the transaction. It is removed when the transaction reaches the final data phase.
11	IRDYN	I	Initiator ready: when active, it indicates the initiator is ready to complete the data phase. IRDYN is asserted during a write operation to indicate that valid data is present on the AD bus. During a read operation, the initiator asserts IRDYN to indicate that the initiator is ready to accept data.
12	TRDYN	O, TS	Target ready: when active, it indicates the target is ready to complete the data phase. TRDYN is asserted by the bus slave. During the read operation, it indicates that valid data is present on the AD lines. During the write cycle, it indicates that the target is ready to accept data.
13	DEVSELN	O, TS	Device select: When active, it indicates the ECON-PCI has decoded its address as the target of the current access.
14	STOPN	O, TS	Stop: when active, it indicates the target is requesting the master to stop the current transaction..
17	PAR	I/O	Parity: An even parity bit across AD bus and CBE bus is generated to ensure the validity of the bus transaction.
29	PCLK	I	PCI bus clock: PCI bus clock.
87	RSTN	I	Reset: Asynchronous system reset signal
88	INTAN	OD	Interrupt A: Open drain, level sensitive, active low signal used to indicate the interrupt request to the host.
98	IDSEL	I	Initialization device select: Used as a chip select during configuration read and write transaction.

Network interface

Pin No.	Pin Name	I/O	Description
52	X2	O	Crystal oscillator output: Oscillator output. Left open if X1 is used as an external clock input.
53	X1	I	Crystal oscillator input: Oscillator or external clock input.
73	LEDACT	OD	Activity LED: An open drain active low output. It indicates the transmission/reception to/from the TP is in progress. It reflects the cable link status and traffic status by means of the following signal. 1. Normally on: Both ends of the UTP cable is linked and no traffic passes through the UTP cable. 2. Blinking: Data passing through either UTP or AUI port. 3. Normally off: AUI port is selected and no traffic passes through the cable.
75, 74	DOP, DON	O	AUI transmit output: Differential current mode driver. This pair of signals send the Manchester-encoded data to the AUI DO circuitry through a transformer coupler. A local terminator resistor of 75Ω should be placed between these two pins.
77, 76	CIP, CIN	I	AUI collision input: Differential collision (SQE) signal input from AUI. The SQE signal is 10MHZ +/- 15% square wave.
79, 78	DIP, DIN	I	AUI receive input: Differential receive input pair from the AUI.
82, 83	TDP, TDN	O	Twisted-pair transmit outputs: Differential current mode driver. This pair of signals send pre-equalized TP data signal to the TP network medium through a transformer. A local 100 Ω terminator resistor should be placed between these two pins.
84, 85	RDP, RDN	I	Twisted pair receive inputs: Differential input pair from the TP interface.

External memory support

Pin No.	Pin Name	I/O	Description
48~41	MD[7:0]	I/O	Memory data bus: These pins form the external SRAM and ROM data buses
43, 42, 41	MD2(EESK), MD1(EEDI), MD0(EEDO)	I/O(O), I/O(O), I/O(I)	EEPROM control signals: These dual purpose pins are interface signals used to access either EEPROM or the external RAM/ROM. If the control bit EEPEN in EEPCMD register is set high and the STOP bit of CR is asserted, these three pins are used to control the clock, DI and DO of the EEPROM respectively; otherwise these pins are used as the memory data bus D0, D1 and D2.

Pin No.	Pin Name	I/O	Description
49	MRDN	O	Memory read: Active low signal, read strobe. When active, the ECON-PCI reads data from external SRAM.
50	MWRN	O	Memory write: Active low signal, write strobe. When active, the ECON-PCI writes data to external SRAM.
69-55	MA[14:0]	O	Memory address bus: External RAM or Boot ROM address bus. These are 14 address lines can cover up to 16K bytes of RAM space. If Boot ROM is enabled, the fifteenth address line MA14 is used to cover up to 32K bytes of space.
71	BPCSB	O	Boot PROM chip select: Active low signal. The external ROM is enabled by setting this pin low.
72	EECS	O	EEPROM chip select: Chip select signal for the external EEPROM. An EEPROM is used to provide the configuration data and Ethernet Address.

Power supply & ground

Pin No.	Pin Name	I/O	Description
1, 16, 30, 31, 54	VDD	P	Positive 5V supply: Supply power to internal digital logic.
15, 28, 32, 51, 86, 100	VSS	G	Negative supply: Digital ground.
81	VDDA	P	Analog 5V supply: Supply power to analog circuit.
80	VSSA	G	Negative supply: Analog ground.

Absolutely Maximum Rating*

Supply Voltage ..... –0.5V to 7V

Input Voltage..... V_{SS}–0.5V to V_{DD}+5V

Lead Soldering Temperature ..... 270°C
(Soldering at a maximum of 10 seconds)

Storage Temperature..... –50°C to 100°C

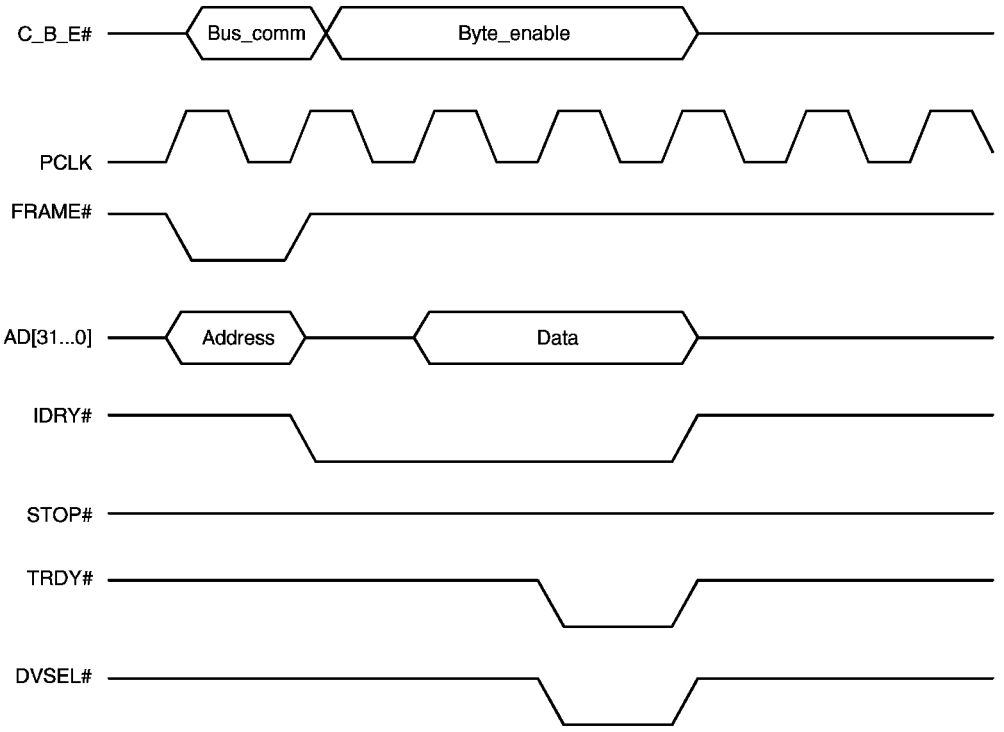
Operating Temperature..... 0°C to 65°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

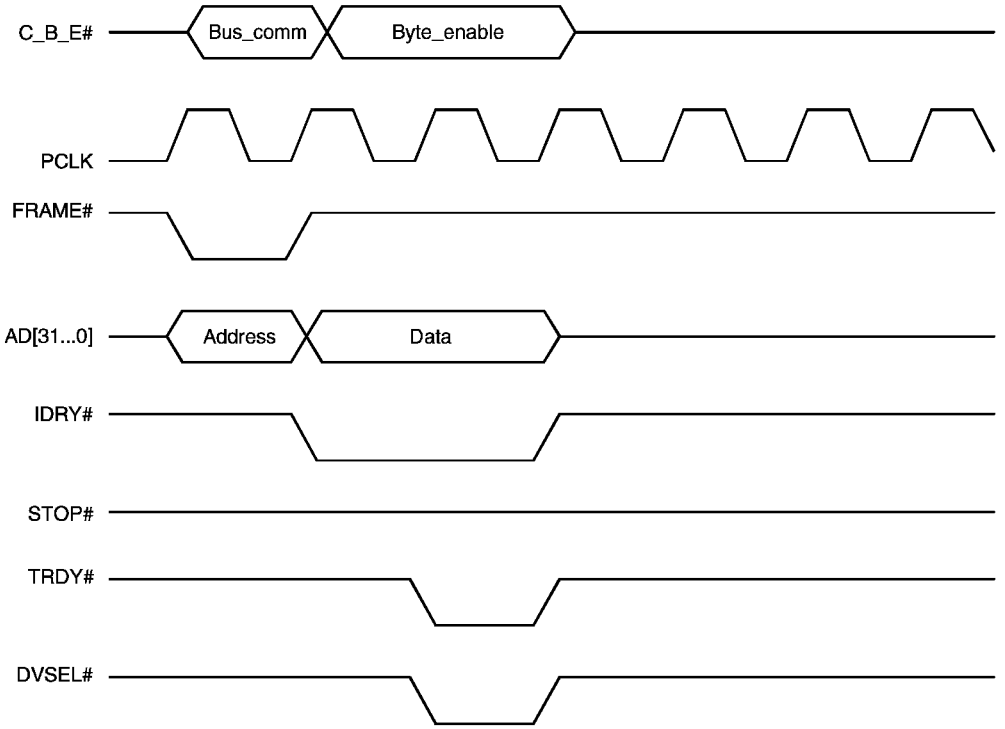
Electrical Characteristics

Parameter	Conditions	Maximum
Power Supply Current (No TX, RX Activity)	V_{DD}@5V, Ambient Temperature@25°C	30mA
Power Supply Current (Both TX and RX Active)	V_{DD}@5V, Ambient Temperature@25°C	70mA

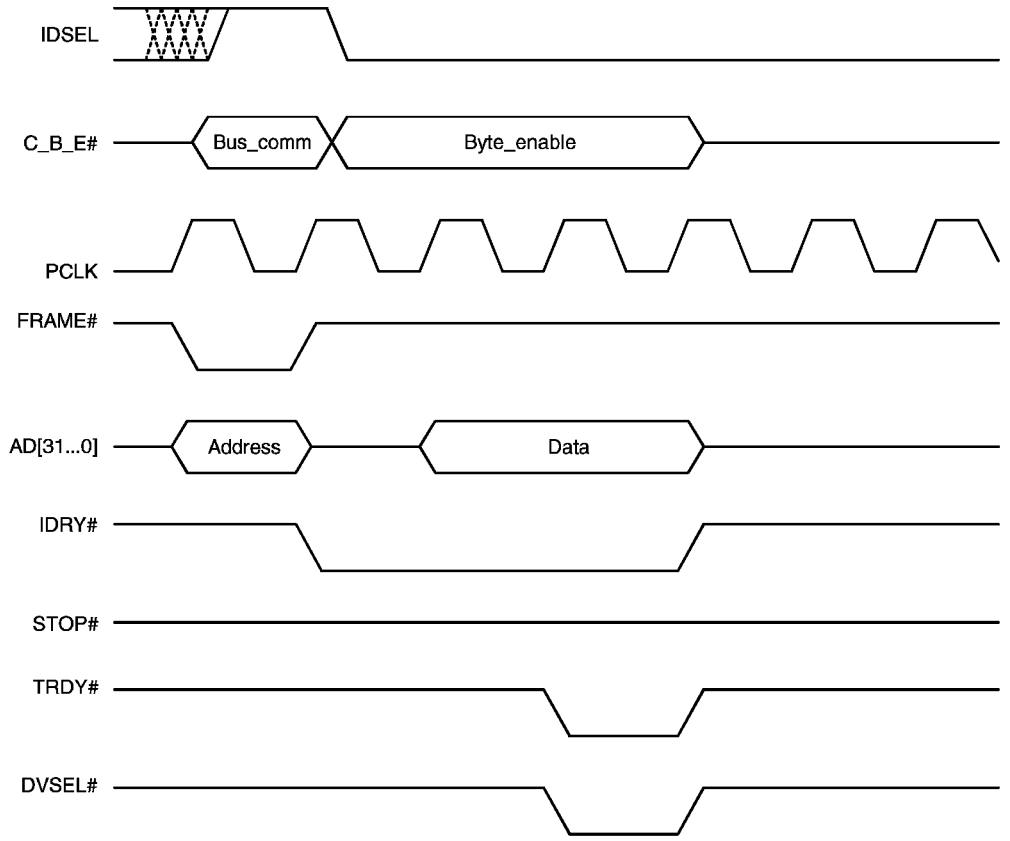
Switching Characteristics



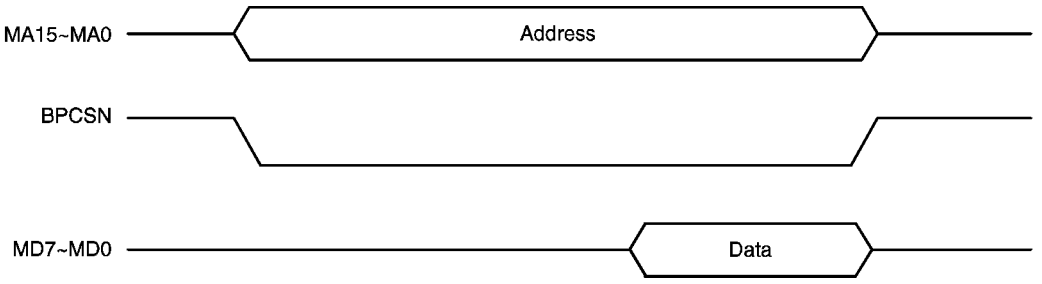
PCI bus I/O READ transaction



PCI bus I/O WRITE data transaction



PCI configuration READ transaction



ROM read cycle

Registers

MAC command and status registers

Page 0 registers (PS1=0 , PS0=0)

Address	Read	Write
00H	CR: Command Register	CR: Command Register
01H	RMBC0: Receiver DMA byte counter 0	PSTART: Page Start Register
02H	RMBC1: Receiver DMA byte counter 1	PSTOP: Page Stop Register
03H	BNRY: Boundary Pointer	BNRY: Boundary Pointer
04H	TSR: Transmit Status Register	TPSR: Transmit Page Start Register
05H	NCR: Number of Collision Register	TBCR0: Transmit Byte Count Register 0
06H	Reserved	TBCR1: Transmit Byte Count Register 1
07H	ISR: Interrupt Status Register	ISR: Interrupt Status Register
08H	CRD0: Current Remote DMA Address 0	RSAR0: Remote Start Address Register 0
09H	CRD1: Current Remote DMA Address 1	RSAR0: Remote Start Address Register 1
0AH	Reserved	RBCR0: Remote Byte Count Register 0
0BH	Reserved	RBCR1: Remote Byte Count Register 1
0CH	RSR: Receive Status Register	RCR: Receive Configuration Register
0DH	TC0: Tally Counter 0 (Frame Alignment Error)	TCR: Transmit Configuration Register
0EH	TC1: Tally Counter 1 (CRC Error)	DCR: Data Configuration Register
0FH	TC2: Tally Counter 2 (Missed Packet)	IMR: Interrupt Mask Register

Page 1 registers (PS1=0, PS0=1)

Address	Read	Write
00H	CR: Command Register	CR: Command Register
01H	PAR0: Physical Address Register 0	PAR0: Physical Address Register 0
02H	PAR1: Physical Address Register 1	PAR0: Physical Address Register 1
03H	PAR2: Physical Address Register 2	PAR0: Physical Address Register 2
04H	PAR3: Physical Address Register 3	PAR0: Physical Address Register 3
05H	PAR4: Physical Address Register 4	PAR0: Physical Address Register 4
06H	PAR5: Physical Address Register 5	PAR0: Physical Address Register 5
07H	CPR: Current Page Register	CPR: Current Page Register
08H	MAR0: Multicast Address 0	MAR0: Multicast Address 0

Address	Read	Write
09H	MAR1: Multicast Address 1	MAR1: Multicast Address 1
0AH	MAR2: Multicast Address 2	MAR2: Multicast Address 2
0BH	MAR3: Multicast Address 3	MAR3: Multicast Address 3
0CH	MAR4: Multicast Address 4	MAR4: Multicast Address 4
0DH	MAR5: Multicast Address 5	MAR5: Multicast Address 5
0EH	MAR6: Multicast Address 6	MAR6: Multicast Address 6
0FH	MAR0: Multicast Address 0	MAR0: Multicast Address 0

Page 0 registers (PS1=1 , PS0=0)

Address	Read	Write
00H	CR: Command Register	CR: Command Register
01H	PSTART: Page Start Register	Reserved
02H	PSTOP: Page Stop Register	Reserved
03H	Reserved	Reserved
04H	TPSR: Transmit Page Start Address	Reserved
05H	Reserved	Reserved
06H	Reserved	Reserved
07H	Reserved	Reserved
08H	Reserved	Reserved
09H	Reserved	Reserved
0AH	Reserved	Reserved
0BH	Reserved	Reserved
0CH	RCR: Receive Configuration Register	Reserved
0DH	TCR: Transmit Configuration Register	Reserved
0EH	Reserved	Reserved
0FH	Reserved	Reserved

Command register (CR)

PS1	PS0	RDMA2	RDMA1	RDMA0	TXP	Start	Stop

Bit Location	Symbol	Function
0	Stop	Software reset command. Once this command is issued, no packets will be received or transmitted. Any packet in progress will continue until that process completes. To perform this command, this bit should be set to "1". To exit the reset state, this bit should be cleared and the Start bit must be set to "1".
1	Start	This bit is used to activated the controller either after power up or after the controller has been placed in a reset mode.
2	TXP	Transmit packet: This command must be issued to transmit a packet.
3	RDMA0	These three encoded bits control the operation of Remote DMA. To abort the Remote DMA in progress, RDMA2 should be set to "1". The Remote byte Count Register cleared when a Remote DMA has been aborted. RD2 RD1 RD0 0 0 0 N/A 0 0 1 Remote read 0 1 0 Remote write 0 1 1 Send packet 1 X X Abort/complete remote DMA
4	RDMA1	
5	RDMA2	
6	PS0	These two bits select which register page is to be accessed. PS1 PS0 0 0 Page 0 0 1 Page 1 1 0 Page 2 1 1 N/A
7	PS1	

Interrupt status register (ISR)

This register indicates the status of the interrupt. When an interrupt is generated, the interrupt service routine will read this register to identify the cause of the interrupt. The individual bit can be cleared by writing a "1" to the corresponding bit location.

RST	RDC	CNT	OVW	TXE	RXE	PTX	PRX

Bit Location	Symbol	Function
0	PRX	Packet received: This bit indicates the data packet was received without error.
1	PTX	Packet transmitted: This bit indicates the data packet was transmitted without error.
2	RXE	Receive error: Set when a data packet is received with one or more of the following errors: 1. Frame Alignment Error; 2. CRC Error ;3. Missed Packet
3	TXE	Transmit error: Set when a data packet is transmitted with excessive collision.

Bit Location	Symbol	Function
4	OVW	Overwrite warning: Set when the receive buffer ring resource has been exhausted.
5	CNT	Counter overflow: Set when one or more network tally counter overflow.
6	RDC	Remote DMA complete: Set when remote DMA operation completes.
7	RST	Reset status: Set when the controller enters the reset state and cleared when the start command is issued to the Command Register. This bit is also set when the receive buffer ring overflow occurs and cleared when one or more packets have been moved out.

Interrupt mask register (IMR)

The individual bit of this register can be programmed to mask/enable the corresponding interrupt.

An interrupt occurs when both the individual bit of the IMR and the corresponding bit of the ISR are set to "1". When the interrupt is masked during the active state of the corresponding interrupt status, the interrupt will be suspended. After the interrupt is unmasked, the interrupt will be generated as long as the corresponding interrupt status bit is set.

The bit definition is the same as that of the IMR except that bit 7 is reserved.

Transmit configuration register (TCR)

<table>
<tr><th>Bit Location</th><th>Symbol</th><th>Function</th></tr>
<tr><td>0</td><td>CRC</td><td>0: Append CRC
1: Inhibit CRC</td></tr>
<tr><td>1, 2</td><td>LB0, LB1</td><td>Loopback Control: These configuration bits set the type of loopback.
<table>
<tr><th>LB1</th><th>LB0</th><th>Meaning</th></tr>
<tr><td>0</td><td>0</td><td>Normal operation</td></tr>
<tr><td>0</td><td>1</td><td>Loopback through MAC</td></tr>
<tr><td>1</td><td>0</td><td>Loopback through Manchester Encoder/Manchester Decoder</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>4</td><td>COFST</td><td>Collision offset: This bit allows the backoff algorithm to be modified. 0: 802.3 backoff algorithm
1: Modified backoff alogorithm. For the first three collisions, the station has higher average backoff delay, making a lower priority.</td></tr>
</table>

Transmit status register (TSR)

Bit Location	Symbol	Function
0	PTX	Packet transmitted: Active high. The transmission has successfully completed.
2	COL	Transmission collided: The transmission encountered collision at least once.
3	ABT	Transmission aborted: The controller aborted the transmission because of excessive collision.
4	CRL	Carrier sense lost: This bit is set when the carrier is lost during the transmission. The transmission is not aborted in this case.
6	CDH	CD Heartbeat: This bit indicates the status of the received heartbeat signal. When the heartbeat signal is received, this bit is set to "0"; otherwise it is set to "1".
7	OWC	Out of window collision: Indicates that a collision occurred after a slot time.

Receive configuration register (RCR)

Bit Location	Symbol	Function
0	SEP	Save erroneous packet: 0:Packets with receive error are rejected. 1:Packets with receive error are accepted.
1	AR	Accept runt packet: 0:Packets less than 64 bytes are rejected. 1:Packets less than 64 bytes are accepted.
2	AB	Accept broadcast: 0:Packets with broadcast destination address are rejected. 1:Packets with broadcast destination address are accepted
3	AM	Accept multicast: 0:Packets with multicast destination address will be ignored. 1:Packets with multicast destination address will be checked.
4	PRM	Promiscuous physical: Enable the receiver to accept all packets with a physical address. 0:Accept the match physical address. 1:Accept all packets with physical address.

Receive status register (RSR)

This register records the status of the received packet. The contents of this register are written to buffer memory by the local DMA controller after reception of a packet. If packets with errors are accepted, this register will be also written to the buffer memory at the head of the corresponding erroneous packet.

Bit Location	Symbol	Function
0	PRX	Packet received without error
1	CRC	CRC error: Packets received with CRC error. This bit will also be set for Frame Alignment error.
2	FAE	Frame alignment error: The incoming data did not end at byte boundary and the CRC did not match at last byte boundary.
4	MPA	Missed packet: This bit is set when the received data packet cannot be saved because of no available buffer memory.
5	MUL	0: Physical address match 1: Multicast address match
7	DFR	Deferring: This bit is set when internal carrier sense or collision signal is generated.

Note: 1. Bit 3 and bit 6 are reserved. 2. All status bits in this register are high active.

Data configuration register (DCR)

Only bit 3 is meaningful. Other bits are reserved. A "0" enables the loopback mode. setting this bit to "1" sets the controller to normal operation mode.

Transmit page start register (TPSR)

This register points to the assembled packet to be transmitted. Only eight higher orders are specified since all transmit packets are assembled with a 256 byte boundary. The lower order addresses are initialized to zero..

Transmit byte count register 0, 1 (TBCR0,TBR1)

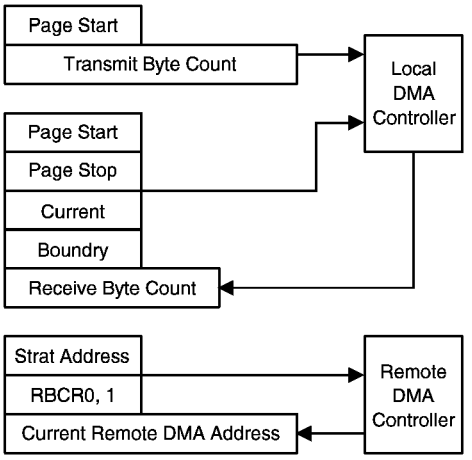
These registers indicate the length of the transmit packet in bytes. This count should include the address and the actual data field. The TBCR1 contains the higher order of the length. Bit 0 of TBCR 0 is the LSB of the transmit byte count.

Page start register, page stop register (PSTART, PSTOP)

The page start register and the page stop register program indicate the starting address and the ending address of the receive buffer ring. These two registers specify the higher order addresses (the page address) of the buffer ring.

Boundary register (BNRYR)

This register is used to prevent the overflow of the Receive Buffer Ring. The Buffer Manager compares the contents of this register to the buffer address when linking the buffers together. If the contents of this register match the next buffer address, the local DMA operation is aborted.



DMA-related register

Address	Read	Write
20H	MACCFG: MAC configuration register	MACCFG: MAC configuration register
21H	SYSCTR: System control register	SYSCTR: System control register
22H	EEPCMD: EEPROM Command register	EEPCMD: EEPROM command register

Notes: 1. The MACCFG is read-writable and initially downloaded from EEPROM.

2. The SYSCTR is read-writable. The initial value is downloaded from EEPROM.

3. The EEPCMD is a special register directly connected to pin EESK, EEDI, EEDO, and EECS.

MACCFG: MAC Configuration Register			
Bit	**Symbol**	**R/W**	**Function**
0, 1	PHYS1, PHYS0	R/W	Physical layer interface: Used to determine the type of physical interface. Bit1 Bit0 MAU Comment 0 0 TPI 10BaseT compatible squelch 0 1 TPI 10BaseT (Reduced squelch level) 1 X AUI 10Base2 or 10Base5
2	LINK	R/W	Link control: Writing a "1"/"0" to this bit will enable/disable the link integrity test. When this bit is read it will indicate the link status. See Note 1 for this bit's application.
3	POL	R/W	Polarity control: This bit is used to control the auto-detection & correction function or to monitor the TP line polarity. See Note 2 for details.
7	FDX	R/W	Full duplex mode: When this bit is set high the full duplex function is enabled if the TPI interface is selected.

Note1: It is read as "0" if the ECON-PCI is in AUI mode
It is read as "1" if the TP link is good
Enabling this bit will also allow the auto-switching from the TP interface to the AUI interface (10Base2 mode) if the link test failed.

Note2: When this bit is set to **"1"/"0"**, the TP receiver will **enable/disable** the auto-detection and correction function. This bit is read as "1" if the TP line polarity is reversed; otherwise it is read as "0".

System Control Configuration Register			
Bit	**Symbol**	**R/W**	**Function**
0, 1	TEST	R/W	Test mode: These bits are reserved for test. They should remain unchanged during normal operation.
3, 2	PWRDN1, PWRDN0	R/W	Power down mode: Determines the type of software power down mode. Bit3 Bit2 Function 0 0 Normal operation 0 1 Sleep mode; only LED are off 1 0 Analog circuit power down; clock is running 1 1 All is powered down; clock is halted
4	ENCUT	R/W	Enable cut through mode: Setting this bit high will enable the cut through (early interrupt) feature for packet receiving. Refer to the section of Cut Through Receive mode.

EEPROM Programming Register			
Bit	**Symbol**	**R/W**	**Function**
0	EECS	R/W	CS of EEPROM chip: Used to control the logic state of pin 72 when the EEPR bit is set to "1". This bit should be set to "0" when EEPROM is not in use.
1	EESK	R/W	SK of EEPROM chip: Used to control the logic state of pin 43 when the EEPR bit is set to "1".
2	EEDI	R/W	DI of EEPROM chip : Used to control the logic state of pin 42 when the EEPR bit is set to "1"
3	EEDO	R	DO of EEPROM chip: Used to control the logic state of pin 41 when the EEPR bit is set to "1".
4	EEPR	R/W	Enable EEPROM programming: Setting this bit high will program pin 41 to pin 43 to EEPROM access mode. Setting this bit low forces pin 41 to pin 43 to function as memory data bus bit 1 to bit 3.

PCI configuration register

Offset Addr. In Configuration Space	R/W Attribute	Register Name	Power On Default Value	Programmed By
01H- 00H	R/W	Vendor-ID	12C3H	EEPROM
03H-02H	R/W	Device-ID	0058H	N/A
05H-04H	R/W	Command	0000H	S/W
07H-06H	R	Status	0280H	S/W
08H	R	Revision ID	00H	N/A
0BH-09H	R	Class-Code	020000H	None
0CH	R	Cache-Line-Size	00H	None
0DH	R	Latency Timer	00H	None
0EH	R	Header Type	00H	None
0FH	R	BIST	00H	None
13H-10H	R/W	IO Base Address	00000001H	S/W
2DH-2CH	R/W	Subsystem Vendor ID	0000H	EEPROM
2FH-2EH	R/W	Subsystem ID	0000H	EEPROM
33H-30H	R/W	ROM Base Address	00000000H	S/W
3CH	R/W	Interrupt Line	00H	S/W
3DH	R	Interrupt Pin	01H	N/A
3EH	R	Min-Grant	00H	N/A
3FH	R	Max-Latency	00H	N/A

Functional Description

Memory arbiter

The memory arbiter allocates the memory resource for each memory requester. Four possible conditions may invoke memory request , i.e. remote DMA read, remote DMA write, local DMA read and local DMA write. A remote DMA read/write will never occur simultaneously, since these two commands are issues through an I/O command. Both local DMA read and local DMA write may request the memory at the same arbitration cycle, if the full-duplex mode is enabled. The memory arbiter features the max. throughput allowing the full-duplex operation without sacrificing the PCI bus band width.

Remote DMA & Local DMA

Like the NE2000 DMA architecture, the ECON-PCI also provides two DMA channel for data transfer. The local DMA moves data between the local FIFO and the packet buffer memory. The remote DMA handles the data transfer between the host and the packet buffer memory. To move data from the host side to the packet buffer memory , the host should issue a remote DMA write command by programming the Command Register (offset 00H), and then write data to the Data Register (offset 10H). For remote DMA read operation, the host programs the Boundary Pointer (offset 03H), the Remote Start Address Register (offset 08H, 09H) and Remote Byte Count Register (offset 0AH, 0BH), and then issues a remote DMA read command to the Command Register (offset 0H). The data will be sequentially moved to the Data Register until the byte count reaches the programmed value.

During data transmission the local DMA uses a programmed pointer and length registers to transfer a packet from local the buffer memory to the local line buffer. During data reception the data is automatically moved to the buffer memory without the intervention of the host, provided the Page Start Register (offset 01H) and the Page Stop Register (02H) were programmed in advance.

Medium Auto-selection

The ECON-PCI provides a medium auto-switching function for the cable selection. By detecting the link-pulse of the UTP receiver, the ECON-PCI can select either the UTP cable or the coaxial cable. If both cable are used, the ECON-PCI will select the UTP cable as the medium with the higher priority. This feature allows the network to use redundant cable for the security of the cabling system.

Smart squelch

To ensure that the impulse noise on the cable will not be mistaken as valid data, the smart squelch circuit adopts both amplitude and timing measurement to recognize the validity of the incoming signal. The smart squelch circuit monitors the incoming signal for two consecutive peaks of alternating polarity that are received within a 300 Ns window. Once this condition has been satisfied, the squelch circuit level is reduced to minimize the probability of erroneous detection of a Start of idle pulse. If the receiver detects activity on the receiver pair, the incoming data is qualified on three peaks of five alternating polarity to prevent the receiver from detecting a false collision caused by the impulse noise.

Link integrity

When no data is transmitted over the cable, the link pulse is generated by the transmitter at both ends of the twisted-pair cable. The receiver can detect whether the cable is broken or shorted by checking the link pulse. A 100nS pulse is transmitted to the other end of the twisted-pair cable every 16mS during the period of no transmission state. If neither normal data nor the link pulse is detected within 64mS, the ECON-PCI will enter a link-fail state. Once entering a link-fail state, the receiver will not enter a link-OK state until four consecutive link pulses are received.

Auto-loading

Upon power on reset, the ECON-PCI will automatically load the proprietary data from an external serial PROM. All data which is board-dependent is downloaded from the serial PROM after the reset transition from active state to inactive state. The subsystem Vendor ID, the subsystem ID, the Ethernet Physical address are dependent on the board vendor and should be programmed to serial PROM during the manufacturing process. For PnP OS such as Win95, the above information is useful for the OS to automatically load the driver. The ECON-PCI provides this auto-loading feature in order to accommodate PnP environments.

Ethernet address filtering

Providing a variety of Ethernet Physical Address filtering schemes, the ECON-PCI can receive data with promiscuous mode, unicast mode, qualified multicast mode as well as broadcast mode.

Memory map of ECON-PCI

	D15 D0
0000H 001FH	PROM
0020H 3FFFH	Aliased PROM Data
4000H 7FFFH	16K×8 Buffer Memory
8000H FFFFh	Aliased 0000H~7FFH

EEPROM interface and programming

ECON-PCI uses a 93C06 or 93C46 to store configuration data and Ethernet address. The contents of the stored data is shown below:

EEPROM contents

see Table 1.

Direct programming

To program an external EEPROM in-site, the EEPROM interface signals can be directly controlled by writing the proper data to the EEPROM programming register (22H). The value on the MD1, & MD0 pins will then be driven onto the EESK (MD0), and EEDI (MD1) outputs respectively. These outputs will be latched to enable the generation of a clock on EESK by alternatively writing 1 then 0 to the appropriate bit. This can be used to generate the EEPROM signals as described in the HT93C06 or HT93C46 data sheet.

Care should be taken that the read or write operation should follow the procedure described in the EEPROM data sheets.

Since the Vendor ID and Device ID are loaded from the EEPROM during power on reset, the BIOS will ignore the ECON-PCI when EEPROM is empty. It is required to program the EEPROM before using the adapter card. Once the EEPROM has been programmed, the contents of the EEPROM can be changed by direct programming.

Cut through (early interrupt) receive mode

The ECON-PCI, in normal mode, will generate an interrupt to the host after a complete packet is received. This, however, will introduce a throughput latency at least longer than the transmission time of the received packet. To allow the host driver program look ahead at the contents of the receiving packet, the ECON-PCI provides a Cut Through Receive Mode which is enabled by setting the ENCUT bit of the SYSCTR Register.

During the cut through receive mode, several interrupts are generated based on the receiving conditions as depicted in the following paragraph.

- Packet header interrupt
  When an incoming packet matches the address (physical or not) of the network controller and the total received byte count reaches 64, the ECON-PCI will generate an interrupt to notify the host that an addressed packet is on the way. The driver can distinguish this early interrupt by reading ISR and RSR. If the ISR shows an PRX status and RSR doesn't reflect that status on its PRX bit, an early interrupt will be generated.

	D15	D0
00H	Ethernet Address 1	Ethernet Address 0
01H	Ethernet Address 3	Ethernet Address 2
02H	Ethernet Address 5	Ethernet Address 4
03H	SYSCTR	MACCFG
04H	Subsystem Vendor ID High	Subsystem Vendor ID Low
05H	Subsystem ID High	Subsystem ID Low
06H	Vendor ID High	Vendor ID Low

Table 1 EEPROM content

- Packet page interrupt

  Every time the receiver buffer is completely filled and a new buffer is requested, the ECON-PCI will generate an interrupt with PRX of RSR set as Packet header interrupt. This kind of interrupt is issued every 256 byte time (~200μs) until packet reception is complete. The current byte count of packet being received can be accessed from register 01H (RMBC0) and 02H (RMBC1) of page 0.

- Receive status interrupt

  This is the normal interrupt generated after an addressed packet is completely received. If the received packet is a good packet, both the ISR and RSR will set PRX bit high. Otherwise, the RXE or OVW will be reflected on ISR and FAE, XRXE, or MPA on RSR.

Boot ROM operation

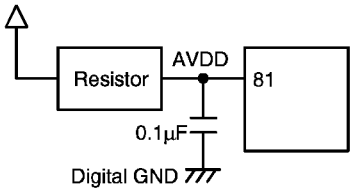
ECON-PCI supports Boot ROM for diskless operation. The memory address space is determined during PCI configuration initialization. The Boot ROM will be detected and executed during the BIOS POST.

ECON-PCI will fetch four consecutive bytes from the Boot ROM, no matter what actual size the PCI bus requires. Retry without data cycles will be issued until four bytes have been stored in the temporary buffer of ECON-PCI. After D-word has been stored, ECON-PCI will drive the data onto the AD bus.

When a 16K or 32K-byte ROM is used as the BOOT ROM, the ROM can be directly inserted into the socket. For a 64K-byte ROM, the actual code size should not be greater than 32K and the code in the upper 32K should be the same as that of the lower 32K. This is because the memory address MA15 is beyond the control of ECON-PCI, which can only drive MA14~MA0.

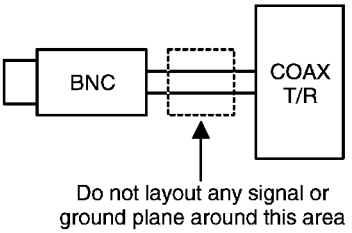
PCB Layout Guide

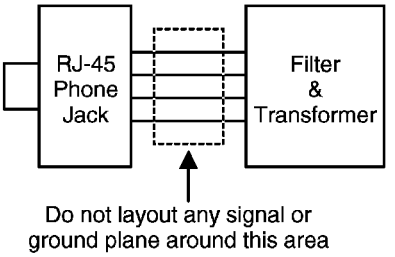
- The de-coupling capacitor between the shielding barrel of the BNC and the chassis ground should be as close to the BNC connector as possible. It is likely to radiate high frequency spectrum, if the capacitor is too far away from the connector.
- It is recommended that the analog power supply (AVDD) should be coupled by either a bead or a 2Ω resistor. This circuit forms a low pass filter, which would prevent the analog circuit from the interference of high frequency noise.



Analog power supply layout

- No signal or ground plane is allowed to be routed next to the following traces: (1) traces between phone jack and the TP transformer; (2) traces between the BNC connector and the coaxial transceiver. The minimum space between these traces and other signal traces is 2mm. This will prevent the high voltage surge from damaging the system. The following figures show the layout guide for both areas.





Package Information

100-pin QFP (100 QFP)