

HD66204

(Dot Matrix Liquid Crystal Graphic Display Column Driver with 80-Channel Outputs)

Description

The HD66204F/HD66204FL/HD66204TF/HD66204TFL, the column driver for a large liquid crystal graphic display, features as many as 80 LCD outputs powered by 80 internal LCD drive circuits. This device latches 4-bit parallel data sent from an LCD controller, and generates LCD drive signals. In standby mode provided by its internal standby function, only one drive circuit operates, lowering power dissipation. The HD66204 has a complete line-up: the HD66204F, a standard device powered by $5\text{ V} \pm 10\%$; the HD66204FL, a 2.7–5.5 V, low power dissipation device suitable for battery-driven portable equipment such as "notebook" personal computers and palm-top personal computers; and the HD66204TF and HD66204TFL, thin package devices powered by $5\text{ V} \pm 10\%$ and 2.7–5.5 V, respectively.

Features

- Duty cycle: 1/64 to 1/240
- High voltage
 - LCD drive: 10–28 V
- High clock speed
 - 8 MHz max under 5-V operation (HD66204F/HD66204TF)
 - 4 MHz max under 3-V operation (HD66204FL/HD66204TFL)
- Display off function
- Internal automatic chip enable signal generator
- Various LCD controller interfaces
 - LCTC series: HD63645, HD64645, HD64646
 - LVIC series: HD66840, HD66841
 - CLINE: HD66850

Ordering Information

Type No.	Voltage Range	Package
HD66204F	$5\text{ V} \pm 10\%$	100-pin plastic QFP (FP-100)
HD66204TF	$5\text{ V} \pm 10\%$	100-pin thin plastic QFP (TFP-100)
HCD66204	$5\text{ V} \pm 10\%$	Chip
HD66204FL	2.7–5.5 V	100-pin plastic QFP (FP-100)
HD66204TFL	2.7–5.5 V	100-pin thin plastic QFP (TFP-100)
HCD66204L	2.7–5.5 V	Chip

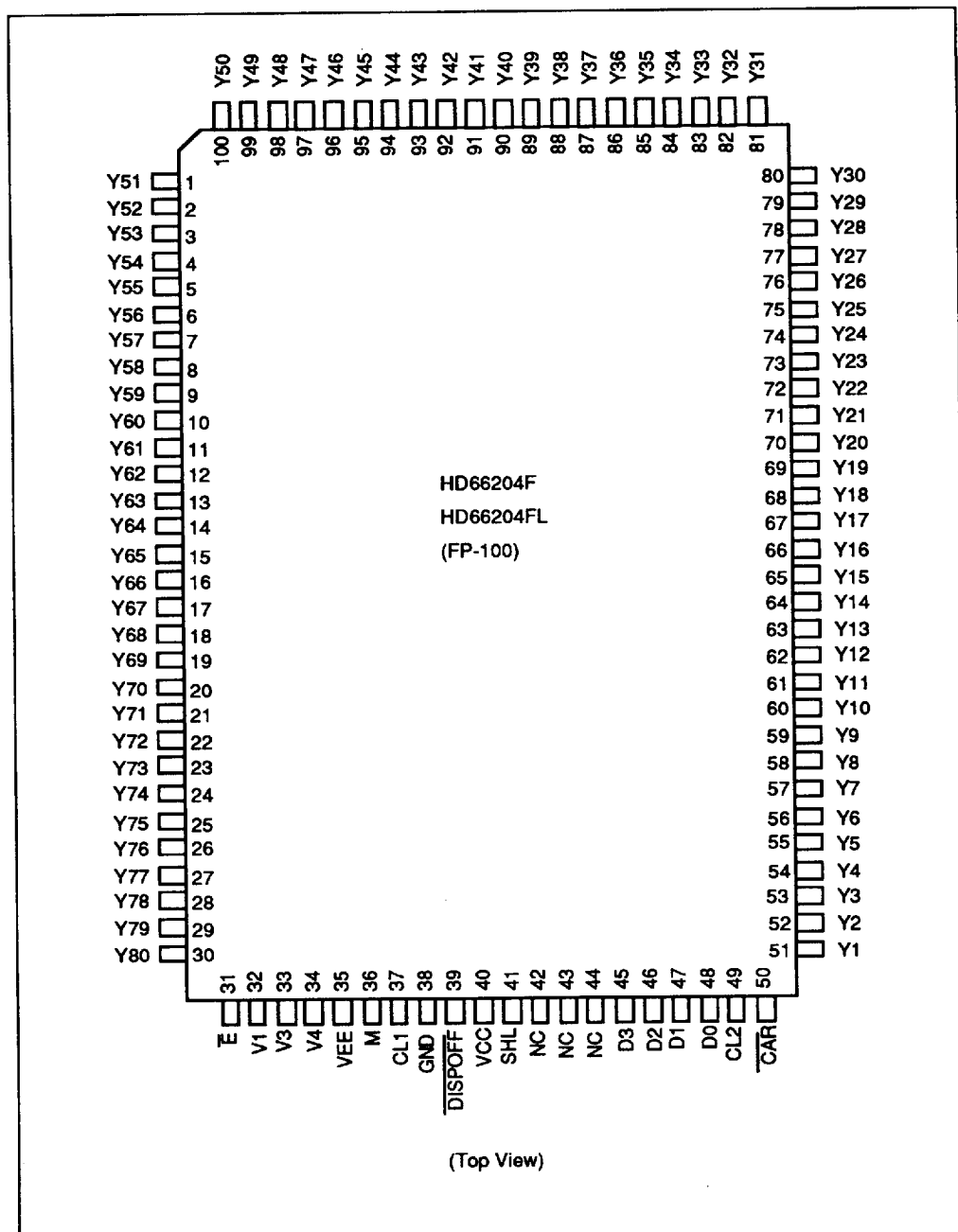
HITACHI

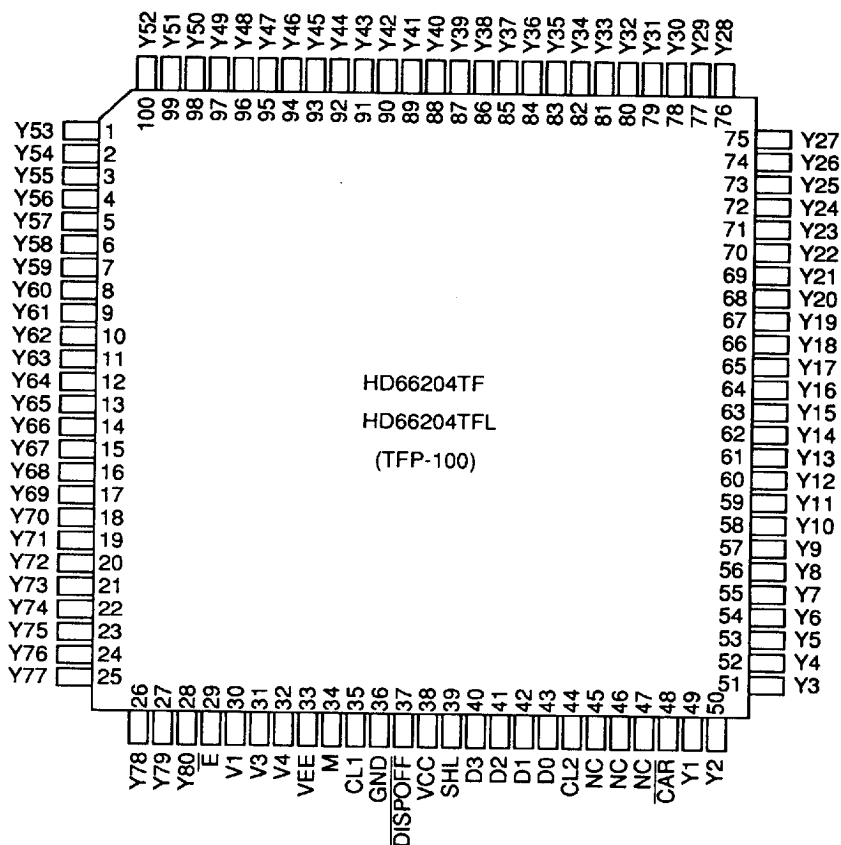
4496204 0046487 866

691

HD66204

Pin Arrangement





HITACHI

4496204 0046489 639

HD66204

Pin Description

Symbol	Pin No. (FP-100/TFP-100)	Pin Name	Input/Output	Classification
V _{CC}	40/38	V _{CC}	—	Power supply
GND	38/36	GND	—	Power supply
V _{EE}	35/33	V _{EE}	—	Power supply
V1	32/30	V1	Input	Power supply
V3	33/31	V3	Input	Power supply
V4	34/32	V4	Input	Power supply
CL1	37/35	Clock 1	Input	Control signal
CL2	49/44	Clock 2	Input	Control signal
M	36/34	M	Input	Control signal
D ₀ –D ₃	48–45/43–40	Data 0–data 3	Input	Control signal
SHL	41/39	Shift left	Input	Control signal
$\overline{E}$	31/29	Enable	Input	Control signal
CAR	50/48	Carry	Output	Control signal
DISPOFF	39/37	Display off	Input	Control signal
Y ₁ –Y ₈₀	51–100, 1–30/49–100, 1–28	Y1–Y80	Output	LCD drive output
NC	42, 43, 44/45, 46, 47	No connection	—	—

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{CC}–V_{EE} supplies power to the LCD drive circuits.

V1, V3, V4: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V3 and V4 are non-selected levels. See figure 1.

Control Signal

CL1: Inputs display data latch pulses for the line data latch circuit. The line data latch circuit latches display data input from the 4-bit latch circuit, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for the 4-bit latch circuit. The 4-bit latch circuit latches display data input via D₀–D₃ at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D₀–D₃: Input display data. High-voltage level of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output. See figure 2.

$\overline{E}$: A low $\overline{E}$ enables the chip, and a high $\overline{E}$ disables the chip.

$\overline{CAR}$: Outputs the $\overline{E}$ signal to the next HD66204 if HD66204s are connected in cascade.

$\overline{DISPOFF}$: A low $\overline{DISP}$ sets LCD drive outputs Y₁–Y₈₀ to V1 level.

LCD Drive Output

Y₁–Y₈₀: Each Y outputs one of the four voltage levels V1, V3, V4, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

NC: Must be open.

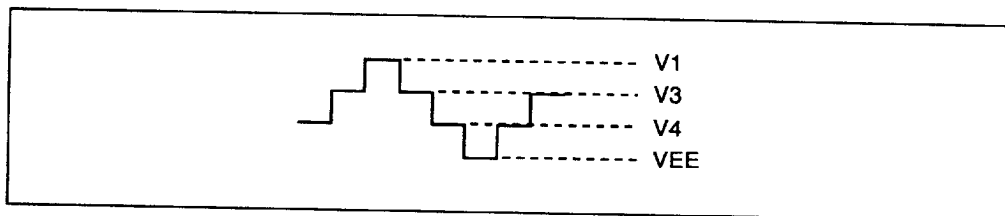


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

HITACHI

4496204 0046491 297

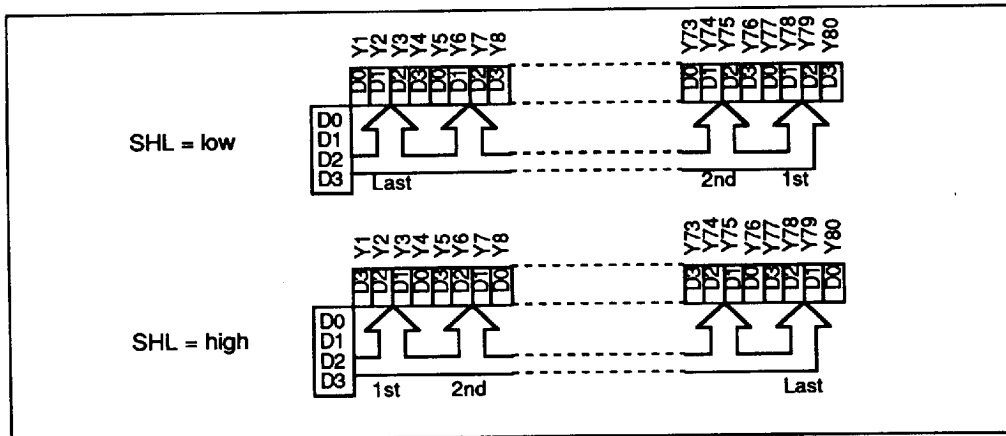


Figure 2 Selection of Destinations of Display Data Output

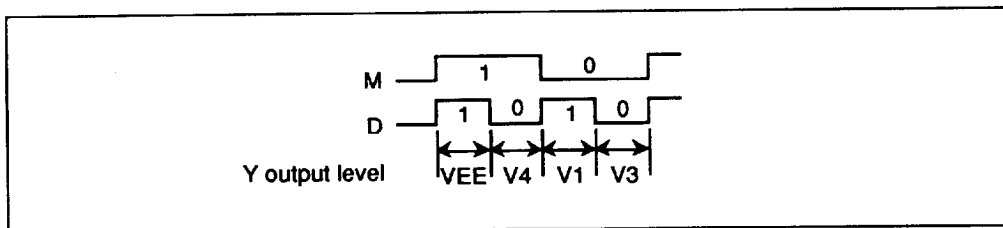


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

Controller: The controller generates the latch signal at the falling edge of each CL2 pulse for the 4-bit latch circuit.

4-Bit Latch Circuit

The 4-bit latch circuit latches 4-bit parallel data input via the D₀ to D₃ pins at the timing generated by the control circuit.

Line Data Latch Circuit

The 80-bit line data latch circuit latches data input from the 4-bit latch circuit, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

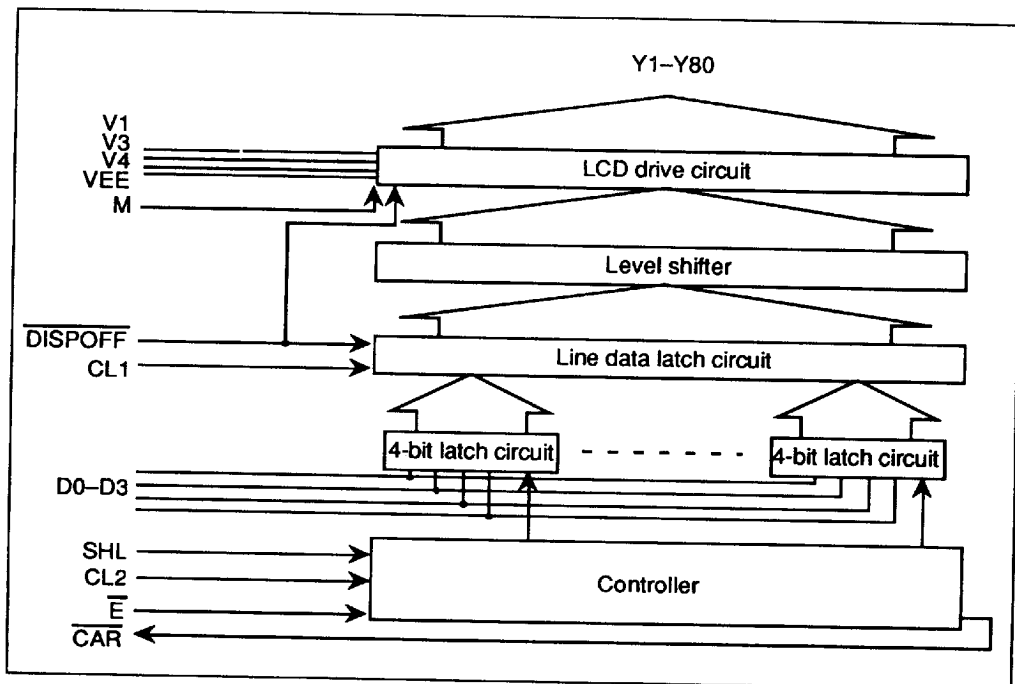
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels V1, V3, V4, and VEE, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the line data latch circuit.

Block Diagram



HITACHI

697

4496204 0046493 06T

HD66204

Comparison of the HD66204 with the HD61104

Item	HD66204	HD61104
Clock speed	8.0 MHz max.	3.5 MHz max.
Display off function	Provided	Not provided
LCD drive voltage range	10–28 V	10–26 V
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V3, V4 (V2 level is the same as VEE level)	V1, V2, V3, V4

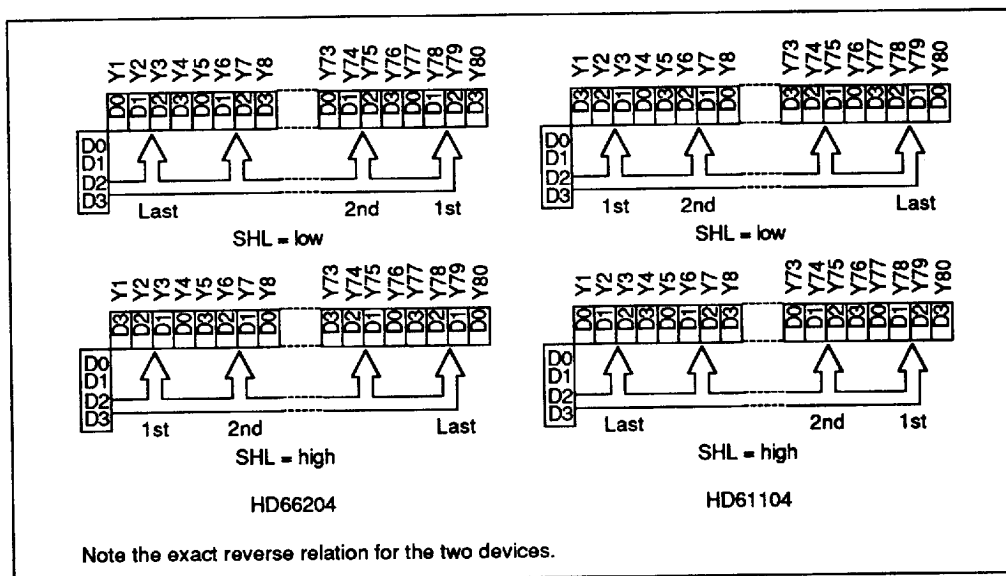


Figure 4 Relation between SHL and LCD Output Destinations for the HD66204 and HD61104

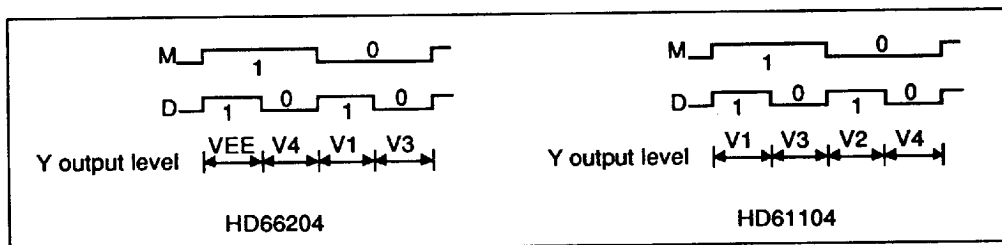
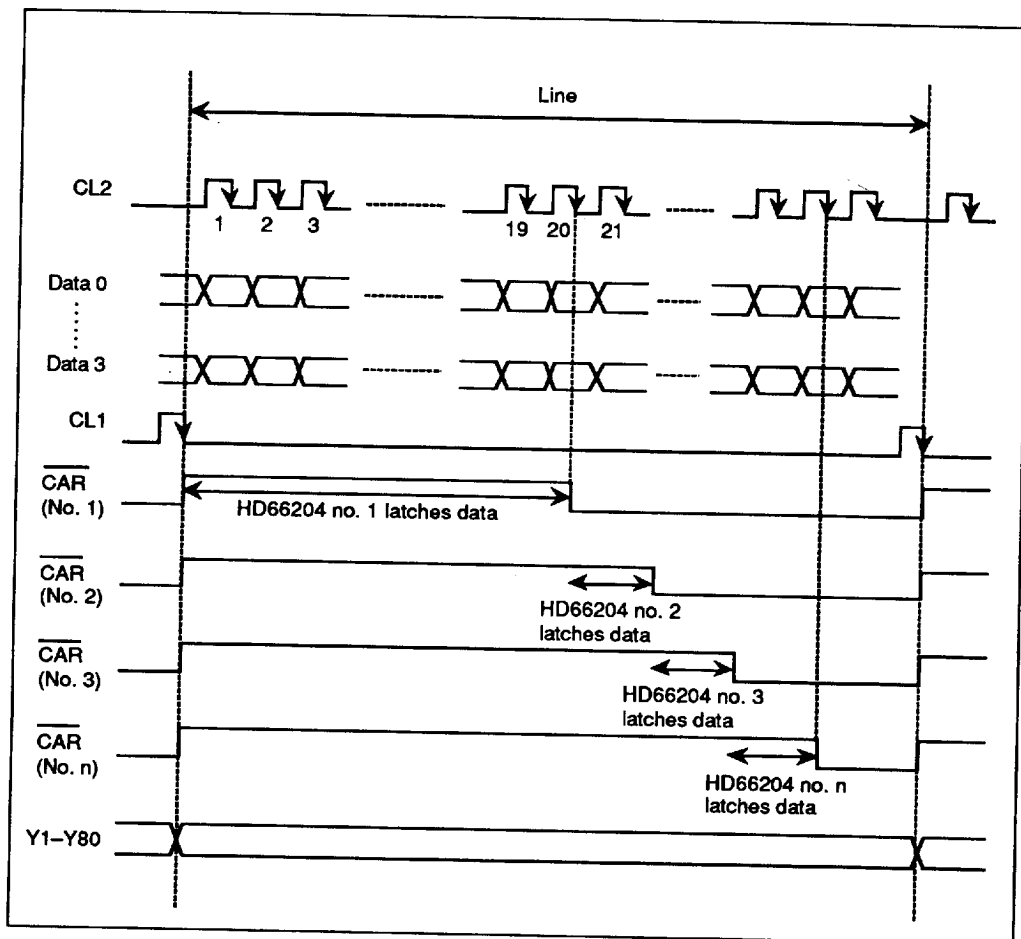


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66204 and HD61104

Operation Timing



HITACHI

699

4496204 0046495 932

Application Example



Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	-0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	$V_{CC} - 30.0$ to $V_{CC} + 0.3$	V	
Input voltage 1	V_{T1}	-0.3 to $V_{CC} + 0.3$	V	1, 2
Input voltage 2	V_{T2}	$V_{EE} - 0.3$ to $V_{CC} + 0.3$	V	1, 3
Operating temperature	T_{opr}	-20 to +75	°C	
Storage temperature	T_{stg}	-55 to +125	°C	

Notes: 1. The reference point is GND (0 V).

2. Applies to pins CL1, CL2, M, SHL, $\bar{E}$, D_0 - D_3 , $\overline{DISPOFF}$.

3. Applies to pins V1, V3, and V4.

4. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66204F/HD66204TF ($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{CC} - V_{EE} = 10$ to 28 V, and $T_a = -20$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.7 \times V_{CC}$	—	V	V		
Input low voltage	V_{IL}	1	0	—	$0.3 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4\text{ mA}$	
Output low voltage	V_{OL}	2	—	—	0.4	V	$I_{OL} = 0.4\text{ mA}$	
V_i - Y_j on resistance	R_{ON}	3	—	—	4.0	k Ω	$I_{ON} = 100\text{ }\mu\text{A}$	1
Input leakage current 1	I_{IL1}	1	-1.0	—	1.0	μA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	-25	—	25	μA	$V_{IN} = V_{CC}$ to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	$f_{CL2} = 8.0\text{ MHz}$ $f_{CL1} = 20\text{ kHz}$ $V_{CC} - V_{EE} = 28\text{ V}$	2
Current consumption 2	I_{EE}	—	—	150	500	μA	Same as above	2
Current consumption 3	I_{ST}	—	—	—	200	μA	Same as above	2, 3

Pins and notes on next page.

HITACHI

701

4496204 0046497 705

HD66204

DC Characteristics for the HD66204FL/HD66204TFL ($V_{CC} = 2.7$ to 5.5 V, $GND = 0$ V, $V_{CC} - V_{EE} = 10$ to 28 V, and $T_a = -20$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.7 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.3 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	V	$I_{OH} = -0.4$ mA	
Output low voltage	V_{OL}	2	—	0.4	V	$I_{OL} = 0.4$ mA	
V_i – Y_j on resistance	R_{ON}	3	—	4.0	k Ω	$I_{ON} = 100$ μ A	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	μ A	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	–25	25	μ A	$V_{IN} = V_{CC}$ to V_{EE}	
Current consumption 1	I_{GND}	—	—	1.0	mA	$f_{CL2} = 4.0$ MHz $f_{CL1} = 16.8$ kHz $f_M = 35$ Hz $V_{CC} = 3.0$ V $V_{CC} - V_{EE} = 28$ V Checker-board pattern	2
Current consumption 2	I_{EE}	—	—	500	μ A	Same as above	2
Current consumption 3	I_{ST}	—	—	50	μ A	Same as above	2, 3

Pins: 1. — CL1, CL2, M, SHL, E, D₀–D₃, DISPOFF

2. $\overline{CAR}$

3. Y_1 – Y_{80} , V1, V3, V4

4. V1, V3, V4

Notes: 1. Indicates the resistance between one pin from Y_1 – Y_{80} and another pin from V1, V3, V4, and V_{EE} , when load current is applied to the Y pin; defined under the following conditions.

$V_{CC} - GND = 28$ V

$V1, V3 = V_{CC} - \{2/10(V_{CC} - V_{EE})\}$

$V4 = V_{EE} + \{2/10(V_{CC} - V_{EE})\}$

V1 and V3 should be near V_{CC} level, and V4 should be near V_{EE} level (figure 6). All voltage must be within ΔV . ΔV is the range within which R_{ON} , the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC} – V_{EE} (figure 7).

2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

3. Applies to standby mode.

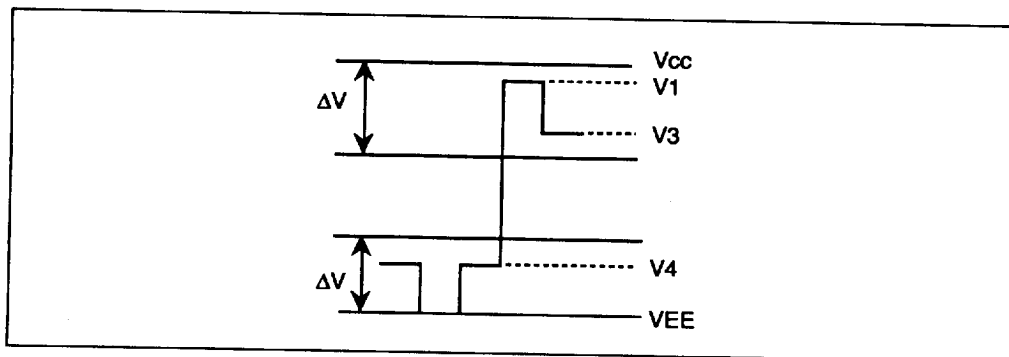


Figure 6 Relation between Driver Output Waveform and Level Voltages

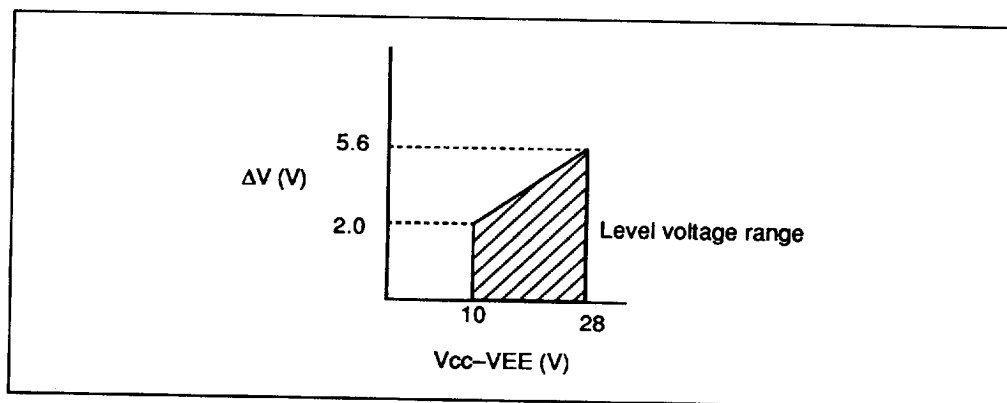


Figure 7 Relation between $V_{CC} - V_{EE}$ and ΔV

HD66204

AC Characteristics for the HD66204F/HD66204TF ($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, and $T_a = -20$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	125	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	45	—	ns	
Clock low-level width	t_{CWL}	CL2	45	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note 1	ns	1
Clock fall time	t_f	CL1, CL2	—	Note 1	ns	1
Data setup time	t_{DS}	D_0 – D_3 , CL2	20	—	ns	
Data hold time	t_{DH}	D_0 – D_3 , CL2	20	—	ns	
Enable ($\bar{E}$) setup time	t_{ESU}	$\bar{E}$, CL2	30	—	ns	
Carry ($\bar{CAR}$) output delay time	t_{CAR}	$\bar{CAR}$, CL2	—	80	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

AC Characteristics for the HD66204FL/HD66204TFL ($V_{CC} = 2.7$ to 5.5 V , $GND = 0\text{ V}$, and $T_a = -20$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	250	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	95	—	ns	
Clock low-level width	t_{CWL}	CL2	95	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note 1	ns	1
Clock fall time	t_f	CL1, CL2	—	Note 1	ns	1
Data setup time	t_{DS}	D_0 – D_3 , CL2	50	—	ns	
Data hold time	t_{DH}	D_0 – D_3 , CL2	50	—	ns	
Enable ($\bar{E}$) setup time	t_{ESU}	$\bar{E}$, CL2	65	—	ns	
Carry ($\bar{CAR}$) output delay time	t_{CAR}	$\bar{CAR}$, CL2	—	155	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

- Notes: 1. $t_r, t_f < (t_{CYC} - t_{CWH} - t_{CWL})/2$ and $t_r, t_f \leq 50\text{ ns}$
 2. The load circuit shown in figure 8 is connected.

The timing diagram illustrates the following parameters and signal behavior:

- CL2:** Shows a single transition with parameters t_r (rise time), t_{CWH} (clock-to-output delay), t_f (fall time), t_{CWL} (clock-to-output delay), and t_{CYC} (cycle time). The signal levels are $0.7V_{CC}$ and $0.3V_{CC}$.
- D0-D3:** Shows data bus activity with parameters t_{DS} (data setup time) and t_{DH} (data hold time). The signal levels are $0.7V_{CC}$ and $0.3V_{CC}$.
- CL1:** Shows a single transition with parameters t_{CWH} (clock-to-output delay) and t_{CL1} (clock-to-output delay). The signal levels are $0.7V_{CC}$ and $0.3V_{CC}$.
- CL2:** Shows multiple transitions with parameters t_{SCL} (setup time), t_{HCL} (hold time), and t_{CAR} (clock-to-output delay). The signal levels are $0.7V_{CC}$ and $0.3V_{CC}$. A "Last data" label is present.
- CAR:** Shows a single transition with parameters t_{CAR} (clock-to-output delay) and t_{ESU} (output setup time). The signal levels are $0.8V_{CC}$ and $0.2V_{CC}$.
- E:** Shows a single transition with parameters t_{CM} (clock-to-output delay) and t_{ESU} (output setup time). The signal levels are $0.7V_{CC}$ and $0.3V_{CC}$.
- M:** Shows a single transition with parameters t_{CM} (clock-to-output delay) and t_{ESU} (output setup time). The signal levels are $0.7V_{CC}$ and $0.3V_{CC}$.

This Material Copyrighted By Its Respective Manufacturer