

Low-Power, Low-Voltage, 24 - Bit $\Delta\Sigma$ ADC

Features

- $\Delta\Sigma$ Analog-to-Digital Converter
 - Linearity Error: 0.0015% FS
 - RMS Noise: 4 μ V
- Two Channel Differential MUX
- Buffered, Fully Differential Analog and Voltage Reference Inputs
- Scalable V_{REF} Input: 0.1 V to Analog Supply
- High Absolute Accuracy via Self-Calibration
- Fixed Digital Filter
 - Single Conversion Settling at 6.7 SPS
 - Simultaneous 50/60 Hz Rejection
- Simple Serial Interface
 - SPI™ and Microwire™ Compatible
 - Schmitt Trigger on Serial Clock (SCLK)
- Low Power
 - Single +3.0 V Supply
 - 330 μ A Supply Current
 - 10 μ A in Sleep Mode

Description

The CS5540 is a low-power and low-voltage $\Delta\Sigma$ analog-to-digital converter (ADC), which achieves highly accurate conversions using a simple non-programmable interface that is easy to understand and design-in. It is optimized to convert analog signals in DC measurement applications, such as temperature and pressure measurement, and various portable devices where low-power consumption is required.

To accommodate these applications, the ADC integrates analog input and reference buffers for increased input impedance and a two-channel multiplexer.

The CS5540 includes a digital filter, which achieves simultaneous rejection of 50/60 Hz signals and provides single conversion settling at 6.7 SPS throughput. Absolute accuracy is achieved via continuous internal self-calibration. The device draws a nominal 330 μ A.

Low-power, low-voltage operation, and a simple serial interface make the CS5540 an ideal device for low-cost, power-conscious DC measurement applications.

ORDERING INFORMATION

CS5540-AS -40 °C - +85 °C 16-Pin SSOP

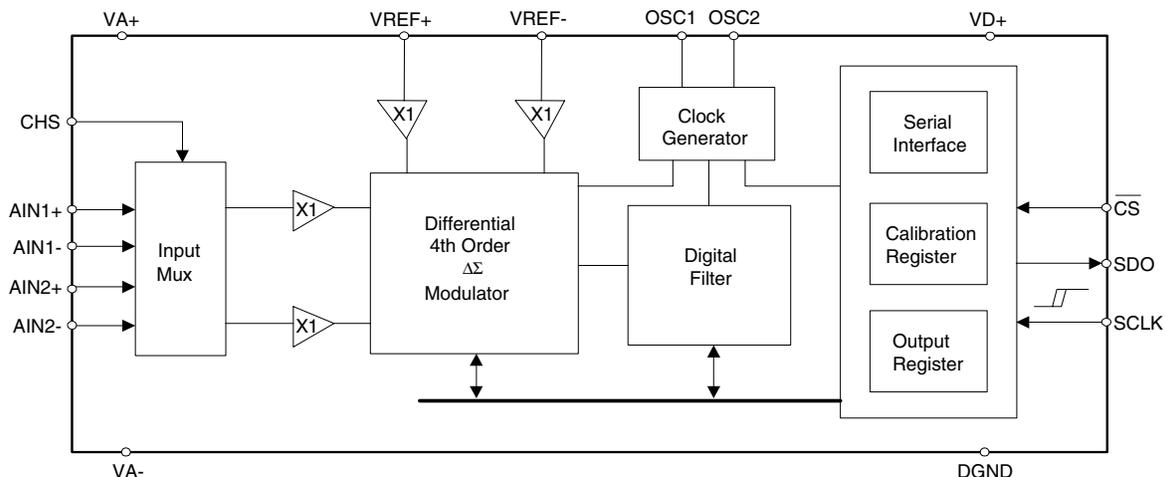


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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$; $V_{A+} = +3.0\text{ V} \pm 5\%$, $V_{A-} = 0\text{ V}$, $V_{D+} = 3.0\text{ V} \pm 5\%$, $DGND = 0\text{ V}$, $V_{REF+} = 2.5\text{ V}$, $V_{REF-} = 0\text{ V}$, $MCLK = 32.768\text{ kHz}$, OWR (Output Word Rate) = 6.7 SPS, Input Range = $\pm 2.5\text{ V}$ Differential, $V_{cm} = 1.25\text{ V}$. (See Note 1.)

Parameter	Min	Typ	Max	Units
Accuracy				
Linearity Error	-	± 0.0015	± 0.003	%FS
No Missing Codes	24	-	-	Bits
Offset Error (Note 2)	-	± 16	TBD	LSB ₂₄
Offset Drift (Notes 2 and 3)	-	20	-	nV/ $^\circ\text{C}$
Full Scale Error	-	± 8	± 31	ppm
Full Scale Drift (Note 3)	-	1	-	ppm/ $^\circ\text{C}$
RMS Noise (Notes 4 and 5)	-	4	-	μV
Bandwidth (-3 dB)	-	11.96	-	Hz

- Notes:
1. Specifications guaranteed by design, characterization, and/or test.
 2. Specification applies to the device only and does not include any effects caused by external parasitic thermocouples.
 3. Drift over specified temperature range after power-up at 25 $^\circ\text{C}$.
 4. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25 $^\circ\text{C}$.
 5. For peak-to-peak noise multiply the RMS value by 6.6.

* Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter		Min	Typ	Max	Units
Analog Input					
Common Mode + Signal on AIN+ or AIN- Single Supply Dual Supplies		0.0	-	VA+	V
		VA-	-	VA+	V
CVF Current on AIN+, AIN-	(Note 6)	-	12	-	nA
Input Leakage for MUX when off		-	10	-	pA
Common Mode Rejection	dc	-	120	-	dB
	50, 60Hz	-	120	-	dB
Input Capacitance		-	8	-	pF
Voltage Reference Input					
Range	(VREF+) - (VREF-) (Note 8)	0.1	2.5	(VA+) - (VA-)	V
CVF Current on VREF+ and VREF-	(Note 7)	-	20	-	nA
Common Mode Rejection	dc	-	120	-	dB
	50, 60 Hz	-	120	-	dB
Input Capacitance		-	12	-	pF
Dynamic Characteristics					
Modulator Sampling Frequency		-	MCLK/2	-	Hz
Filter Settling to 1/2 LSB (Full Scale Step) 6.7 SPS OWR	(Note 9)	-	1/OWR	-	s
Power Supplies					
DC Power Supply Currents (Normal Mode)	IA+	-	225	280	μA
	ID+	-	25	36	μA
Power Consumption	Normal Mode (Note 10)	-	750	1000	μW
	Sleep Mode	-	30	-	μW
Power Supply Rejection	dc Positive Supplies	-	80	-	dB
	dc Negative Supplies	-	80	-	dB

Notes: 6. See Section 2.1, "Analog Input".

7. See Section 2.2, "Voltage Reference Input".

8. Absolute voltages on VREF+ and VREF- must be less than or equal to the supply voltages.

9. The CS5540 includes a digital filter. The filter which achieves simultaneous rejection of 50/60 Hz provides single conversion settling at a 6.7 SPS throughput.

10. All outputs unloaded. All inputs at CMOS levels.

3 V DIGITAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$; $V_{A+} = 3.0\text{ V} \pm 5\%$, $V_{A-} = 0\text{ V}$, $V_{D+} = 3.0\text{ V} \pm 5\%$, $DGND = 0\text{ V}$.) (See Notes 1 and 11.) All voltage levels measured relative to DGND.

Parameter			Symbol	Min	Typ	Max	Units
High-Level Input Voltage:	All Pins Except	OSC1, SCLK	V_{IH}	0.6VD+	-	-	V
		OSC1	V_{IH}	TBD	-	-	V
		SCLK	V_{IH}	(VD+)-0.45	-	-	V
Low-Level Input Voltage:	All Pins Except	OSC1, SCLK	V_{IL}	-	-	0.16VD+	V
		OSC1	V_{IL}	-	-	TBD	V
		SCLK	V_{IL}	-	-	0.6	V
High-Level Output Voltage:	SDO, $I_{out} = -1.0\text{ mA}$		V_{OH}	(VD+)-.25	-	-	V
Low-Level Output Voltage:	SDO, $I_{out} = 1.6\text{mA}$		V_{OL}	-	-	0.4	V
Input Leakage Current			I_{in}	-	± 1	± 10	μA
3-State Leakage Current			I_{OZ}	-	-	± 10	μA
Digital Output Pin Capacitance			C_{out}	-	9	-	pF

Notes: 11. All measurements performed under static conditions.

ABSOLUTE MAXIMUM RATINGS (DGND = 0 V; See Note 12.)

Parameter	Symbol	Min	Typ	Max	Units	
DC Power Supplies (Notes 13 and 14)	Positive Digital	VD+	-0.3	-	+4.0	V
	Positive Analog	VA+	-0.3	-	+4.0	V
	Negative Analog	VA-	-0.3	-	+0.3	V
Input Current, Any Pin Except Supplies (Notes 15 and 16)	I _{IN}	-	-	±10	mA	
Output Current	I _{OUT}	-	-	±25	mA	
Power Dissipation (Note 17)	PDN	-	-	500	mW	
Analog Input Voltage AIN and VREF pins	V _{INA}	(VA-) + (-0.3)	-	(VA+)+0.3	V	
Digital Input Voltage	V _{IND}	-0.3	-	(VD+)+0.3	V	
Ambient Operating Temperature	T _A	-40	-	+85	°C	
Storage Temperature	T _{stg}	-65	-	+150	°C	

Notes: 12. All voltages are measured with respect to the digital ground pin (DGND).

13. VA+ and VA- must satisfy $\{(VA+) - (VA-)\} \leq +4.0$ V.

14. VD+ and VA- must satisfy $\{(VD+) - (VA-)\} \leq +4.0$ V.

15. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.

16. Transient current of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

17. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$; $V_{A+} = +3.0\text{ V} \pm 5\%$ $V_{A-} = 0\text{ V}$, $V_{D+} = 3.0\text{ V} \pm 5\%$, $DGND = 0\text{ V}$; Input Levels: Logic 0 = 0 V, Logic 1 = V_{D+} ; $C_L = 50\text{ pF}$)

Parameter	Symbol	Min	Typ	Max	Units		
Master Clock Frequency:	External Clock	5	-	40	kHz		
	Internal Oscillator (Note 18)	-	32.768	-			
Master Clock Duty Cycle		40	-	60	%		
Rise Times	(Note 19)	t_{rise}	-	-			
	Any Digital Input Except SCLK					1.0	μs
	SCLK					100	μs
SDO Output	50	ns					
Fall Times	(Note 19)	t_{rise}	-	-			
	Any Digital Input Except SCLK					1.0	μs
	SCLK					100	μs
SDO Output	50	ns					
Start-up							
Oscillator Start-up Time	XTAL = 32.768 kHz (Note 20)	t_{ost}	-	500	ms		
Power-on Reset Period		t_{por}	-	490	MCLK cycles		
Serial Port Timing							
Serial Clock Frequency	SCLK	0	-	2	MHz		
Serial Clock	Pulse Width High	t_1	250	-	ns		
	Pulse Width Low	t_2	250	-	ns		
CS Enabled to SCLK Rising		t_3	50	-	ns		
SCLK falling prior to Chip Select Disabled		t_4	100	-	ns		
SDO Read Timing							
CS to Data Valid		t_5	-	-	150 ns		
SCLK Falling to New Data Bit		t_6	-	-	150 ns		
CS Rising to SDO Hi-Z		t_7	-	-	150 ns		

Notes: 18. Device parameters are specified with 32.768 kHz clock; however, clocks up to 40 kHz can be used for increased throughput.

19. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

20. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

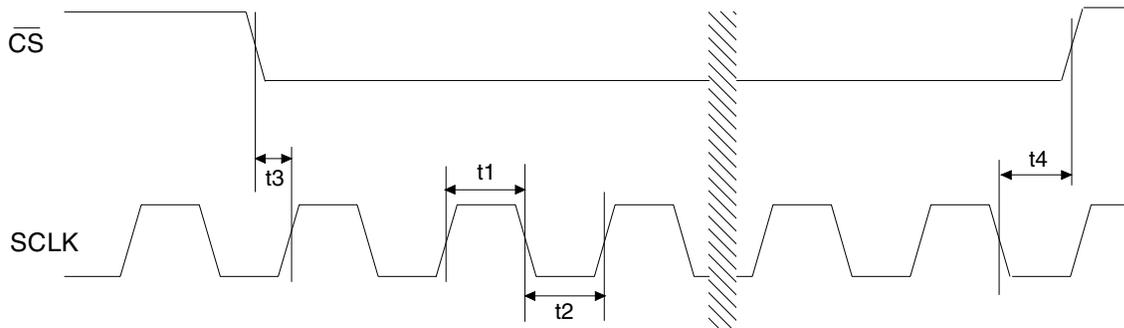


Figure 1. Continuous Running SCLK Timing (Not to Scale)

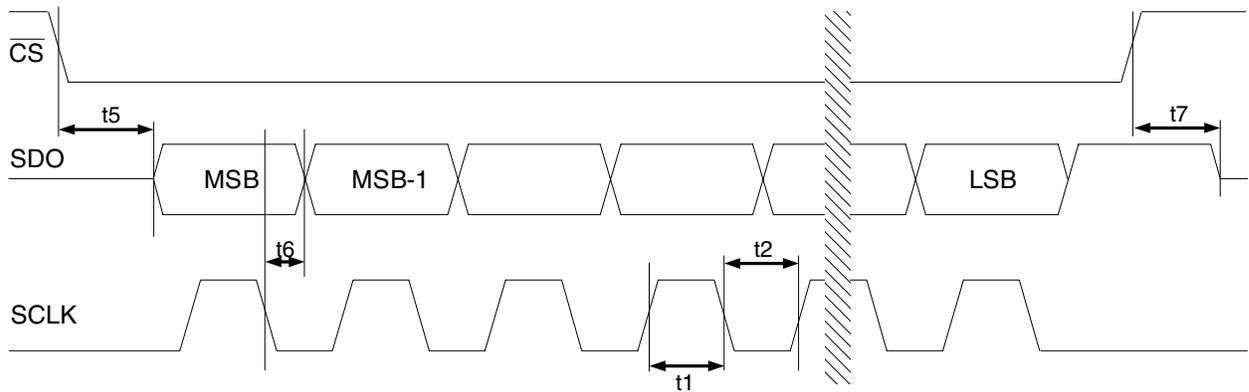


Figure 2. SDO Read Timing (Not to Scale)

2. GENERAL DESCRIPTION

The CS5540 is a low-power and low-voltage 24-bit $\Delta-\Sigma$ analog-to-digital converter (ADC). It is optimized to convert analog signals in DC measurement applications such as temperature and pressure measurement, and various portable devices where low power consumption is required.

To accommodate these applications, the ADC integrates analog input and reference buffers for increased input impedance and includes a two-channel multiplexer. Absolute accuracy is accomplished via self-calibration. The device also operates with a variety of supply configurations while drawing a nominal 330 μA .

The CS5540 includes a digital filter which achieves simultaneous rejection of 50/60 Hz and provides single conversion settling at a 6.7 SPS throughput. The filter’s output word rate can be increased by approximately 1.22X by using a 40 kHz master clock, although the 50/60 Hz rejection will be sacrificed.

To ease communications between the ADC and a microcontroller, the converter includes a simple three-wire serial interface which is SPI and Microwire compatible. A Schmitt Trigger input is provided on the serial clock (SCLK) input.

2.1 Analog Input

Figure 3 illustrates a block diagram of the CS5540. The device consists of a multiplexer, a unity gain coarse/fine charge input buffer, a fourth order $\Delta-\Sigma$ modulator, and a digital filter.

2.1.1 Analog Input Model

Figure 4 illustrates the input models for the AIN pins. The model includes a coarse/fine charge buffer which reduces the dynamic current demands from the analog input signal. The buffer is designed to accommodate rail to rail (common-mode plus signal) input voltages. Typical CVF (sampling) current is about 8 nA (MCLK = 32.768 kHz). Application Note 30, “Switched-Capacitor A/D Input Structures”, details various input architectures.

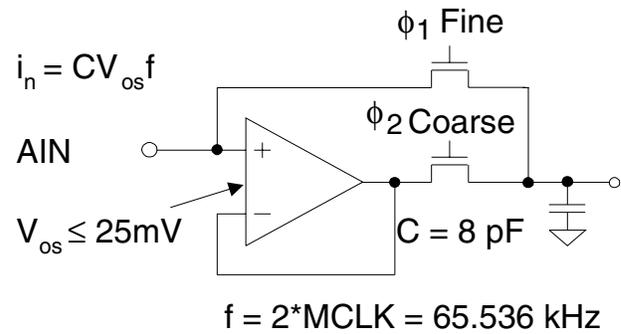


Figure 4. Input model for AIN+ and AIN- pins

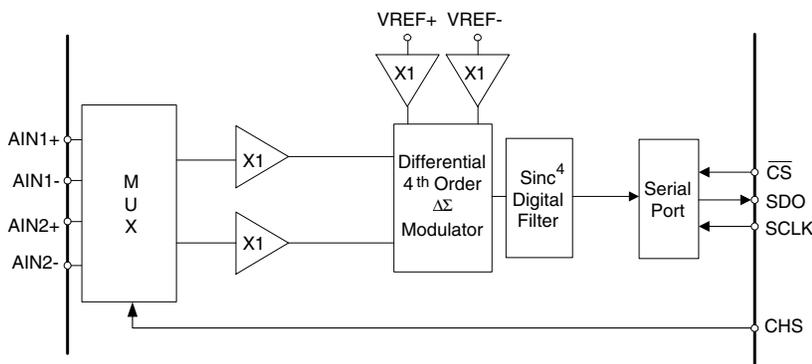


Figure 3. Multiplexer Configuration

2.2 Voltage Reference Input

The differential voltage between VREF+ and VREF- sets the nominal full scale input span of the converter. For a single-ended reference voltage, the reference output is connected to the VREF+ pin of the CS5540 and the ground reference is connected to the VREF- pin. Note that the differential reference voltage can be from 0.1 V to ((VA+)- (VA-)). The noise-free resolution of a single sample from the ADC is directly proportional to the voltage reference as depicted in Figure 5.

Note: When a lower reference voltage is used, the resulting code widths are smaller. Since the output codes exhibit more changing codes for a fixed amount of noise, the converter appears noisier.

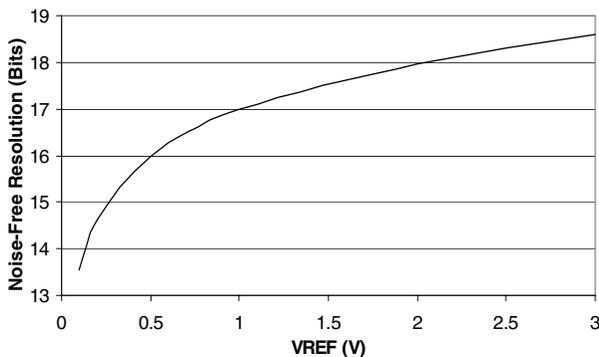


Figure 5. Typical Noise-Free Resolution vs. Voltage Reference

Noise-Free Res. = \log_2 (Bipolar Span/6.6*RMS Noise)

2.2.1 Voltage Reference Input Model

Figure 6 illustrates the input models for the VREF pins. It includes a coarse/fine charge buffer which reduces the dynamic current demand of the external reference. The reference's buffer is designed to accommodate rail-to-rail (common-mode plus signal) input voltages. Typical CVF (sampling) current is about 16 nA (MCLK = 32.768 kHz).

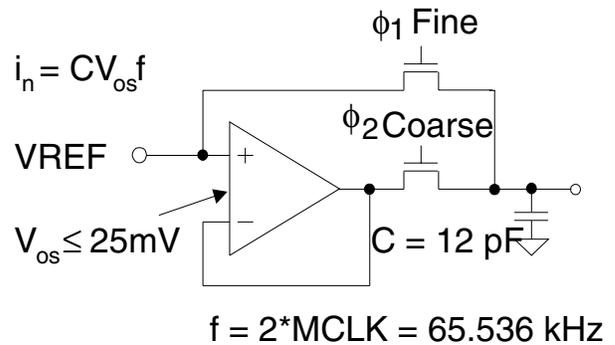


Figure 6. Input model for VREF+ and VREF- pins

2.3 Power Supply Arrangements

The CS5540 is designed to operate with a total supply voltage of $3.0\text{ V} \pm 5\%$. For maximum flexibility, separate pins are provided for VA+, VA-, VD+, and DGND, which is especially useful with ground-referenced input signals.

Figure 7 illustrates the CS5540 connected with a single +3.0 V supply for both the analog and digital sections.

2.4 Clock Generator

The CS5540 includes an oscillator circuit which can be connected with an external crystal to provide the master clock for the chip. The chip is designed to operate using a low-cost 32.768 kHz “tuning fork” type crystal. One lead of the crystal should be connected to OSC1 and the other to OSC2. A 10 megohm resistor is required in parallel with the crystal. Lead lengths should be minimized to reduce stray capacitance. Note that the converter will operate with an external (CMOS compatible) clock with frequencies up to 40kHz, applied to the OSC1 pin.

2.5 Serial Port Interface

The CS5540’s serial interface consists of three control lines: $\overline{\text{CS}}$, SDO, and SCLK.

$\overline{\text{CS}}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{\text{CS}}$ pin is tied to logic 0, the port can function as a three wire interface.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{\text{CS}}$ is at logic 1.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC’s serial port. The $\overline{\text{CS}}$ pin must be held at logic 0 before SCLK transitions can be recognized by the port logic. To accommodate opto-isolators, SCLK is designed with a Schmitt-trigger input.

2.6 Input Channel Selector

CHS, the Channel Select input, permits the user to select between AIN1 and AIN2 for data conversions. When CHS = 0, AIN1 is converted. When CHS = 1, AIN2 is converted. Note that since the converter continuously converts the input selected

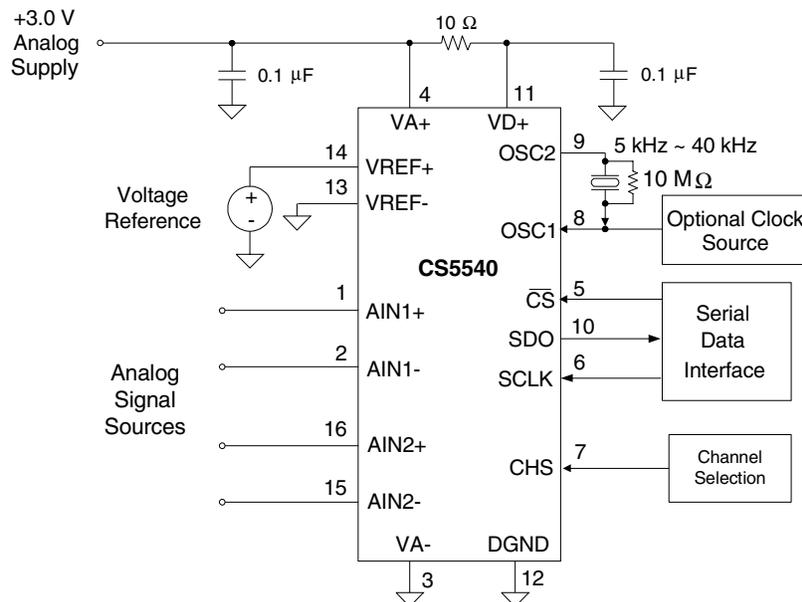


Figure 7. CS5540 Configured with a single +3.0 V Supply

by CHS, the channel being converted can be switched at any time. The conversion in-process when CHS is switched will be aborted and a new conversion will begin on the selected channel. The indicator bits in the SDO output will indicate which channel was converted.

2.6.1 Switching Channels

7358 clock cycles after CHS is toggled, SDO will fall (indicating new data present). All subsequent data will be presented to the serial port every 4884 clock cycles, as portrayed in Figure 8.

2.7 Serial Port and Data Conversions

When power is applied to the CS5540, it is reset by the power-on reset circuit. Then the converter enters the data mode where the ADC continuously converts the analog input channel selected by the channel select pin (CHS). After a conversion is complete, the SDO pin falls to logic 0 to indicate an end of conversion and the next 32 serial clock pulses shift data out of the serial port. Figure 8 illustrates the sequence necessary to read output data from the data conversion register.

The CS5540 operates in a self-calibration mode which allows the converter to calibrate continuously between each conversion (if a user requires system calibration, this can be accommodated in the system microcontroller). The sections that follow detail the conversion mode and also explain how to

decode the conversion word into the respective flag and data bits.

Note: The CS5540 offers self calibration, in which the ADC calibrates out offset and gain errors due to the ADC itself. Calibration in the CS5540 is used to set the zero and gain slope of the ADC's transfer function. For the self-calibration of offset, the converter internally ties the inputs of the modulator together and routes them to the VREF- pin as shown in Figure 9. VREF- must be tied to a fixed voltage between VA+ and VA-. For self-calibration of gain, the differential inputs of the modulator are connected to VREF+ and VREF- as shown in Figure10. Further note that each calibration step (offset or gain) is transparent to the user and is included in the specified 6.7 SPS output rate.

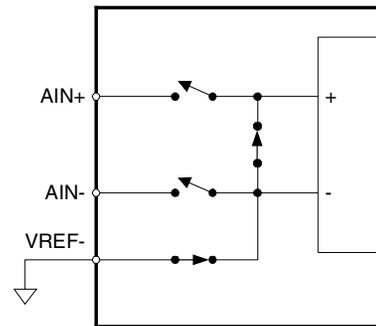


Figure 9. Self Calibration of Offset

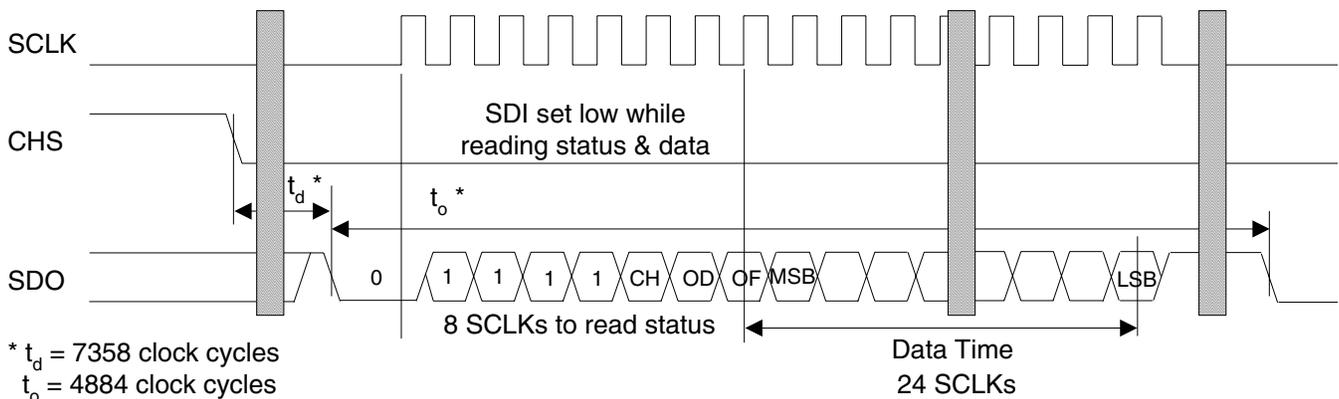


Figure 8. Command and Data Word Timing

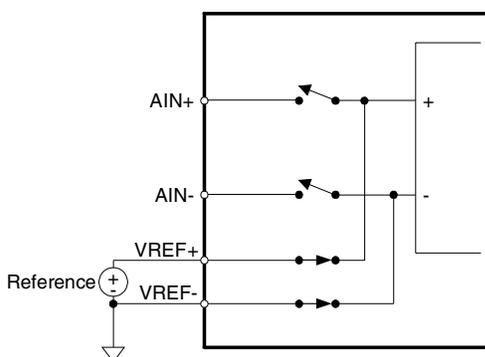


Figure 10. Self Calibration of Gain

2.7.1 Reading Conversions

At the completion of a conversion, SDO will fall to logic 0 to indicate that the conversion is complete. Calibration will be transparent to the user. Nevertheless, to read a conversion word, the user must issue 32 SCLK's. The first 8 SCLKs clear the SDO flag and read the status flags. Upon the falling edge of the 8th SCLK, the SDO pin will present the first bit (MSB) of the conversion word. 24 SCLKs (high, then low) are then required to read the conversion word from the port. Upon the falling edge of the 32nd SCLK, SDO will return high, waiting till the next conversion is complete before it falls again.

The user is not required to read every conversion. If the user chooses not to read a conversion after SDO falls, SDO will rise one MCLK clock cycle before the next conversion is completed and then fall to signal that another conversion word is available (assuming \overline{CS} is kept low).

- Note:
- 1) If the user begins to clear the SDO flag and read the conversion data, this action must be finished before the conversion cycle which is occurring in the background is complete if the user wants to be able to read the new conversion data.
 - 2) If the multiplexer CHS input of the converter is switched while it is performing a conversion, the filter will abort the current conversion and start a new conversion on the new channel.

- 3) If the channel is switched when SDO is low, SDO will remain low, and the previous conversion result will remain in the serial port. SDO will rise one MCLK cycle before the new channel's data is ready, then fall to indicate that the conversion data is available.

2.7.2 Output Coding

The CS5540 outputs a 24-bit two's-complement data conversion word. To read a conversion word the user must read the conversion data register, which is 24 bits long and outputs the conversions MSB first. Once a conversion is complete, SDO falls and 32 SCLK's are required to read a conversion. The first 8 SCLKs are used to clear an internal SDO flag and clock out status flags.

The CH (CHannel indicator) bit keeps track of which input channel was converted (0=AIN1; 1=AIN2).

The OD (Oscillation Detect) bit is set to a logic 1 any time that an oscillatory condition is detected in the modulator. This does not occur under normal operating conditions, but may occur whenever the input to the converter is extremely overranged. If the OD bit is set, the conversion data bits can be completely erroneous. The OD flag bit will be cleared to logic 0 when the modulator becomes stable.

The OF (Overrange Flag) bit is set to a logic 1 any time the input signal is: 1) more positive than positive full scale, or 2) more negative than negative full scale. It is cleared back to logic 0 whenever a conversion word occurs which is not overranged.

The last 24 SCLKs are used to clock the actual data out of the conversion data register.

Table 1 and Table 2 illustrate the output coding for the CS5540. Conversion data is output in two's complement format.

2.7.3 Digital Filter

The CS5540 filter achieves simultaneous rejection of 50/60 Hz and provides single conversion settling at a 6.7 SPS throughput, including auto-calibration.

The filter is optimized to yield better than 80 dB rejection between 47 Hz to 63 Hz (i.e. 80 dB minimum rejection for both 50 Hz and 60 Hz) when the master clock is 32.768 kHz. The filter's output word rate can be increased by approximately 1.22X by using a 40 kHz master clock, although the 50/60 Hz rejection will be sacrificed. The filter has a response as shown in Figure 11.

Note: The converter's digital filter linearly scales with MCLK.

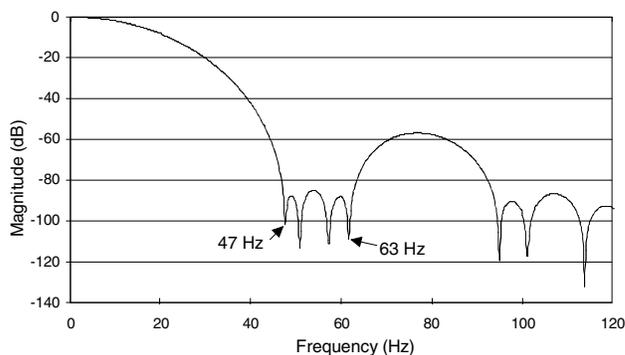


Figure 11. Filter Response (MCLK = 32.768 kHz)

				D31	D30	D29	D28	D27	D26	D25	D24
				0	1	1	1	1	CH	OD	OF
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
MSB	22	21	20	19	18	17	16	15	14	13	12
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
11	10	9	8	7	6	5	4	3	2	1	LSB

Table 1. Output Conversion Data Register Description (24 bits + flags)

Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	7FFFFFFF
VFS-1.5 LSB	7FFFFFFF ----- 7FFFFFFE
-0.5 LSB	000000 ----- FFFFFFF
-VFS+0.5 LSB	800001 ----- 800000
<(-VFS+0.5 LSB)	800000

Table 2. CS5540 24-Bit Bipolar Output Coding

Note: Plus or minus VFS is defined as a differential input signal equal in magnitude to the voltage between the VREF+ and VREF- pins. See the text about error flags for overrange and underrange conditions.

2.8 Sleep Mode

The CS5540 features two power consumption modes: normal and sleep. The normal mode, the default mode, is entered after a power-on-reset. In normal mode, the CS5540 performs conversions and typically consumes 750 μ W.

To enter sleep, transmit 8 SCLK's (low-high transitions) after SDO falls, indicating that a conversion is complete (32 SCLK's would be needed to read the conversion). One conversion cycle later, when SDO falls again, the part enters sleep, reducing the consumed power to around 30 μ W. During sleep, most of the analog portion of the chip is powered down and filter convolutions are halted. While the part is in the sleep mode, the SDO pin will remain in a logic high state, as long as the Chip Select is enabled.

To exit the sleep mode, transmit 8 more SCLK's. Since the sleep mode disables the oscillator, approximately a 500 ms crystal oscillator start-up delay period is required before the ADC returns to the normal mode. If an external clock is used, the ADC will return to normal power mode within 3 milliseconds. In either case, the SDO pin will go low to indicate when new data is available and can be read.

2.9 Power-Up and Initialization

Care must be exercised to insure that no pins are ever taken below the negative analog supply (VA-) potential. The analog and digital supplies should be applied simultaneously to assure that the power-on reset circuit will automatically reset the ADC when both supplies are at acceptable levels.

Conversions will begin once a stable clock is available to the ADC. If a 32.768 kHz crystal is being used, it will take approximately 500 ms for the oscillator to stabilize and to begin conversions after power has been applied to the converter. If a CMOS compatible clock source with no start-up

delay is being used to drive the ADC, then conversions will begin immediately.

Note: The CS5540 includes an on-chip power on reset circuit to automatically reset the ADC shortly after power-up. When power to the CS5540 is applied, the ADC is held in a reset condition until the master clock has started and a counter-timer elapses (i.e. the counter-timer counts 490 clock cycles to make sure the oscillator is fully stable).

After a valid reset, the ADC is initialized into the data state where it begins to continuously calibrate the ADC and convert the analog input. Once a valid conversion is complete, monitor the SDO pin for a falling edge to indicate that the data is ready to be read.

2.10 PCB Layout

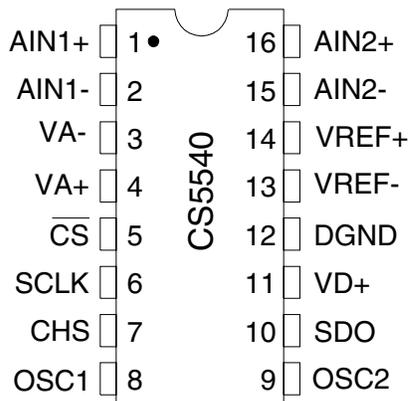
The CS5540 should be placed entirely over an analog ground plane with the DGND pin of the device connected to the analog ground plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip

See the CDB5540/41 data sheet for suggested layout details and refer to *Applications Note 18* for more detailed layout guidelines.

Applications engineering provides a Free and Confidential Schematic Review Service.



3. PIN DESCRIPTIONS



Clock Generator

OSC1; OSC2 - Master Clock.

An inverting amplifier inside the chip is connected between these pins and can be used with a crystal or resonator to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock (powered relative to VD+) can be supplied into the OSC1 pin to provide the master clock for the device and the OSC2 pin can be left unconnected.

Control Pins and Serial Data I/O

$\overline{\text{CS}}$ - Chip Select.

When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{\text{CS}}$ should only be changed when SCLK = 0.

SDO - Serial Data Output.

SDO is the serial data output. It will output a high impedance state if $\overline{\text{CS}} = 1$.

SCLK - Serial Clock Input.

A clock signal on this pin determines the output rate of the data for the SDO pins respectively. This input is a Schmitt trigger to allow for slow rise-time signals. The SCLK pin will recognize clocks only when $\overline{\text{CS}}$ is low.

CHS - Channel Select Input.

CHS permits the user to select between AIN1 and AIN2 for data conversions. When CHS = 0, AIN1 is converted. When CHS = 1, AIN2 is converted. Note that since the converter continuously converts the input selected by CHS, the channel being converted can be switched at any time. The current conversion will be aborted and a new one started on the newly selected channel. The serial data status flags will indicate which channel was converted.

Measurement and Reference Inputs

AIN1+, AIN1-, AIN2+, AIN2- - **Differential Analog Inputs.**

Differential input pins into the device.

VREF+, VREF- - **Voltage Reference Inputs.**

Fully differential inputs which establish the voltage reference for the on-chip modulator.

Power Supply Connections

VA+ - Positive Analog Power.

Positive analog supply voltage.

VA- - Negative Analog Power.

Negative analog supply voltage.

VD+ - Positive Digital Power.

Positive digital supply voltage.

DGND - Digital Ground.

Ground return for the digital supply.

4. SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two end points of the A/D Converter transfer function. One end point is located 1/2 LSB below the first code transition and the other end point is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity

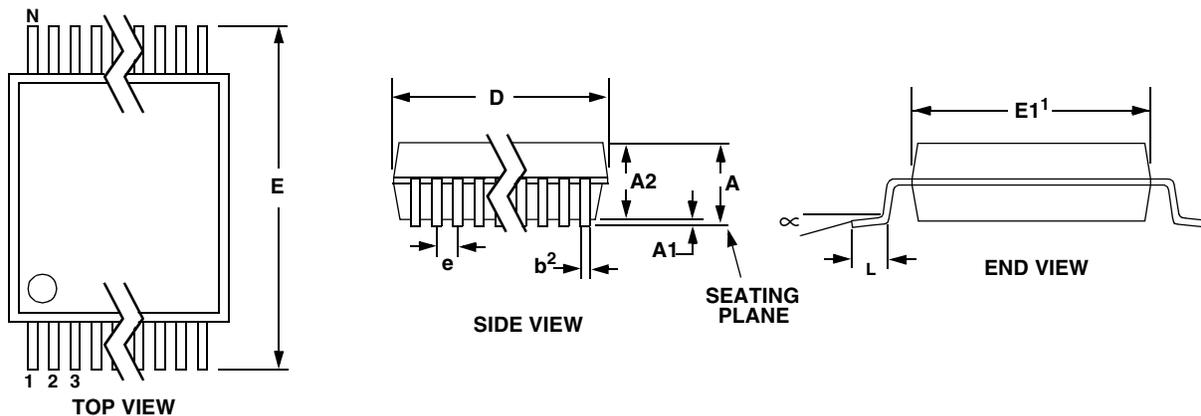
The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition from the ideal $[(V_{REF+}) - (V_{REF-})] - 3/2 \text{ LSB}$. Units are in LSBs.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below zero volts differential between the AIN+ and AIN- pins). Units are in LSBs.

5. PACKAGE DIMENSIONS
16L SSOP PACKAGE DRAWING


DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.005	0.010	0.05	0.13	0.25	
A2	0.064	0.069	0.074	1.68	1.75	1.88	
b	0.009	0.012	0.015	0.22	--	0.38	2,3
D	0.232	0.244	0.256	5.90	6.20	6.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0295	0.041	0.63	0.75	1.03	
∞	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

- Notes:
1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
 2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
 3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

• **Notes** •

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