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# HN27C4000FP Series

524288-Word  $\times$  8-Bit/262144-Word  $\times$  16-Bit CMOS One Time  
Programmable ROM

# HITACHI

ADE-203-310B (Z)

Rev. 2.0

Jun. 22, 1995

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## Description

The Hitachi HN27C4000FP is a 4-Mbit one time programmable ROM that is organized either as 524288-word  $\times$  8-bit or as 262144-word  $\times$  16-bit, featuring extra-high speed burst mode that gives two times faster 4-word or 8-byte serial access than normal. And also high speed and fast programming are served as well as the existing Hitachi 4M device HN27C4096 and HN27C4001. Fabricated on advanced fine process and high speed circuitry technique, HN27C4000 makes high speed access time and low power dissipation in either active or stand-by mode. Therefore, it is suitable for all systems featuring high speed microprocessor such as the 80386, 80486, 68030, 68040 and so on.

## Features

- Organization: 524288-word  $\times$  8-bit/262144-word  $\times$  16-bit ( $\overline{\text{BYTE}}/\text{V}_{\text{pp}}$  enables selection byte-wide or word-wide)
- High speed:
  - Access time 120 ns/150 ns (max)
  - Burst access time 60 ns/60 ns (max)
- Low power dissipation:
  - Standby mode; 5  $\mu\text{W}$  (typ)
  - Active mode; 150 mW/MHz (typ)
- Fast high reliability page programming, fast high-reliability programming and option programming:
  - Program voltage; +12.5 V DC
  - Program time; 3.5 sec (min) (Theoretical in Page programming)
- Inputs and outputs TTL compatible during both read and program modes
- Pin arrangement: 40-pin EIAJ standard pin compatible with HN62414FA/ HN62434FA
- Device identifier mode: Manufacturer code and device code

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# HN27C4000FP Series

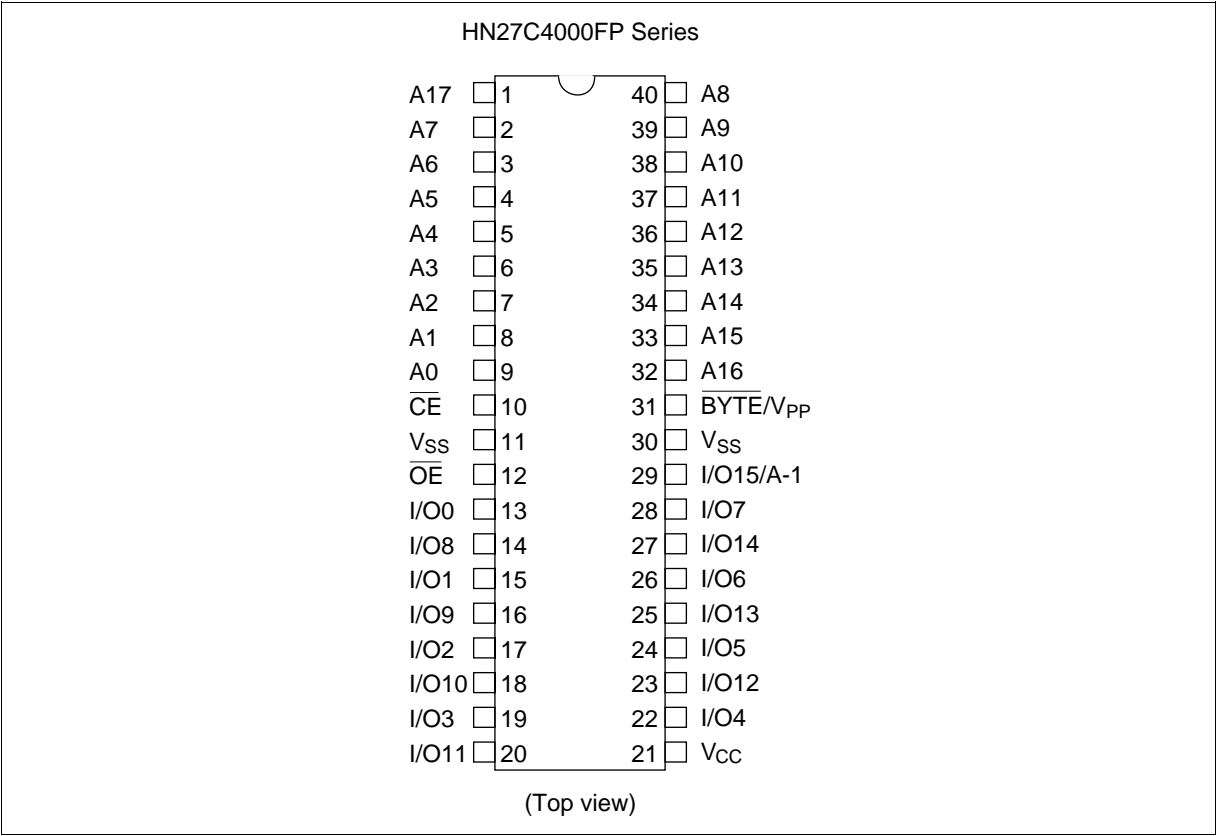
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## Ordering Information

Type No.	Access Time	Package
HN27C4000FP-12	120 ns	525-mil 40-pin plastic SOP (FP-40D)
HN27C4000FP-15	150 ns	

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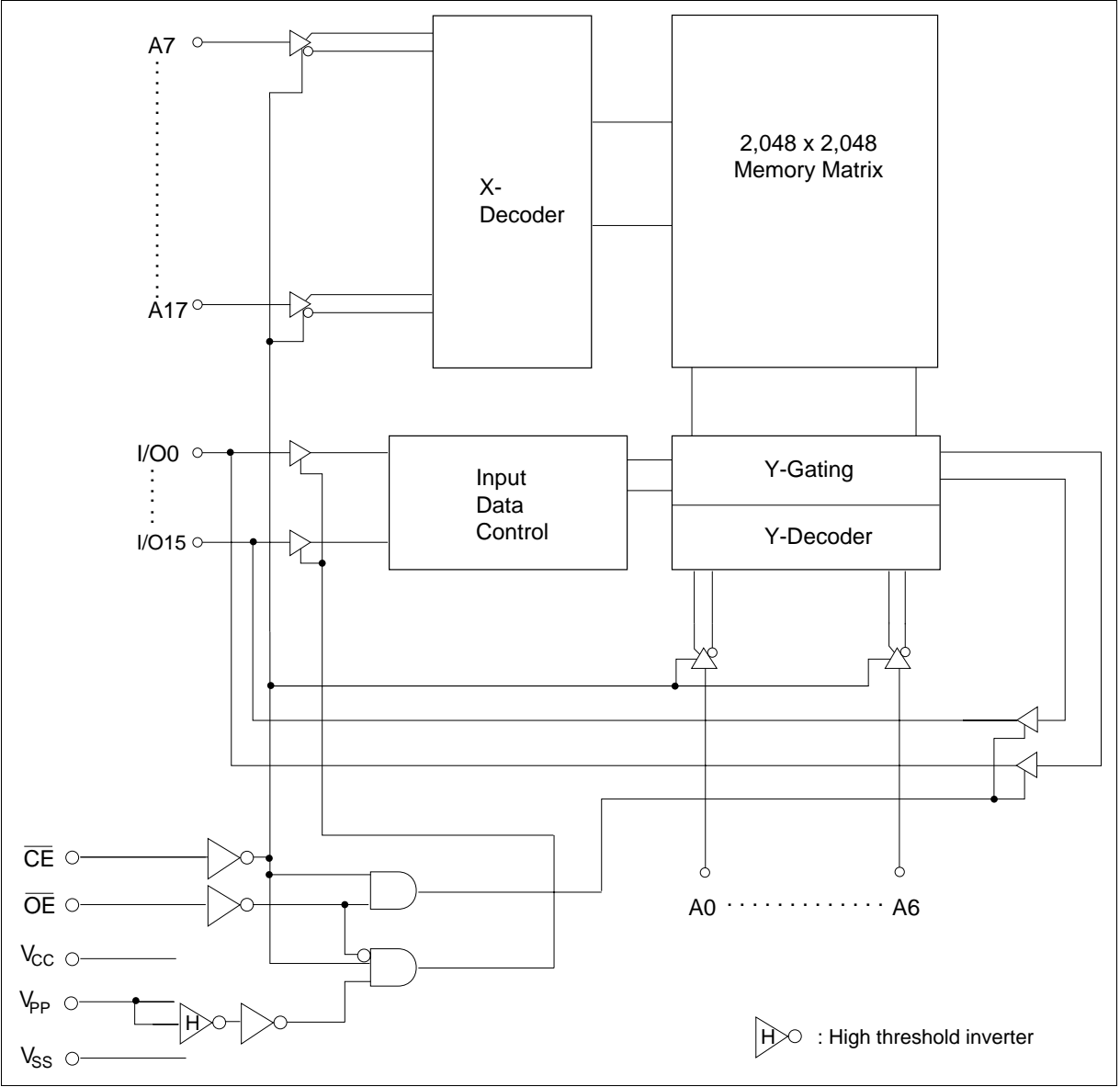
Pin Arrangement



Pin Description

Pin Name	Function
A0 – A17	Address
I/O0 – I/O14	Input/output
I/O15/A-1	Input/output/address
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
$\text{V}_{\text{CC}}$	Power supply
$\overline{\text{BYTE}}/\text{V}_{\text{PP}}$	Byte/word selection/ Programming power supply
$\text{V}_{\text{SS}}$	Ground

Block Diagram



## Mode Selection

Mode	Pin FP-40D	$\overline{\text{CE}}$ (10)	$\overline{\text{OE}}$ (12)	A9 (39)	$\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ (31)	$\text{V}_{\text{CC}}$ (21)	I/O0 – I/O7, (13 – 20,	I/O8 – I/O14, 22 – 28,	I/O15/ A-1 29)
Read (X16 bit)		$\text{V}_{\text{IL}}$	$\text{V}_{\text{IL}}$	X	$\text{V}_{\text{IH}}$	$\text{V}_{\text{CC}}$	Dout	Dout	Dout
Read (X8 bit)		$\text{V}_{\text{IL}}$	$\text{V}_{\text{IL}}$	X	$\text{V}_{\text{IL}}$	$\text{V}_{\text{CC}}$	Dout	High-Z	$\text{V}_{\text{IH}}/\text{V}_{\text{IL}}$
Output disable (X16 bit)		$\text{V}_{\text{IL}}$	$\text{V}_{\text{IH}}$	X	$\text{V}_{\text{IH}}$	$\text{V}_{\text{CC}}$	High-Z	High-Z	High-Z
Output disable (X8 bit)		$\text{V}_{\text{IL}}$	$\text{V}_{\text{IH}}$	X	$\text{V}_{\text{IL}}$	$\text{V}_{\text{CC}}$	High-Z	High-Z	$\text{V}_{\text{IH}}/\text{V}_{\text{IL}}$
Standby	$\text{V}_{\text{IH}}$	X	X	$\text{V}_{\text{SS}} - \text{V}_{\text{CC}}$	$\text{V}_{\text{CC}}$	High-Z	High-Z	High-Z	
Page program	Page program set	$\text{V}_{\text{IH}}$	$\text{V}_{\text{H}}^{*2}$	X	$\text{V}_{\text{PP}}$	$\text{V}_{\text{CC}}$	High-Z	High-Z	High-Z
	Page data latch	$\text{V}_{\text{IL}}$	$\text{V}_{\text{H}}^{*2}$	X	$\text{V}_{\text{PP}}$	$\text{V}_{\text{CC}}$	Din	Din	Din
	Page program	$\text{V}_{\text{IL}}$	$\text{V}_{\text{IH}}$	X	$\text{V}_{\text{PP}}$	$\text{V}_{\text{CC}}$	High-Z	High-Z	High-Z
	Page program verify	$\text{V}_{\text{IH}}$	$\text{V}_{\text{IL}}$	X	$\text{V}_{\text{PP}}$	$\text{V}_{\text{CC}}$	Dout	Dout	Dout
	Page program reset	$\text{V}_{\text{IH}}$	$\text{V}_{\text{IH}}$	X	$\text{V}_{\text{CC}}$	$\text{V}_{\text{CC}}$	High-Z	High-Z	High-Z
Word program	Program	$\text{V}_{\text{IL}}$	$\text{V}_{\text{IH}}$	X	$\text{V}_{\text{PP}}$	$\text{V}_{\text{CC}}$	Din	Din	Din
	Program verify	$\text{V}_{\text{IH}}$	$\text{V}_{\text{IL}}$	X	$\text{V}_{\text{PP}}$	$\text{V}_{\text{CC}}$	Dout	Dout	Dout
	Optional verify	$\text{V}_{\text{IL}}$	$\text{V}_{\text{IL}}$	X	$\text{V}_{\text{PP}}$	$\text{V}_{\text{CC}}$	Dout	Dout	Dout
	Program inhibit	$\text{V}_{\text{IH}}$	$\text{V}_{\text{IH}}$	X	$\text{V}_{\text{PP}}$	$\text{V}_{\text{CC}}$	High-Z	High-Z	High-Z
Identifier		$\text{V}_{\text{IL}}$	$\text{V}_{\text{IL}}$	$\text{V}_{\text{H}}^{*2}$	$\text{V}_{\text{SS}} - \text{V}_{\text{CC}}$	$\text{V}_{\text{CC}}$	Code	Code	Code

- Notes: 1. X: Don't care.  
2.  $\text{V}_{\text{H}}^{*}$ : 12.0 V  $\pm$  0.5 V

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
All input and output voltages	$\text{V}_{\text{in}}, \text{V}_{\text{out}}$	$-0.6^{*2}$ to +7.0	V	1, 2
Voltage on pin A9 and $\overline{\text{OE}}$	$\text{V}_{\text{ID}}$	$-0.6^{*2}$ to +13.0	V	2
$\text{V}_{\text{PP}}$ voltage	$\text{V}_{\text{PP}}$	-0.6 to +13.5	V	1
$\text{V}_{\text{CC}}$ voltage	$\text{V}_{\text{CC}}$	-0.6 to +7.0	V	1
Operating temperature range	$\text{T}_{\text{opr}}$	0 to +70	°C	
Storage temperature range	$\text{T}_{\text{stg}}$	-65 to +125	°C	3
Storage temperature under bias	$\text{T}_{\text{bias}}$	-20 to +80	°C	

- Notes: 1. Relative to  $\text{V}_{\text{SS}}$ .  
2.  $\text{V}_{\text{in}}, \text{V}_{\text{out}}, \text{V}_{\text{ID}}$  min = -2.0 V for pulse width  $\leq$  20 ns  
3. Storage temperature range of device before programming.

HN27C4000FP Series

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Input capacitance	Cin	—	—	12	pF	Vin = 0 V	Except $\overline{\text{BYTE}}/V_{\text{PP}}$
Output capacitance	Cout	—	—	20	pF	Vout = 0 V	

Read Operation

DC Characteristics (VCC = 5 V ± 10%, VPP = VSS to VCC, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	ILi	—	—	2	μA	Vin = 5.5 V
Output leakage current	ILO	—	—	2	μA	Vout = 5.5 V/0.45 V
VPP current	IPP1	—	1	20	μA	VPP = 5.5 V
Standby VCC current	ISB1	—	—	1	mA	$\overline{\text{CE}} = V_{\text{IH}}$
	ISB2	—	1	20	μA	$\overline{\text{CE}} = V_{\text{CC}} \pm 0.3 \text{ V}$
Operating VCC current	ICC1	—	—	35	mA	Iout = 0 mA, f = 1 MHz
	ICC2	—	—	120	mA	Iout = 0 mA, f = 10 MHz
Input voltage	VIL	−0.3 <sup>1</sup>	—	0.8	V	
	VIH	2.2	—	VCC + 1 <sup>2</sup>	V	
Output voltage	VOL	—	—	0.45	V	IOL = 2.1 mA
	VOH	2.4	—	—	V	IOL = −400 μA

Notes: 1. VIL min = −1.0 V for pulse width ≤ 50 ns  
VIL min = −2.0 V for pulse width ≤ 20 ns  
2. VIH max = VCC + 1.5 V for pulse width ≤ 20 ns  
If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{PP} = V_{SS}$  to  $V_{CC}$ ,  $T_a = 0$  to  $+70^{\circ}\text{C}$ )

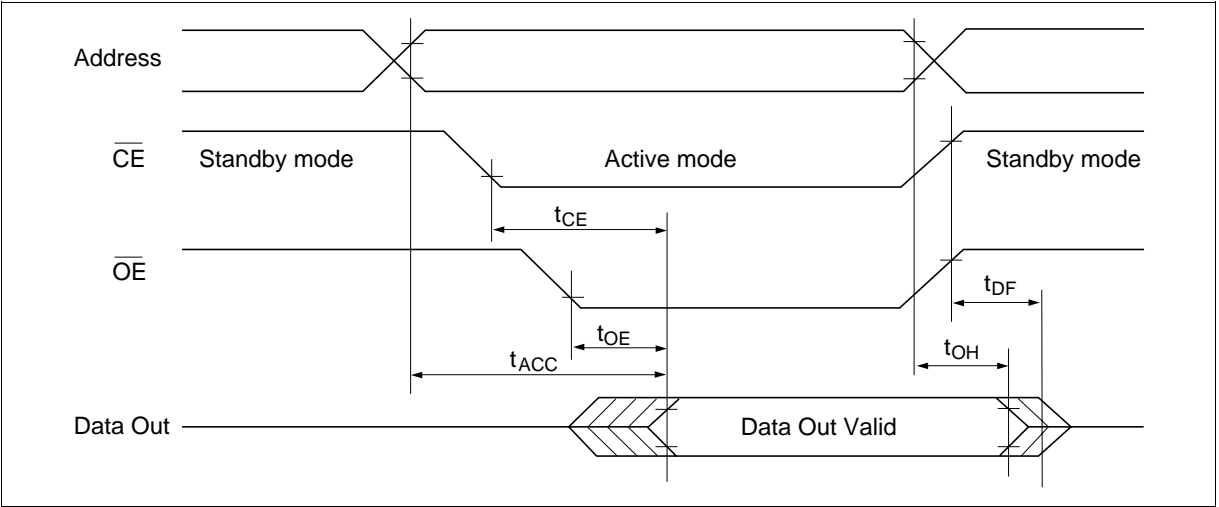
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time:  $\leq 10\text{ ns}$
- Output load: 1 TTL gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

HN27C4000FP							
Parameter	Symbol	-12		-15		Unit	Test Conditions
		Min	Max	Min	Max		
Address to output delay	$t_{ACC}$	—	120	—	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	$t_{CE}$	—	120	—	150	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	$t_{OE}$	—	60	—	70	ns	$\overline{CE} = V_{IL}$
Burst address to output delay	$t_{BAC}$	—	60	—	60	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float <sup>*1</sup>	$t_{DF}$	0	40	0	50	ns	$\overline{CE} = V_{IL}$
Address to output hold	$t_{OH}$	5	—	5	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$

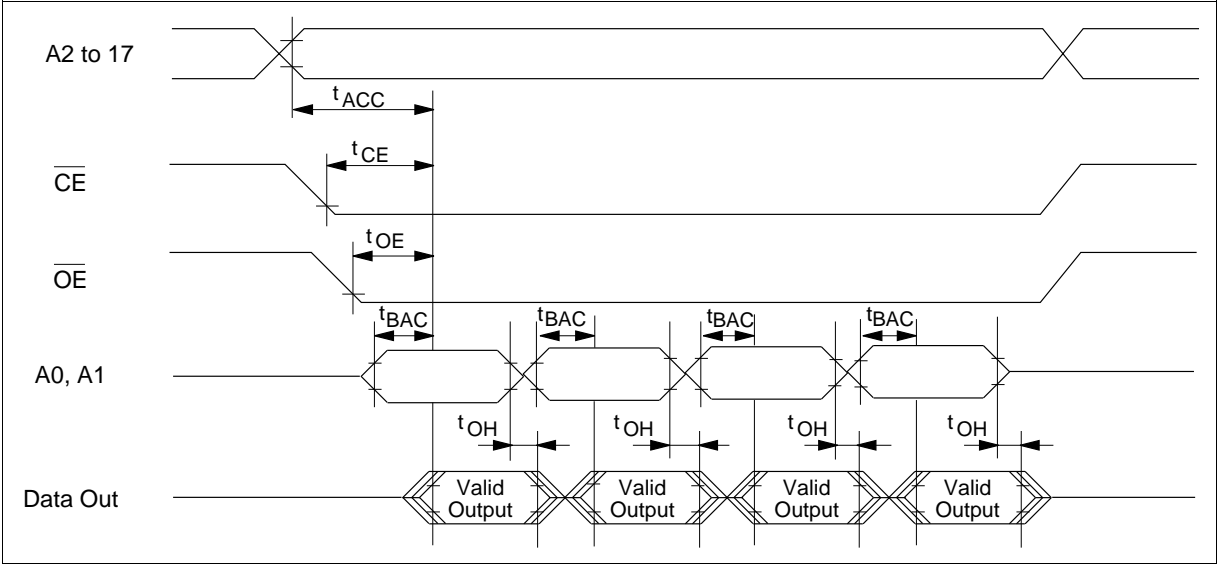
Note: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform

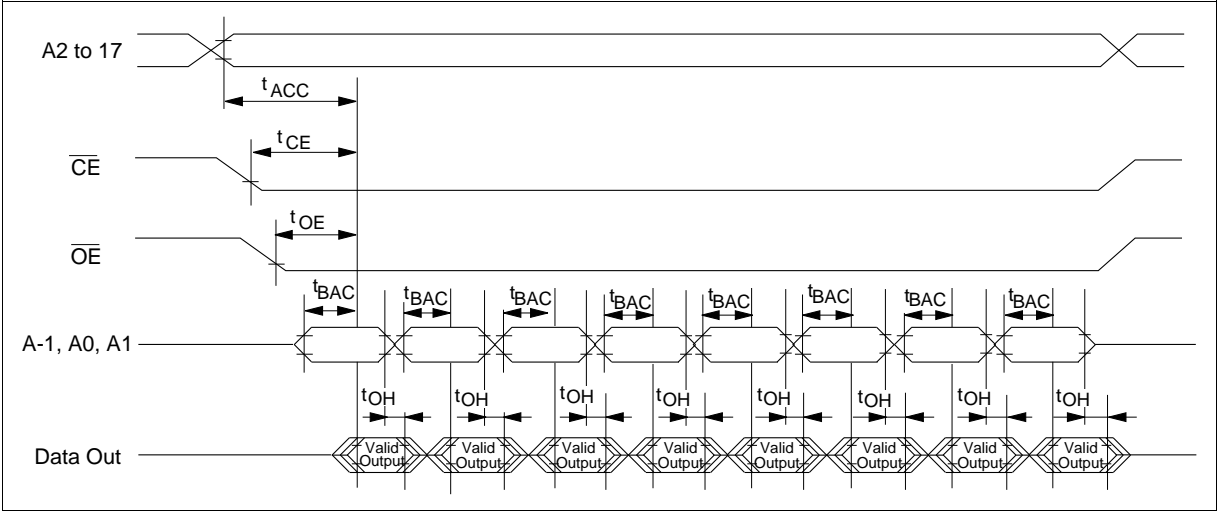


Read Timing Waveform (Burst access mode)

In Burst Access mode, fast read-out of 4 word data is selected by address A0, A1. (Valid only for Read × 16 mode)



In Burst Access mode, fast read-out of 8 byte data is selected by address A-1, A0, A1. (Valid only for Read × 8 mode)





## **Fast High-Reliability Page Programming**

This device can be applied the high performance page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

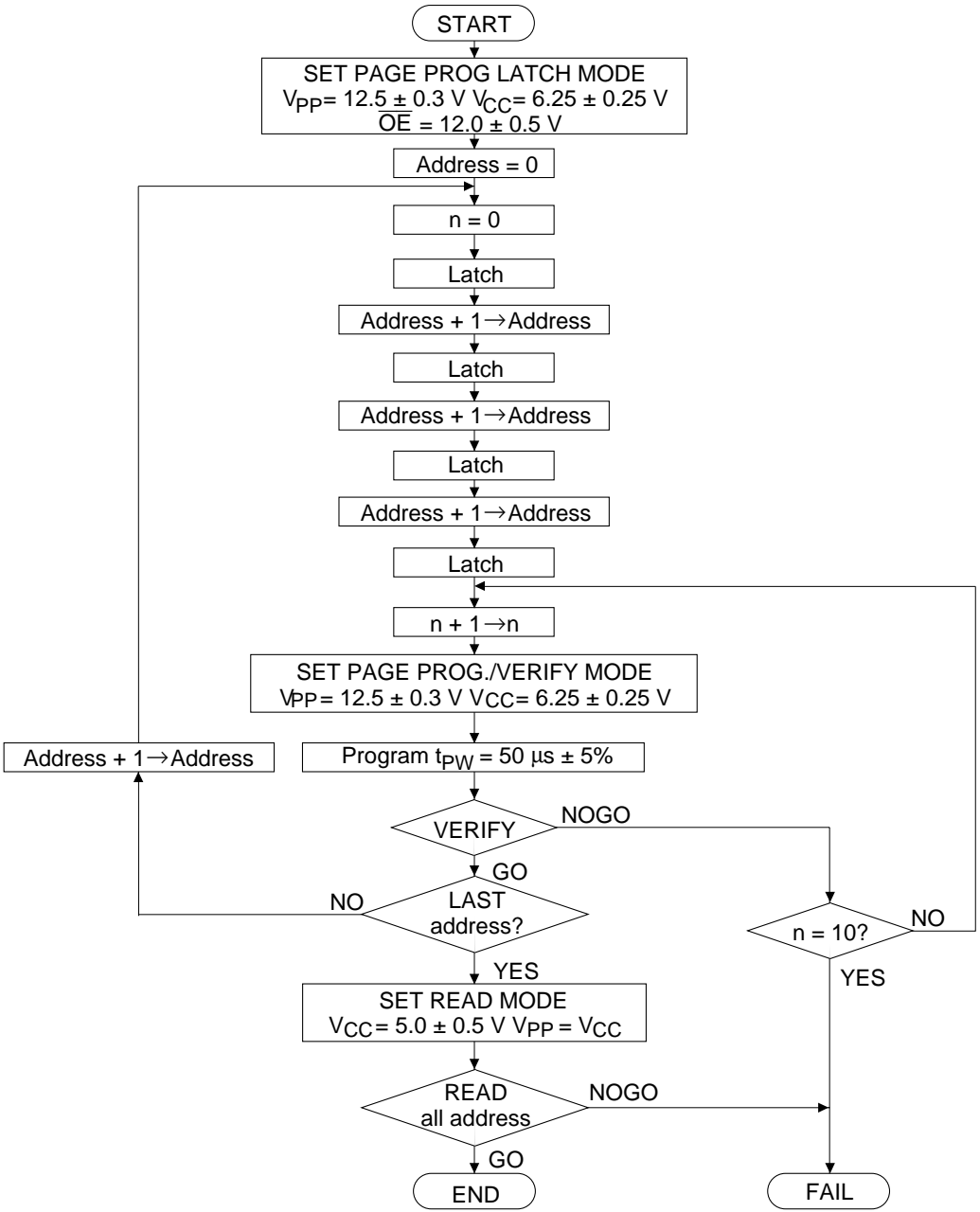
### **Page Program Set**

Apply 12 V to  $\overline{\text{OE}}$  pin after applying 12.5 V to  $V_{\text{PP}}$  to set a page program mode.

The device operates in a page program mode until reset.

### **Page Program Reset**

Set  $V_{\text{PP}}$  to  $V_{\text{CC}}$  level or less to reset a page program mode.



Fast High-Reliability Page Programming Flowchart

**DC Characteristics** ( $V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$ ,  $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{in} = 6.5 \text{ V}/0.45 \text{ V}$
Output voltage during verify	$V_{OL}$	—	—	0.45	V	$I_{OL} = 2.1 \text{ mA}$
	$V_{OH}$	2.4	—	—	V	$I_{OH} = -400 \mu\text{A}$
Operating $V_{CC}$ current	$I_{CC}$	—	—	50	mA	
Input voltage	$V_{IL}$	$-0.1^{*5}$	—	0.8	V	
	$V_{IH}$	2.2	—	$V_{CC} + 0.5^{*6}$	V	
	$V_H$	11.5	12.0	12.5	V	
$V_{PP}$ supply current	$I_{PP}$	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
  2.  $V_{PP}$  must not exceed 13 V including overshoot.
  3. An influence may be had upon device reliability if the device is installed or removed while  $V_{PP} = 12.5 \text{ V}$ .
  4. Do not alter  $V_{PP}$  either  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{low}$ .
  5.  $V_{IL} \text{ min} = -0.6 \text{ V}$  for pulse width  $\leq 20 \text{ ns}$ .
  6. If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ( $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )

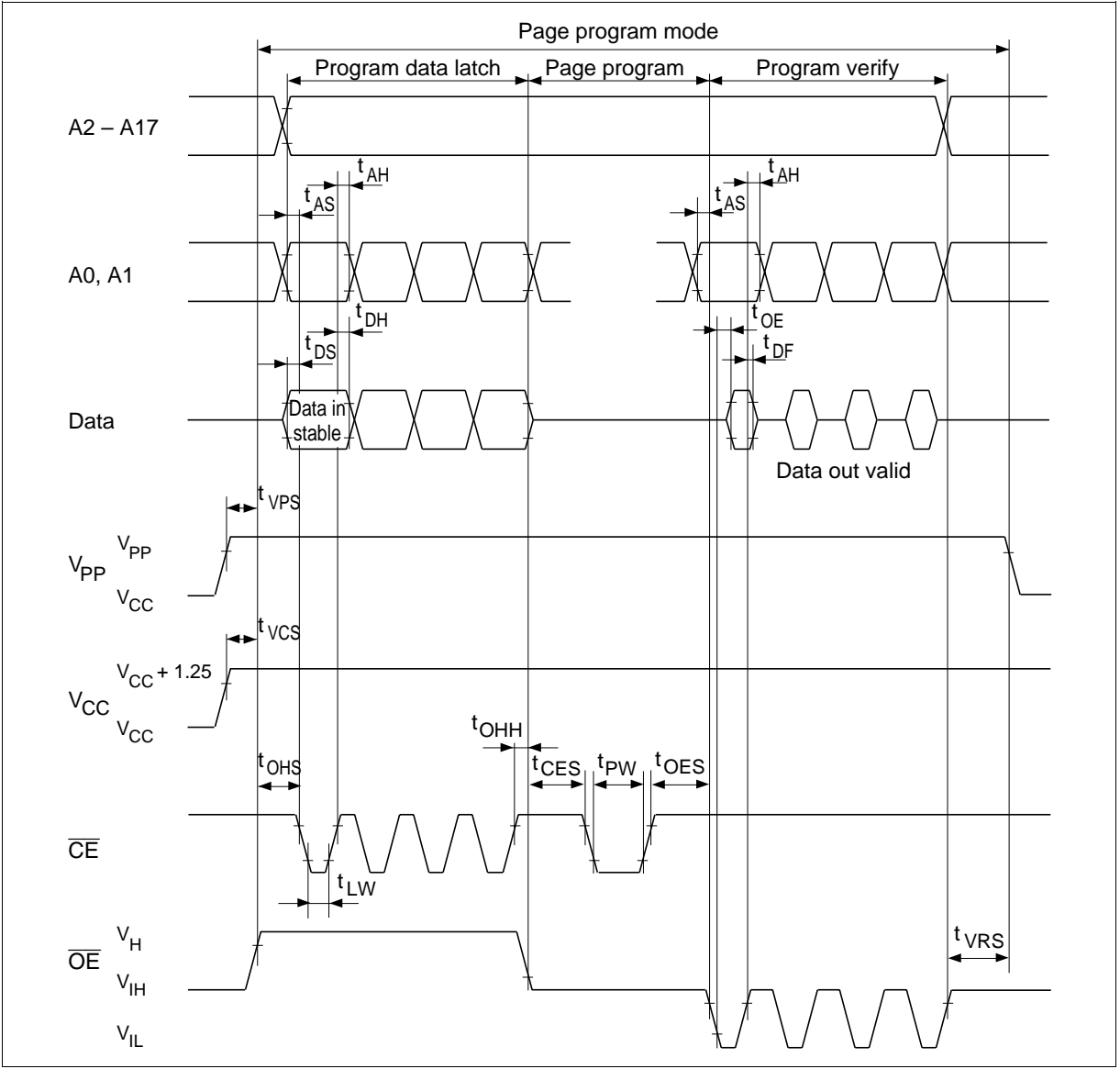
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time:  $\leq 20\text{ ns}$
- Reference levels for measuring timing: Inputs; 0.8 V, 2.0 V,  
Outputs; 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	$t_{AS}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ setup time	$t_{OES}$	2	—	—	$\mu\text{s}$	
Data setup time	$t_{DS}$	2	—	—	$\mu\text{s}$	
Address hold time	$t_{AH}$	0	—	—	$\mu\text{s}$	
Data hold time	$t_{DH}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ high to output float delay	$t_{DF}^{*1}$	0	—	130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2	—	—	$\mu\text{s}$	
$V_{CC}$ setup time	$t_{VCS}$	2	—	—	$\mu\text{s}$	
$\overline{CE}$ initial programming pulse width	$t_{PW}$	47.5	50.0	52.5	$\mu\text{s}$	
$\overline{CE}$ setup time	$t_{CES}$	2	—	—	$\mu\text{s}$	
Data valid from $\overline{OE}$	$t_{OE}$	0	—	150	ns	
$\overline{CE}$ pulse width during data latch	$t_{LW}$	1	—	—	$\mu\text{s}$	
$\overline{OE} = V_H$ setup time	$t_{OHS}$	2	—	—	$\mu\text{s}$	
$\overline{OE} = V_H$ hold time	$t_{OHH}$	2	—	—	$\mu\text{s}$	
$V_{PP}$ hold time <sup>*2</sup>	$t_{VRS}$	1	—	—	$\mu\text{s}$	

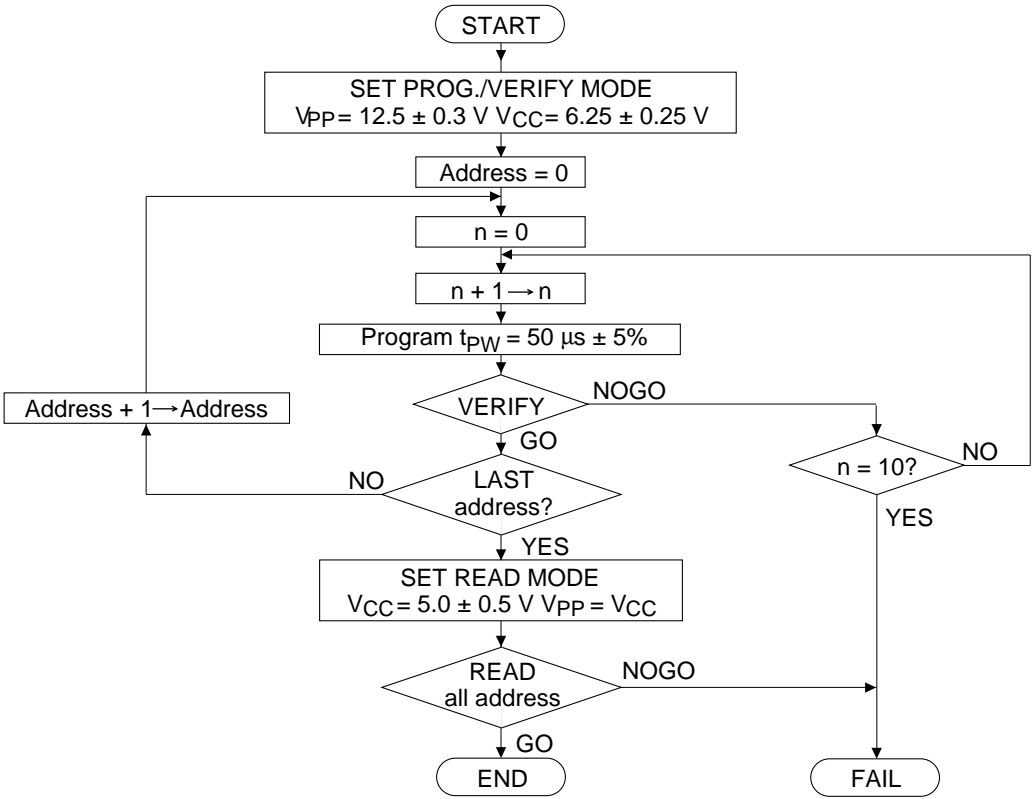
Notes: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.  
2. Page program mode will be reset when  $V_{PP}$  is set to  $V_{CC}$  or less.

Fast High-Reliability Page Programming Timing Waveform



Fast High-Reliability Programming

This device can be applied the fast high-reliability programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

**DC Characteristics** ( $V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$ ,  $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{in} = 6.5 \text{ V}/0.45 \text{ V}$
$V_{PP}$ supply current	$I_{PP}$	—	—	40	$\text{mA}$	$\overline{CE} = V_{IL}$
Operating $V_{CC}$ current	$I_{CC}$	—	—	50	$\text{mA}$	
Input voltage	$V_{IL}$	$-0.1^{*5}$	—	0.8	$\text{V}$	
	$V_{IH}$	2.2	—	$V_{CC} + 0.5^{*6}$	$\text{V}$	
Output voltage	$V_{OL}$	—	—	0.45	$\text{V}$	$I_{OL} = 2.1 \text{ mA}$
	$V_{OH}$	2.4	—	—	$\text{V}$	$I_{OH} = -400 \mu\text{A}$

- Notes: 1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
2.  $V_{PP}$  must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while  $V_{PP} = 12.5 \text{ V}$ .
4. Do not alter  $V_{PP}$  either  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{low}$ .
5.  $V_{IL} \text{ min} = -0.6 \text{ V}$  for pulse width  $\leq 20 \text{ ns}$ .
6. If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.

**AC Characteristics** ( $V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$ ,  $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

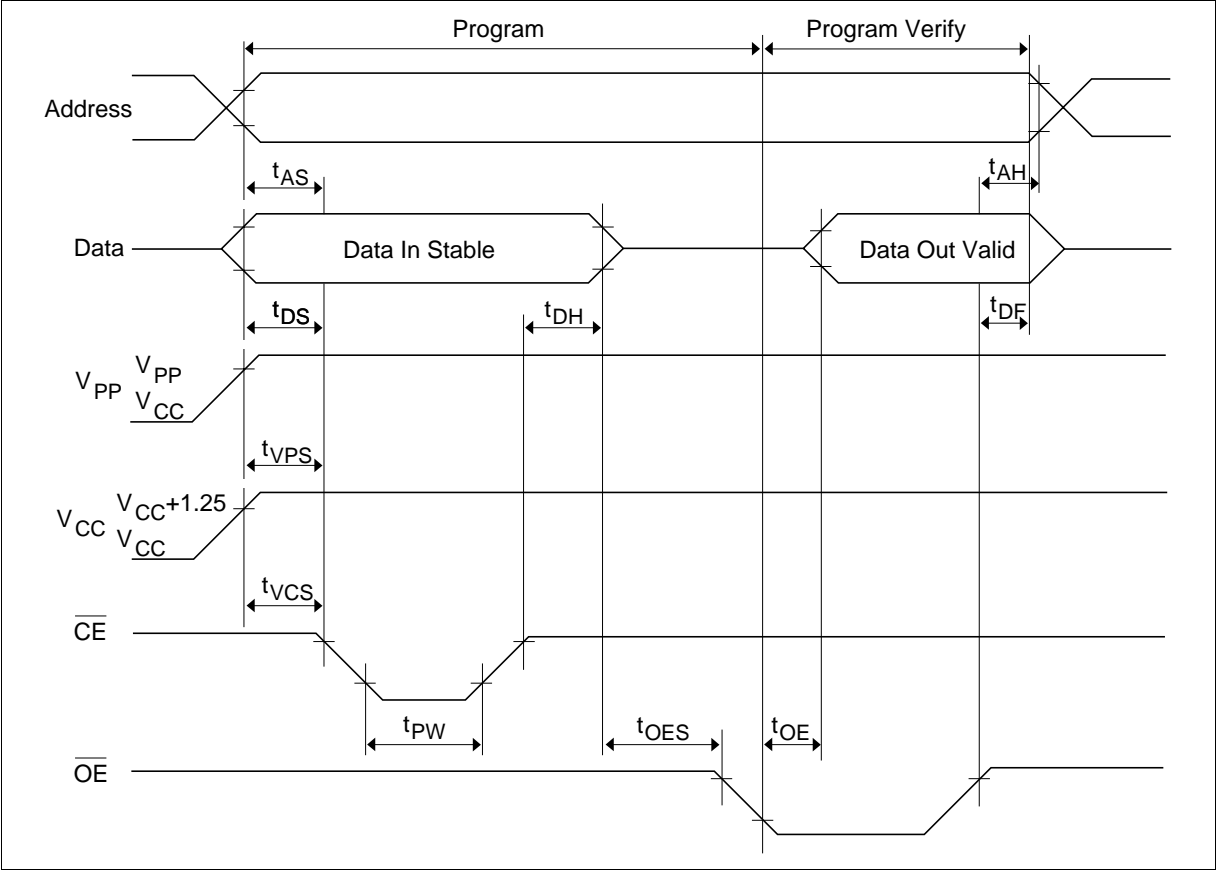
**Test Conditions**

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time:  $\leq 20 \text{ ns}$
- Reference levels for measuring timings: 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	$t_{AS}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ setup time	$t_{OES}$	2	—	—	$\mu\text{s}$	
Data setup time	$t_{DS}$	2	—	—	$\mu\text{s}$	
Address hold time	$t_{AH}$	0	—	—	$\mu\text{s}$	
Data hold time	$t_{DH}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ to output float delay	$t_{DF}^{*1}$	0	—	130	$\text{ns}$	
$V_{PP}$ setup time	$t_{VPS}$	2	—	—	$\mu\text{s}$	
$V_{CC}$ setup time	$t_{VCS}$	2	—	—	$\mu\text{s}$	
$\overline{CE}$ initial programming pulse width	$t_{PW}$	47.5	50.0	52.5	$\mu\text{s}$	
Data valid from $\overline{OE}$	$t_{OE}$	0	—	150	$\text{ns}$	

- Note: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Fast High-Reliability Programming Timing Waveform



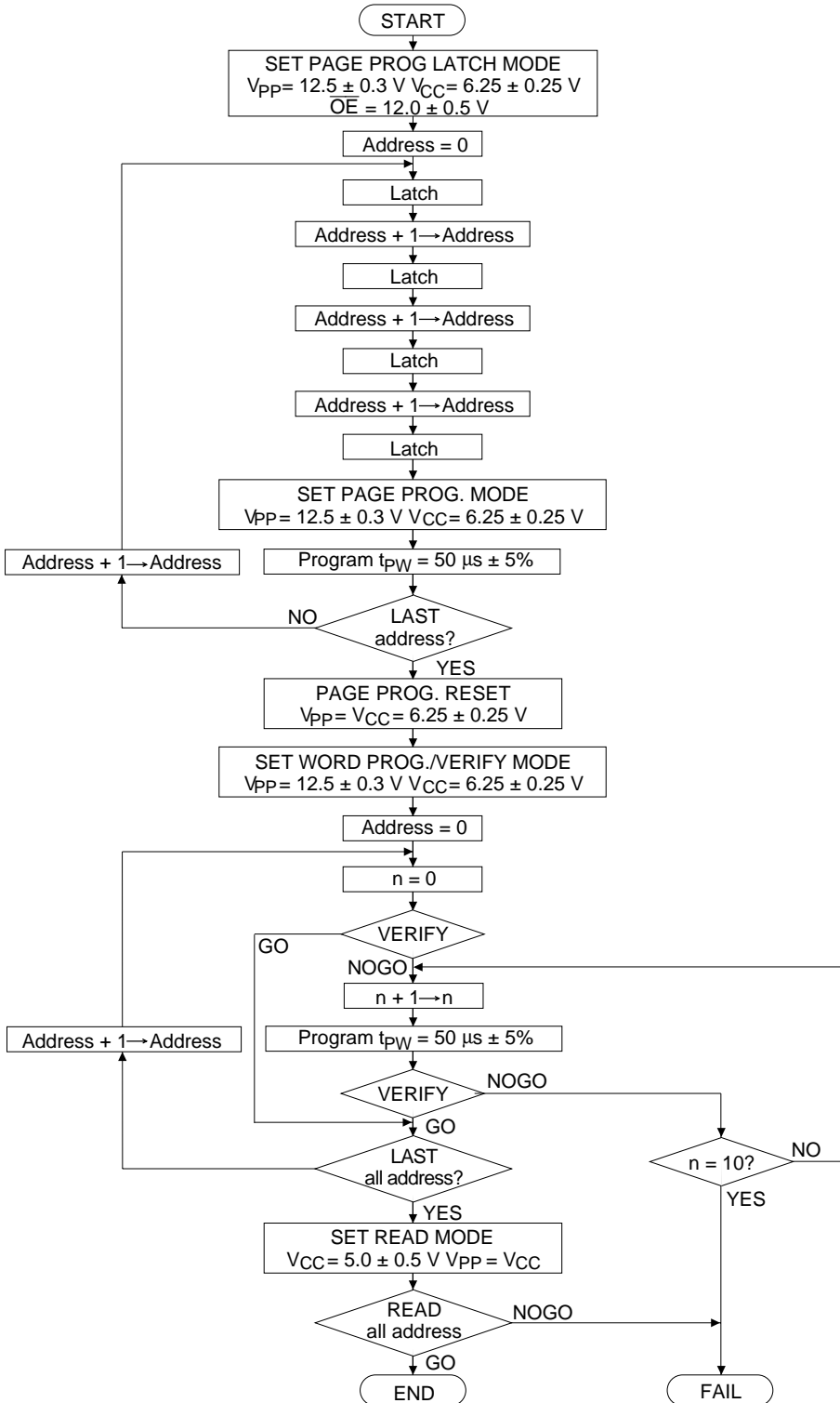
Optional Page Programming

This device can be applied the optional page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

This programming algorithm is the combination of page programming and word verify. It can avoid the increase of programming verify time when a programmer with slow machine cycle is used, and shorten the total programming time.

Regarding the timing specifications for page programming and word verify, please refer to the specifications for fast high-reliability page programming and fast high-reliability programming.





Optional Page Programming Flowchart

# HN27C4000FP Series

DC Characteristics ( $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{in} = 6.5\text{ V}/0.45\text{ V}$
Output voltage during verify	$V_{OL}$	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
	$V_{OH}$	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$
Operating $V_{CC}$ current	$I_{CC}$	—	—	50	mA	
Input voltage	$V_{IL}$	$-0.1^{*5}$	—	0.8	V	
	$V_{IH}$	2.2	—	$V_{CC} + 0.5^{*6}\text{ V}$		
	$V_H$	11.5	12.0	12.5	V	
$V_{PP}$ supply current	$I_{PP}$	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
  2.  $V_{PP}$  must not exceed 13 V including overshoot.
  3. An influence may be had upon device reliability if the device is installed or removed while  $V_{PP} = 12.5\text{ V}$ .
  4. Do not alter  $V_{PP}$  either  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{low}$ .
  5.  $V_{IL}\text{ min} = -0.6\text{ V}$  for pulse width  $\leq 20\text{ ns}$ .
  6. If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.

**AC Characteristics** ( $V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$ ,  $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

**Test Conditions**

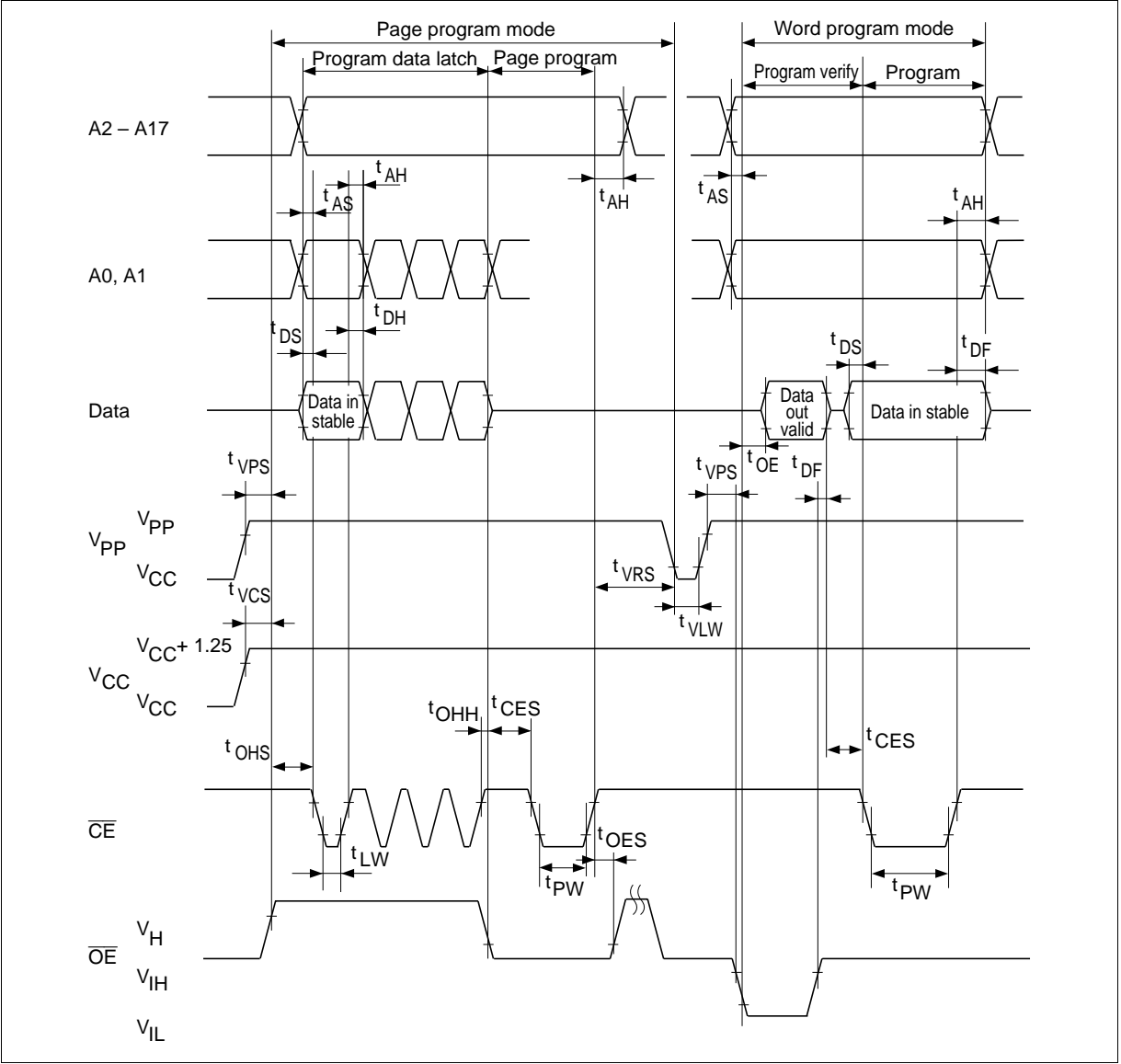
- Input pulse levels:  $\leq 0.45 \text{ V}$  to  $2.4 \text{ V}$
- Input rise and fall time:  $\leq 20 \text{ ns}$
- Reference levels for measuring timings: Inputs;  $0.8 \text{ V}$ ,  $2.0 \text{ V}$   
Outputs;  $0.8 \text{ V}$ ,  $2.0 \text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	$t_{AS}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ setup time	$t_{OES}$	2	—	—	$\mu\text{s}$	
Data setup time	$t_{DS}$	2	—	—	$\mu\text{s}$	
Address hold time	$t_{AH}$	0	—	—	$\mu\text{s}$	
Data hold time	$t_{DH}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ high to output float delay	$t_{DF}^{*1}$	0	—	130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2	—	—	$\mu\text{s}$	
$V_{CC}$ setup time	$t_{VCS}$	2	—	—	$\mu\text{s}$	
$\overline{CE}$ initial programming pulse width	$t_{PW}$	47.5	50.0	52.5	$\mu\text{s}$	
$\overline{CE}$ setup time	$t_{CES}$	2	—	—	$\mu\text{s}$	
Data valid from $\overline{OE}$	$t_{OE}$	0	—	150	ns	
$\overline{CE}$ pulse width during data latch	$t_{LW}$	1	—	—	$\mu\text{s}$	
$\overline{OE} = V_H$ setup time	$t_{OHS}$	2	—	—	$\mu\text{s}$	
$\overline{OE} = V_H$ hold time	$t_{OHH}$	2	—	—	$\mu\text{s}$	
Page programming reset time <sup>*2</sup>	$t_{VLW}$	1	—	—	$\mu\text{s}$	
$V_{PP}$ hold time <sup>*2</sup>	$t_{VRS}$	1	—	—	$\mu\text{s}$	

Notes: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

2. Page program mode will be reset when  $V_{PP}$  is set to  $V_{CC}$  or less.

Option Page Programming Timing Waveform



Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

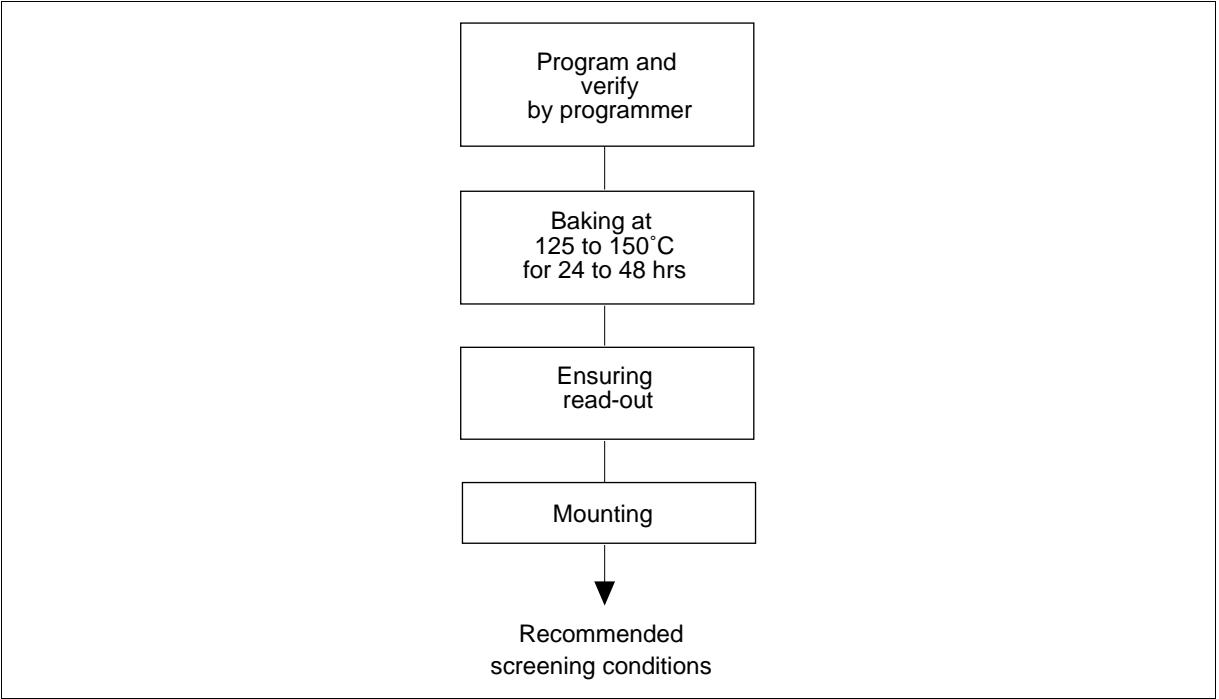
HN27C4000FP Identifier Code

Identifier	FP-40D	A0 (9)	I/O8 – I/O15 —	I/O7 (28)	I/O6 (26)	I/O5 (24)	I/O4 (22)	I/O3 (19)	I/O2 (17)	I/O1 (15)	I/O0 (13)	Hex Data
Manufacturer code		V <sub>IL</sub>	X	0	0	0	0	0	1	1	1	07
Device code		V <sub>IH</sub>	X	1	0	1	0	0	0	0	1	A1

- Notes:
- 1. V<sub>CC</sub> = 5.0 V ± 10%
  - 2. A9 = 12.0 V ± 0.5 V
  - 3.  $\overline{CE}, \overline{OE} = V_{IL}$
  - 4. A1 – A8, A10 – A17: Don't care.
  - 5. X: Don't care.

Recommended Screening Conditions

Before mounting, please make the screening (baking without bias) shown below.



HN27C4000FP Series

Package Dimensions

HN27C4000FP Series (FP-40D)

Unit: mm

