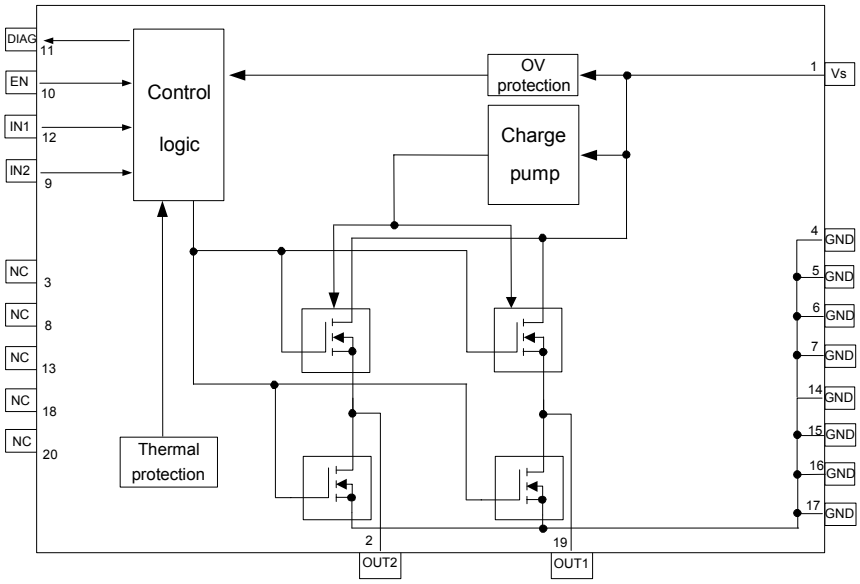
Features

- **Supply Voltage up to 40 V**
- **Operation Voltage up to 16.5 V**
- **$R_{DS\ ON}$ Typically 1 Ω at 27°C, Maximum 2.0 Ω at T_J = 150°C**
- **Up to 1.3 A Output Current**
- **Two Half-bridge Outputs Formed by Two High-side and Two Low-side Drivers**
- **Capable to Switch all Kinds of Loads Such as DC Motors, Bulbs, Resistors, Capacitors and Inductors**
- **Very Low Quiescent Current I_{VS} < 1 µA in Standby Mode**
- **Outputs Short-circuit Protected**
- **Overtemperature Protection**
- **Overvoltage Protection for Supply Voltage up to 40 V**
- **Outputs Withstand DC Voltages up to 40 V**
- **Diagnosis Function for Overtemperature and Overvoltage at the Power Supply**
- **SO20 Power Package**

Description

The ATA6822 is a fully protected driver interface designed in 0.8 µm BCDMOS technology. It is used to control different loads by setting two logic level input signals. The ATA6822 can be configured to cover a wide range of automotive and industrial applications. Each of the push-pull output stages is capable to drive currents up to 1.3 A. The drivers are connected internally to form two half-bridges and can be controlled separately with two logic level input signals. Therefore, all kinds of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC design supports the application as a DC motor driver especially. Protection is guaranteed in terms of short-circuit conditions, overtemperature and overvoltage up to 40 V supply voltage. A diagnosis function in case of overtemperature and overvoltage is embedded. To reduce the overall current consumption the ATA6822 can be switched into standby mode. The output pins are designed to withstand DC voltages up to 40 V. Automotive qualification referring to conducted interferences, EMC protection and 2 kV ESD protection gives added value and enhanced quality for demanding up-market applications.

Figure 1. Block Diagram



Dual Half-bridge DMOS Output Driver

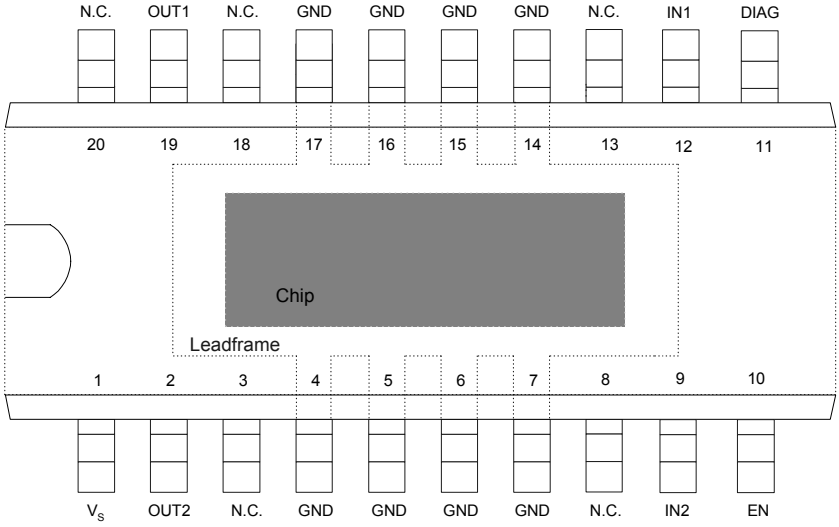
ATA6822

Preliminary

Rev. 4565A–BCD–09/02

Pin Configuration

Figure 2. Pinning SO20



Pin Description

Pin	Symbol	Function
1	V_S	Power supply for output stages OUT1, OUT2 and internal supply.
2	OUT2	Push-pull power output formed by internal high-side switch and low-side switch with internal reverse diodes, short circuit protection, overtemperature protection, diagnosis function for overtemperature and overvoltage.
3	N.C.	Not connected.
4	GND	Ground, reference potential for signal and power, internal connected to pin 5, 6, 7, 14, 15, 16 and 17 by lead frame.
5	GND	Ground, see Pin 4.
6	GND	Ground, see Pin 4.
7	GND	Ground, see Pin 4.
8	N.C.	Ground, see Pin 4.
9	IN2	Schmitt trigger input with hysteresis to control the outputs OUT1 and OUT2.
10	EN	Schmitt trigger input with hysteresis to switch the IC into standby and outputs into tristate condition.
11	DIAG	Diagnosis open drain output, reports overvoltage or overtemperature detection.
12	IN1	Schmitt trigger input with hysteresis to control the outputs OUT1 and OUT2.
13	N.C.	Not connected.
14	GND	Ground, see Pin 4.
15	GND	Ground, see Pin 4.
16	GND	Ground, see Pin 4.
17	GND	Ground, see Pin 4.
18	N.C.	Not connected.
19	OUT1	Push-pull power output, see Pin 2.
20	N.C.	Not connected.

Table 1. Functional Overview

IN1	IN2	EN	OUT1	OUT2	DIAG - Level	Note
---	---	Low	Tristate	Tristate	High	Standby mode
High	High	High	Source	Source	High	Recommended mode for braking DC motors
High	Low	High	Source	Sink	High	
Low	High	High	Sink	Source	High	
Low	Low	High	Sink	Sink	High	
---	---	High	Tristate	Tristate	Low	Overvoltage and overtemperature detected

Functional Description

The basic function is shown in Table 1.

Output Stages

Each of the two output stages, OUT1 and OUT2, can be controlled separately via the logic level input signals, IN1 and IN2. The logic level enable input signal, EN, switches the IC into standby mode reducing overall current consumption to less than 1 µA.

Each of the output stages is capable to drive load currents up to 1.3 A. Depending on the combination of the input signals, IN1 and IN2, different modes for the output stages can be selected, see µ. The output OUT1 as well as output OUT2 can be either switched as current source or as current sink. The outputs are designed to withstand DC voltages up to 40 V. The ON resistance ($R_{DS\ ON}$) of each output stage is 1 Ω at 27°C junction temperature. For worst case calculations a maximum ON resistance ($R_{DS\ ON}$) of 2 Ω needs to be considered.

In DC motor applications the best case for braking is the Source/Source mode, see Table 1. For braking the sink, the driver stage has to be switched into Source mode. Now, the inductive current has a low resistance path to battery voltage, thus the internal IC power dissipation is reduced.

No Shoot-through Condition

An active high side switch off-circuitry prevents shoot-through current, while the output switches are in transition from Source to Sink state or vice versa. Therefore, it is guaranteed that the HS stages are switched off before the LS stages can be activated.

No Leakage Current Condition

In failure mode, like overtemperature and overvoltage, if the high side switch-off circuitry is still activated, a load connected to battery could draw a leakage current from battery to ground. To get a tristate mode as described in Table 1, the high side switch-off circuitry is disabled during failure mode.

Diagnosis

An implemented diagnosis function detects overtemperature and overvoltage conditions. The output, DIAG, is designed as open collector output with an pull up resistor connected externally. The DIAG output current is limited internally.

Overvoltage Protection

The circuit features an overvoltage disable function by monitoring the supply voltage V_{VS}. The overvoltage protection circuitry disables both, the low side as well as the high side output stage, if supply voltage exceeds the voltage threshold 19.5 V. The overvoltage sense comparator provides a hysteresis of 0.9 V. Both outputs are switched into tristate in overvoltage condition and the diagnostic output will be switched on. With a pull up resistor connected to 5 V externally, the output voltage at Pin 11 (DIAG) switches below 0.5 V.

Overtemperature Protection

The thermal shutdown protection circuitry switches off the outputs (tristate) and activate the diagnostic output, if junction temperature exceeds the thermal switch-off threshold temperature of 175°C. In tristate mode the output drivers cool down and if the junction temperature falls below the thermal switch on threshold the outputs switch back into normal operation. The IC is designed with a thermal hysteresis of 15 Kelvin between switch off and switch on state. Depending on the thermal environment of the IC a thermal oscillation has to be considered during output switch-off, cool down and switch-on state.

Short Circuit Protection

The output currents are sensed by a short current protection circuitry and are limited to a maximum short circuit current of approximately 1.7 A.

Absolute Maximum Ratings

All values refer to GND pins.

Parameters	Pin	Symbol	Value	Unit
Supply voltage	1	V_{VS}	-0.3 to +40	V
Logic input voltage	9, 10, 12	V_{EN}, $V_{IN1,2}$	-0.3 to +7	V
Logic output voltage	11	V_{DIAG}	-0.3 to +7	V
Input current	9, 12	$I_{IN1,2}$	-10 to +10	mA
Output short-circuit current -0.3 V < V_{OUT} < V_{VS} +0.3 V	2, 19	$I_{OUT1,2}$	Internally limited	
DC sink current -0.3 V < V_{DIAG} < 7 V	11	I_{DIAG}	Internally limited	
Reverse conducting current (tpulse = 150 µs)	2, 19 towards Pin 1	$I_{Out1,2}$	17	A
Junction temperature range		T_J	-40 to +150	°C
Storage temperature range		T_{STG}	-55 to +150	°C

Thermal Resistance

Parameters	Test Conditions/Pins	Symbol	Value	Unit
Junction pin	Measured to GND: 4 to 7, 14 to 17	R_{thJP}	15	K/W
Junction ambient		R_{thJA}	50 (1)	K/W

Note: 1. Depend on cooling area on PCB

Operating Range

Parameters	Test Conditions/ Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	1	V_{VS}	7		V_ovth (1)	V
Logic input voltage	9, 10, 12	V_{EN}, $V_{IN1, 2}$	-0.3		7	V
Junction temperature range		T_J	-40		150	°C

Note: 1. Threshold for qvervoltage detection

Noise and Surge Immunity

Parameters	Test Conditions	Value
Conduted interference	ISO 7637-1	Level 4 (1)
Interference suppression	VDE 0879 part 2	Level 5
ESD (Human Body Model)	ESD S 5.1	2 kV
ESD (Machine Model)	JEDEC A115A	200 V

Note: 1. Test pulse 5 maximum voltage 40 V (load dump)

Electrical Characteristics

7 V < V_{VS} < 16.5 V, -40°C < T_J < 150°C, EN = HIGH, unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type (*)
1	**Current Consumption**								
1.1	Quiescent current (at VS)	V_{EN} = 0 V, V_{VS} < 16.5 V	1	I_{VS}	-1		5	µA	A
1.3	Supply current (at VS)	EN = 5 V, $I_{OUT1} = I_{OUT2}$ = 0 A	1	I_{VS}			5.5	mA	A
2	**Overvoltage Shutdown**								
2.1	Supply overvoltage threshold		1, 11	V_{ovth}	17.5		20.5	V	A
2.2	Supply overvoltage hysteresis		1, 11	V_{ovth_hys}		0.9		V	A
3	**Thermal Shutdown**								
3.1	Thermal shutdown		9	$T_{J\_switch\ off}$	150	175	200	°C	B
3.2	Thermal shutdown		9	$T_{J\_switch\ on}$	135	160	185	°C	B
3.3	Thermal shutdown hysteresis		9	ΔT_{J_switch}		15		K	B
4	**Output Specification (OUT1, OUT2)**								
4.1	ON resistance to VS or GND		2, 19	$R_{DS\ ON1, 2}$		1	2	Ω	A
4.2	Source overcurrent limitation and shutdown threshold		2, 19	$I_{OUT\ 1, 2}$	-2.2	-1.7	-1.3	A	A
4.3	Sink overcurrent limitation and shutdown threshold		2, 19	$I_{OUT\ 1, 2}$	1.3	1.7	2.2	A	A
4.4	Leakage current	V_{EN} = 0 V, no load connected Low side: $V_{VS} = V_{OUT1} = V_{OUT2}$ = 40 V High side: V_{VS} = 16.5 V, $V_{OUT1} = V_{OUT2}$ = 0 V	2, 19	I_{OUT_leak}	-5		5	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (Continued)

7 V < V_{VS} < 16.5 V, -40°C < T_J < 150°C, EN = HIGH, unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type (*)
4.5	Turn on delay time	See Figure 3 and Figure 4 V_{VS} = 13 V, measured with 93 Ω to GND for high-side and 93 Ω to V_S for low-side	2, 19	t_{ONLH_HS}		50	80	µs	A
4.6	Turn on delay time		2, 19	t_{ONLH_LS}		50	80	µs	A
4.7	Turn off delay time		2, 19	t_{OFFHL_HS}			10	µs	A
4.8	Turn off delay time		2, 19	t_{OFFLH_LS}			1.5	µs	A
4.9	Turn on HS delay time		2, 19	t_{dLH_HS}			10	µs	A
4.10	Turn off LS delay time		2, 19	t_{dLH_LS}			1.5	µs	A
4.11	Turn off HS delay time		2, 19	t_{dHL_HS}			5	µs	A
4.12	Turn on LS delay time		2, 19	t_{dHL_LS}			15	µs	A
5	**Logic Inputs (EN, IN1, IN2)**								
5.1	Low enable voltage		10	V_{ENL}			2	V	A
5.2	High enable voltage		10	V_{ENH}	3.5			V	A
5.3	Hysteresis of enable voltage		10	$\Delta V_{EN\ 1,\ 2}$	200		600	mV	A
5.4	Enable input current	V_{EN} = 5 V	10	I_{EN}		90	200	µA	A
5.5	Low input voltage		9, 12	$V_{IN1,\ 2L}$			2	V	A
5.6	High input voltage		9, 12	$V_{IN1,\ 2H}$	3.5			V	A
5.7	Hysteresis of input voltage		9, 12	$\Delta V_{IN1,\ 2}$	200		600	mV	A
5.8	Input bias current	V_{IN} = 0 V, V_{EN} = 5 V	9, 12	$I_{IN1,\ 2}$	-1	0	1	µA	A
5.9	Pull-down current	V_{IN} = 5 V, V_{EN} = 5 V	9, 12	$I_{IN1,\ 2}$		35	50	µA	A
6	**Logic Output (DIAG)**								
6.1	Diagnostic output drop	I_{DIAG} = 0.5 mA, overvoltage or overtemperature	11	V_{DIAG}			0.5	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 3. Timing Diagram

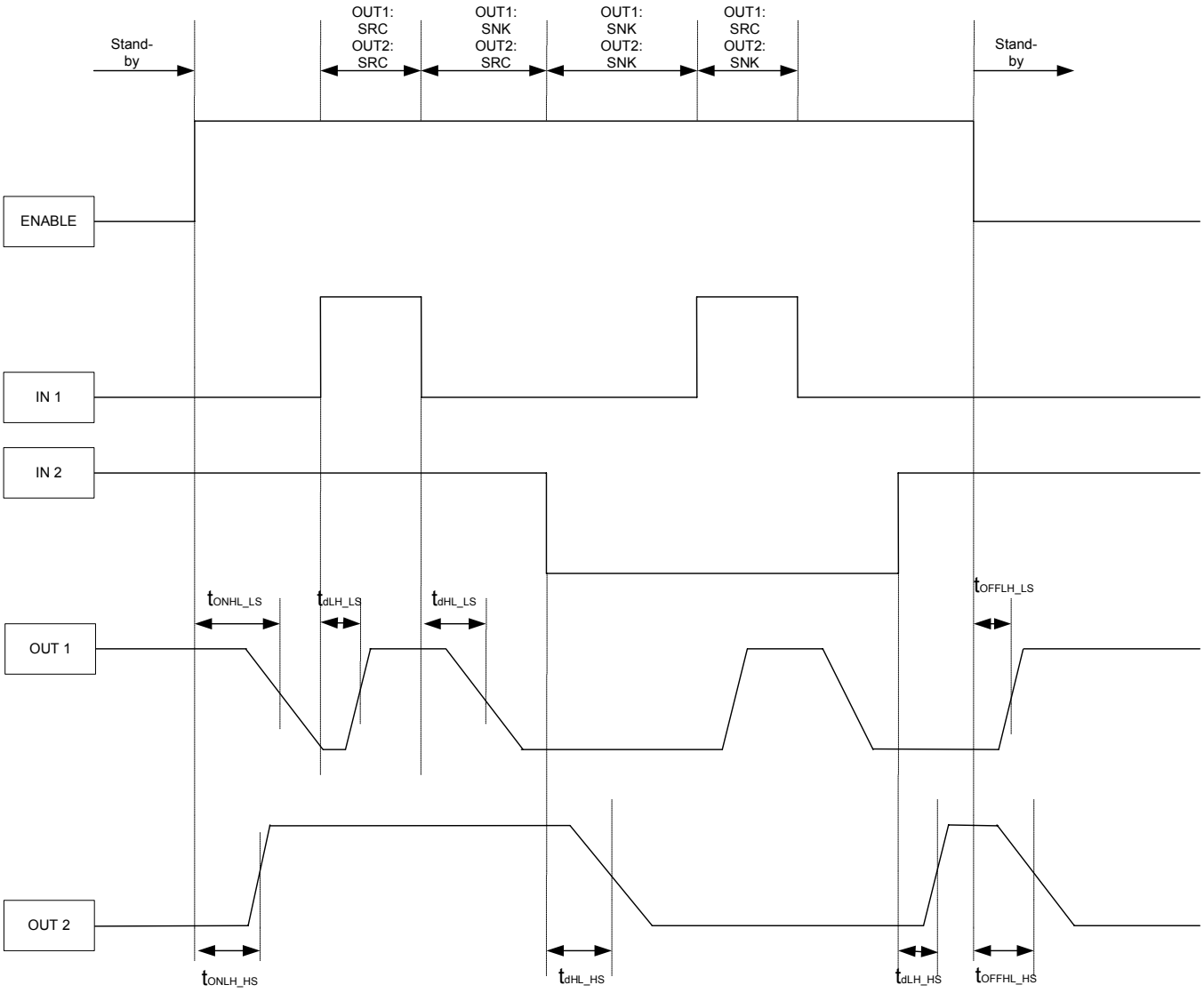


Figure 4. Test Circuit

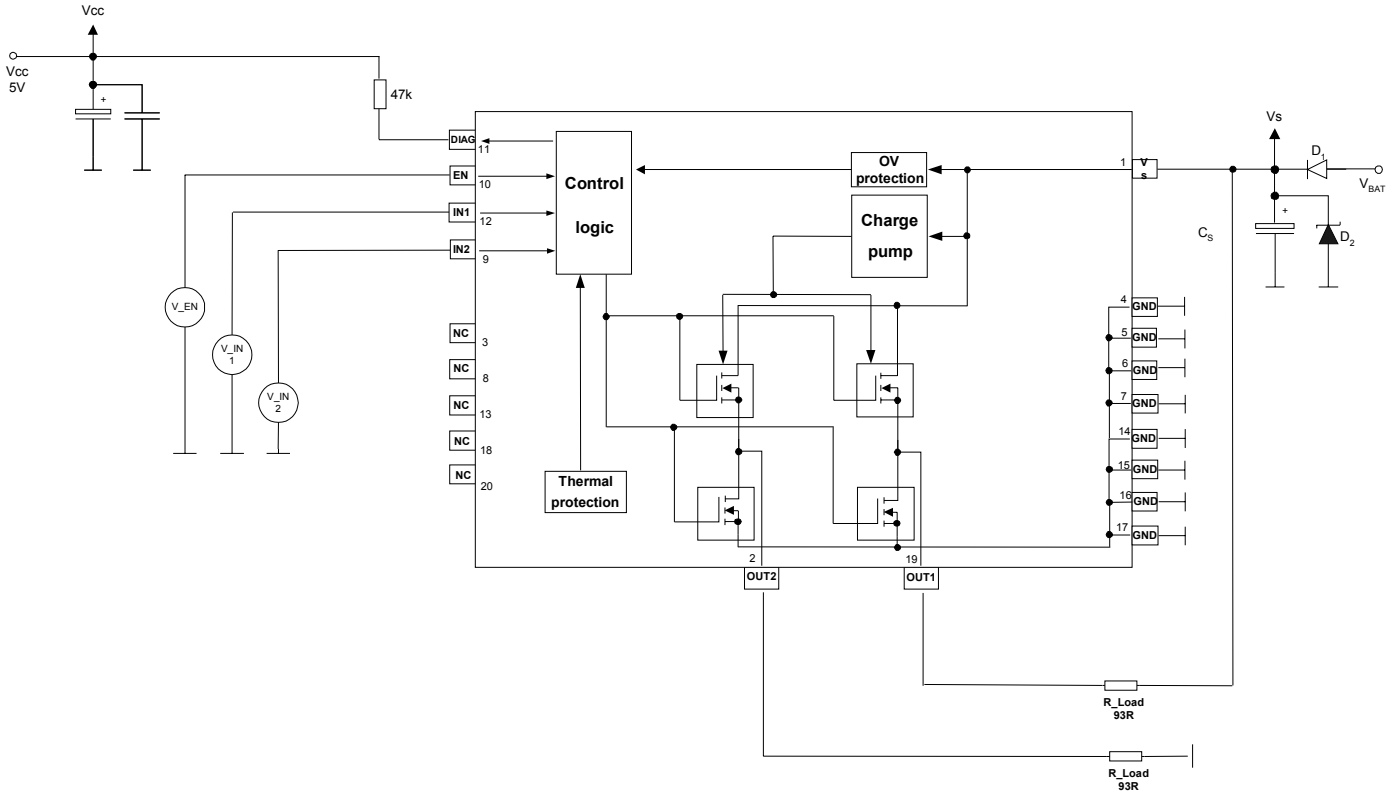
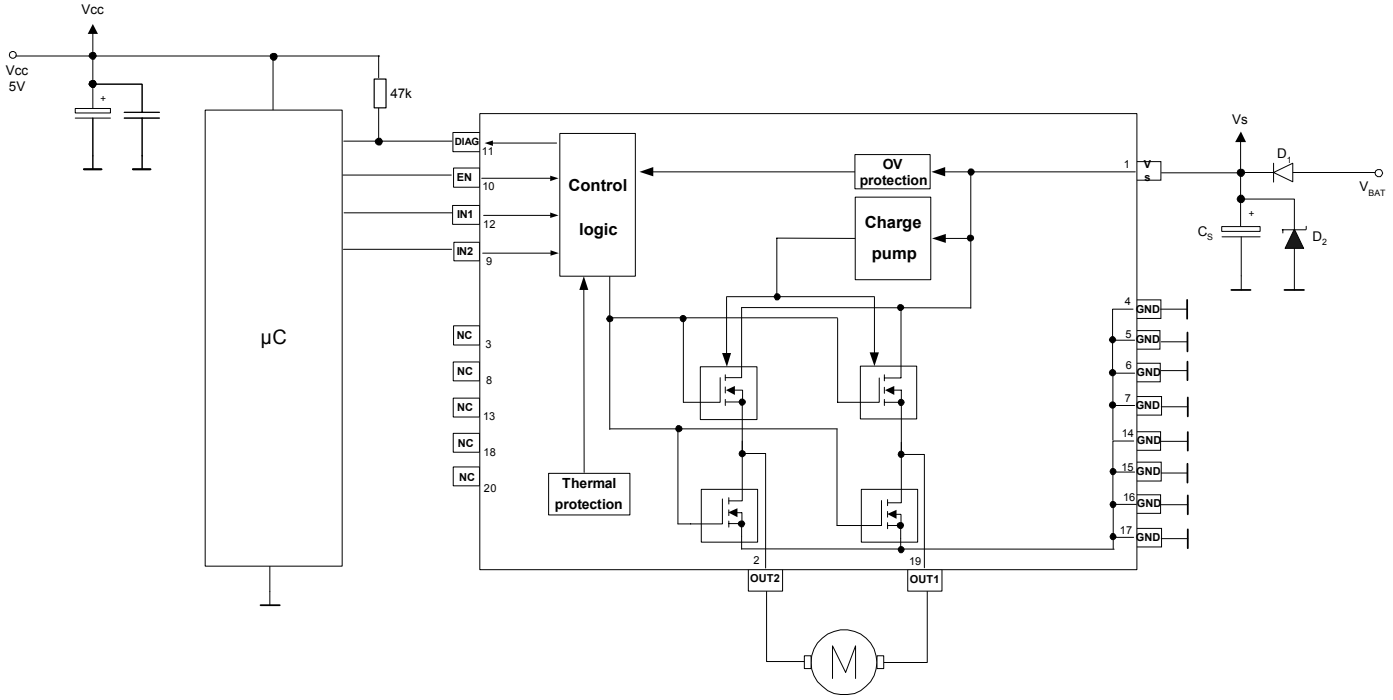


Figure 5. Application Circuit



Application Notes

It is strongly recommended to connect the blocking capacitors at V_S as close as possible to the power supply and GND pins, see Figure 5. Recommended values for capacitors at V_S, electrolytic capacitor C = 22 µF in parallel with a ceramic capacitor C = 100 nF. Value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current I_{OUT} (see Absolute Maximum Ratings). To reduce thermal resistance it is recommended to place cooling areas on the PCB as close as possible to GND pins.

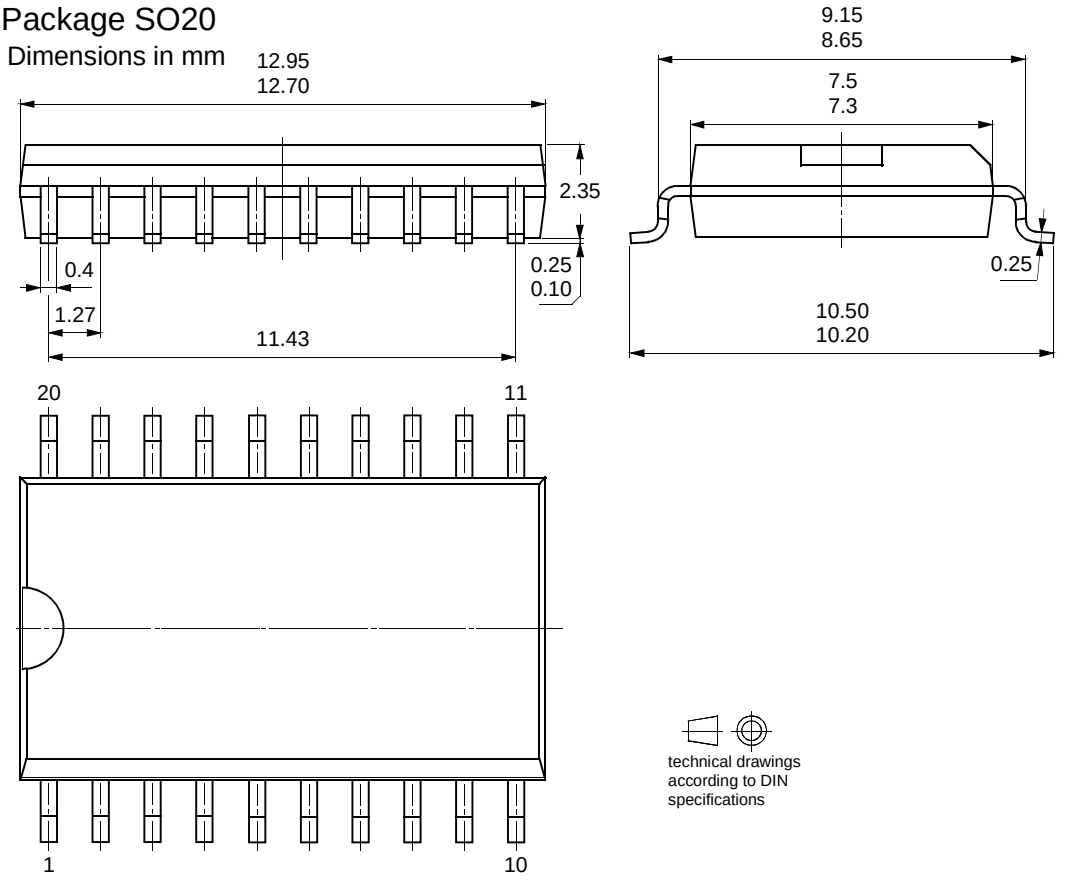
Ordering Information

Extended Type Number	Package	Remarks
ATA6822	SO20	–

Package Information

Package SO20

Dimensions in mm



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