September 2001

National Semiconductor

ADC10D020
Dual 10-Bit, 20 MSPS, 150 mW A/D Converter

General Description

The ADC10D020 is a dual low power, high performance CMOS analog-to-digital converter that digitizes signals to 10 bits resolution at sampling rates up to 30 MSPS while consuming a typical 150 mW from a single 3.0V supply. No missing codes is guaranteed over the full operating temperature range. The unique two stage architecture achieves 9.5 Effective Bits over the entire Nyquist band at 20 MHz sample rate. An output formatting choice of straight binary or 2's complement coding and a choice of two gain settings eases the interface to many systems. Also allowing great flexibility of use is a selectable 10-bit multiplexed or 20-bit parallel mode. An offset correction feature nulls the offset error to less than 1 LSB.

To ease interfacing to most low voltage systems, the digital output power pins of the ADC10D020 can be tied to a separate supply voltage of 1.5V to 3.6V, making the outputs compatible with other low voltage systems. When not converting, power consumption can be reduced by pulling the PD (Power Down) pin high, placing the converter into a low power state where it typically consumes less than 1 mW and from which recovery is about 1 ms. Bringing the STBY (Standby) pin high places the converter into a standby mode where power consumption is about 27 mW and from which recovery is 800 ns.

The ADC10D020's speed, resolution and single supply operation makes it well suited for a variety of applications, including high speed portable applications.

Operating over the industrial ($-40^\circ \le T_A \le +85^\circ C$) temperature range, the ADC10D020 is available in a 48-pin TQFP. An evaluation board is available to ease the design effort.

Features

- Internal sample-and-hold
- Dual gain settings
- Offset correction
- Selectable straight binary or 2's complement output
- Multiplexed or parallel output bus
- Single +2.7V to 3.6V operation
- Power down and standby modes
- 3V TTL Logic input/output compatible

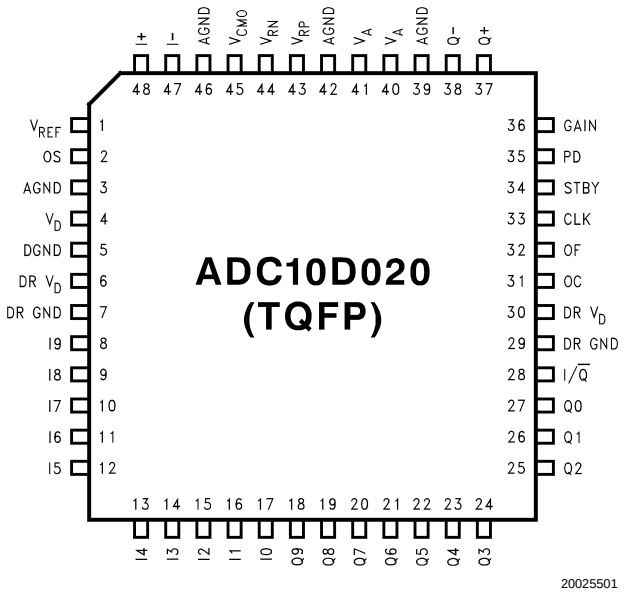
Key Specifications

■ Resolution	10 Bits
■ Conversion Rate	20 MSPS
■ ENOB	9.5 Bits (typ)
■ DNL	0.35 LSB (typ)
■ Conversion Latency Parallel Outputs	2.5 Clock Cycles
— Multiplexed Outputs, I Data Bus	2.5 Clock Cycles
— Multiplexed Outputs, Q Data Bus	3 Clock Cycles
■ PSRR	50 dB
■ Power Consumption — Normal Operation	150 mW (typ)
— Power Down Mode	1 mW (typ)
— Fast Recovery Standby Mode	27 mW (typ)

Applications

- Digital Video
- CCD Imaging
- Portable Instrumentation
- Communications
- Medical Imaging
- Ultrasound

Connection Diagram



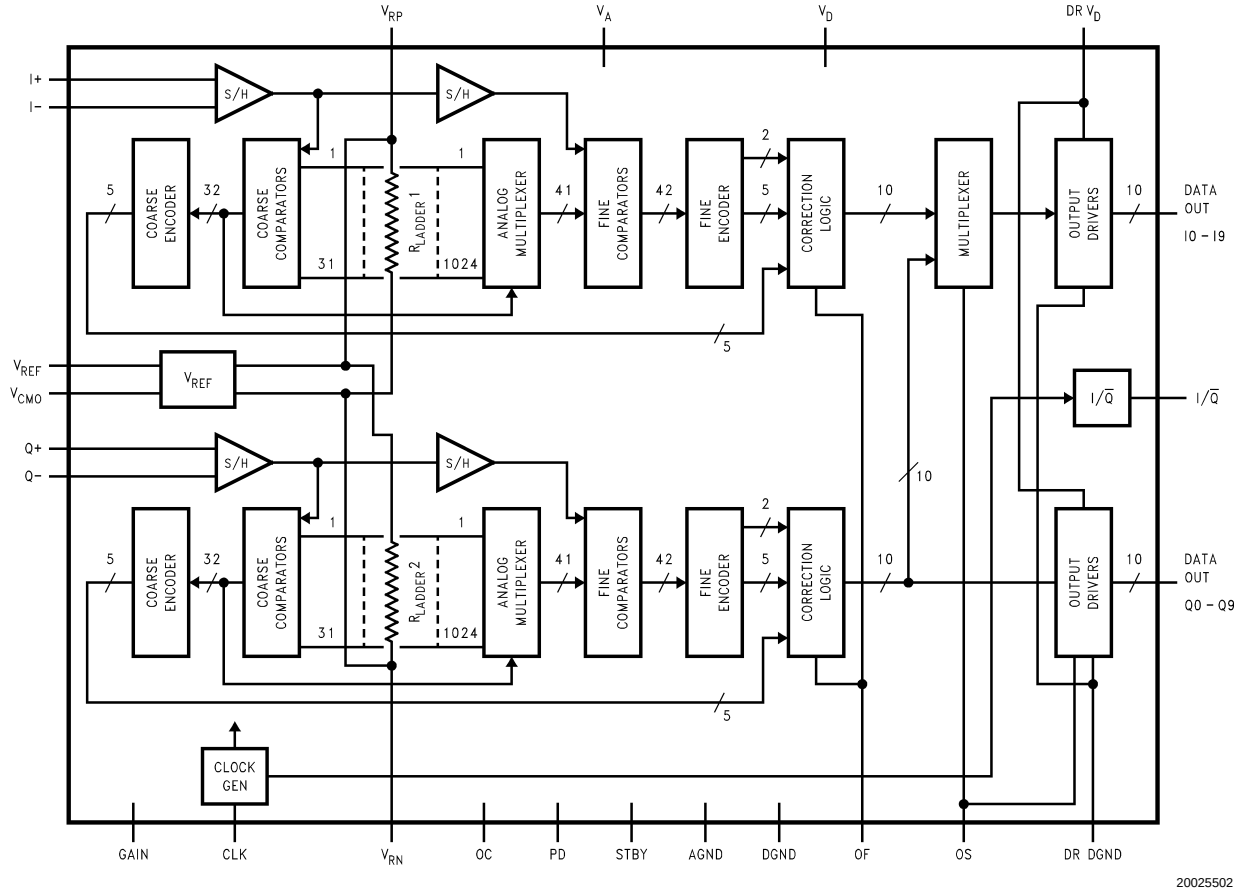
20025501

TOP VIEW

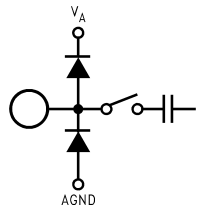
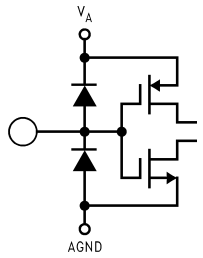
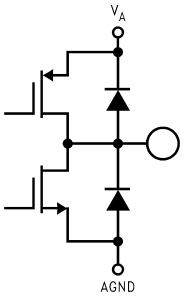
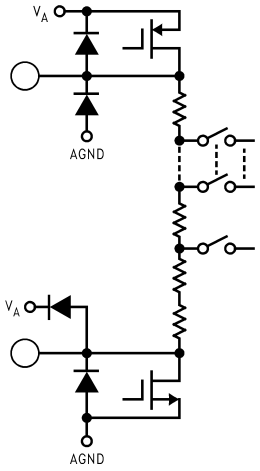
Ordering Information

Industrial Temperature Range ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	NS Package
ADC10D020CIVS	TQFP
ADC10D020EVAL	Evaluation Board

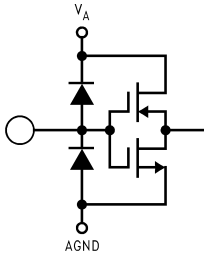
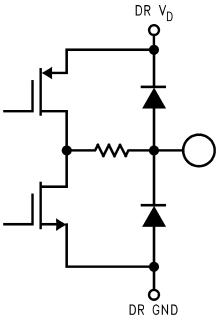
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
48 47	I+ I−		Analog inputs to “I” ADC. Nominal conversion range is 1.25V to 1.75V with GAIN pin low, or 1.0V to 2.0V with GAIN pin high.
37 38	Q+ Q−		Analog inputs to “Q” ADC. Nominal conversion range is 1.25V to 1.75V with GAIN pin low, or 1.0V to 2.0V with GAIN pin high.
1	V_{REF}		Analog Reference Voltage input. The voltage at this pin should be in the range of 0.8V to 1.5V. With 1.0V at this pin and the GAIN pin *low*, the full scale differential inputs are 1 V_{P-P}. With 1.0V at this pin and the GAIN pin *high*, the full scale differential inputs are 2 V_{P-P}. This pin should be bypassed with a 1 µF capacitor.
45	V_{CMO}		This is an analog output which can be used to set the common mode voltage of the input. It should be bypassed with a minimum of 2 µF low ESR capacitor in parallel with a 0.1 µF capacitor. This pin has a nominal output voltage of 1.5V and has a 1 mA output capability.
43	V_{RP}		Top of the reference ladder. **Do not drive this pin.** Bypass this pin with a 10 µF low ESR capacitor and a 0.1 µF capacitor.
44	V_{RN}		Bottom of the reference ladder. **Do not drive this pin.** Bypass this pin with a 10 µF low ESR capacitor and a 0.1 µF capacitor.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
33	CLK		Digital clock input for both converters. The analog inputs are sampled on the falling edge of this clock input.
2	OS		Output Bus Select. With this pin at a logic high, both the "I" and the "Q" data are present on their respective 10-bit output buses (Parallel mode of operation). When this pin is at a logic low, the "I" and "Q" data are multiplexed onto the "I" output bus and the "Q" output lines all remain at a logic low (multiplexed mode).
31	OC		Offset Correct pin. A low-to-high transition on this pin initiates an independent offset correction sequence for each converter, which takes 34 clock cycles to complete. During this time 32 conversions are taken and averaged. The result is subtracted from subsequent conversions. Each input pair should have 0V differential value during this entire 34 clock period.
32	OF		Output Format pin. When this pin is LOW the output format is Straight Binary. When this pin is HIGH the output format is 2's complement. This pin may be changed "on the fly", but this will result in errors for one or two conversions.
34	STBY		Standby pin. The device operates normally with a logic low on this and the PD (Power Down) pin. With this pin at a logic high and the PD pin at a logic low, the device is in the standby mode where it consumes just 27 mW of power. It takes just 800 ns to come out of this mode after the STBY pin is brought low.
35	PD		Power Down pin that, when high, puts the converter into the Power Down mode where it consumes just 1 mW of power. It takes 1 ms to recover from this mode after the PD pin is brought low. If both the STBY and PD pins are low simultaneously, the PD pin dominates.
36	GAIN		This pin sets the internal signal gain at the inputs to the ADCs. With this pin low the full scale differential input peak-to-peak signal is equal to V_{REF}. With this pin high the full scale differential input peak-to-peak signal is equal to 2 x V_{REF}.
8 thru 27	I0–I9 and Q0–Q9		3V TTL/CMOS-compatible Digital Output pins that provide the conversion results of the I and Q inputs. I0 and Q0 are the LSBs, I9 and Q9 are the MSBs. Valid data is present just after the rising edge of the CLK input in the Parallel mode. In the multiplexed mode, valid data is present just after the rising edge of the CLK input for I0–I9 and just after the falling edge of the CLK input for Q0–Q9.
28	I/$\overline{Q}$		Output data valid signal. In the multiplexed mode, this pin transitions from low to high when the data bus transitions from Q-data to I-data, and from high to low when the data bus transitions from I-data to Q-data. In the Parallel mode, this pin transitions from low to high as the output data changes.
40, 41	V_A		Positive analog supply pin. This pin should be connected to a quiet voltage source of +2.7V to +3.6V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
4	V_D		Positive digital supply pins. These pins should be connected to a quiet voltage source of +2.7V to +3.6V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.
6, 30	DR V_D		Positive digital output pins. These pins should be connected to a clean, quiet voltage source of +1.5V to V_D and be bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors. These pins should also be well decoupled from V_A and V_D and never exceed V_D.
3, 39, 42, 46	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC10D020 package.
5	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC10D020 package.
7, 29	DR GND		The ground return of the digital output drivers.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltages	3.8V
Voltage on Any Pin	−0.3V to (V_A or V_D +0.3V)
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Package Dissipation at T_A = 25˚C	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2500V
Machine Model	250V
Soldering Temperature,	
Infrared, 10 sec. (Note 6)	235˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	−40˚C ≤ T_A ≤ +85˚C
V_A, V_D Supply Voltage	+2.7V to +3.6V
DR V_D Supply Voltage	+1.5V to V_D
V_{IN} Differential Voltage Range	
GAIN = Low	V_{REF}/2
GAIN = High	V_{REF}
V_{CM} Input Common Mode Range	
GAIN = Low	V_{REF}/4 to (V_A–V_{REF}/4)
GAIN = High	V_{REF}/2 to (V_A–V_{REF}/2)
V_{REF} Voltage Range	0.8V to 1.5V
Digital Input Pins Voltage Range	−0.3V to (V_A +0.3V)

Converter Electrical Characteristics

The following specifications apply for V_A = +3.0 V_{DC}, V_D = +3.0 V_{DC}, DR V_D = +3.0 V_{DC}, V_{REF} = 1.0 V_{DC}, GAIN = OF = 0V, OS = 3.0V, V_{IN} (ac coupled) = FSR = 1.0 V_{P-P}, C_L = 15 pF, f_{CLK} = 20 MHz, 50% Duty Cycle, R_S = 50Ω, t_{rc} = t_{fc} = 2 ns, NOT offset corrected. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25˚C (Note 7).

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
INL	Integral Non-Linearity		±0.65	**±1.8**	LSB(max)
DNL	Differential Non-Linearity		±0.35	**+1.2**	LSB(max)
				−1.0	LSB(min)
	Resolution with No Missing Codes			**10**	Bits
V_{OFF}	Offset Error	Without Offset Correction	−5	+10	LSB(max)
				−16	LSB(min)
		With Offset Correction	+0.5	+2.0	LSB(max)
				−1.5	LSM(min)
GE	Gain Error		−4	**+6**	%FS(max)
				−14	%FS(min)
DYNAMIC CONVERTER CHARACTERISTICS					
ENOB	Effective Number of Bits	f_{IN} = 1.0 MHz, V_{IN} = FSR −0.1 dB	9.5		Bits
		f_{IN} = 4.7 MHz, V_{IN} = FSR −0.1 dB	9.5	**9.0**	Bits(min)
		f_{IN} = 9.5 MHz, V_{IN} = FSR −0.1 dB	9.5		Bits
		f_{IN} = 19.5 MHz, V_{IN} = FSR −0.1 dB	9.5		Bits
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 1.0 MHz, V_{IN} = FSR −0.1 dB	59		dB
		f_{IN} = 4.7 MHz, V_{IN} = FSR −0.1 dB	59	**56**	dB(min)
		f_{IN} = 9.5 MHz, V_{IN} = FSR −0.1 dB	59		dB
		f_{IN} = 19.5 MHz, V_{IN} = FSR −0.1 dB	59		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 1.0 MHz, V_{IN} = FSR −0.1 dB	59		dB
		f_{IN} = 4.7 MHz, V_{IN} = FSR −0.1 dB	59	**56**	dB(min)
		f_{IN} = 9.5 MHz, V_{IN} = FSR −0.1 dB	59		dB
		f_{IN} = 19.5 MHz, V_{IN} = FSR −0.1 dB	59		dB
THD	Total Harmonic Distortion	f_{IN} = 1.0 MHz, V_{IN} = FSR −0.1 dB	−73		dB
		f_{IN} = 4.7 MHz, V_{IN} = FSR −0.1 dB	−73	**−62**	dB(min)
		f_{IN} = 9.5 MHz, V_{IN} = FSR −0.1 dB	−73		dB
		f_{IN} = 19.5 MHz, V_{IN} = FSR −0.1 dB	−73		dB

Converter Electrical Characteristics (Continued)

The following specifications apply for V_A = +3.0 V_{DC}, V_D = +3.0 V_{DC}, DR V_D = +3.0 V_{DC}, V_{REF} = 1.0 V_{DC}, GAIN = OF = 0V, OS = 3.0V, V_{IN} (ac coupled) = FSR = 1.0 V_{P-P}, C_L = 15 pF, f_{CLK} = 20 MHz, 50% Duty Cycle, R_S = 50Ω, t_{rc} = t_{fc} = 2 ns, NOT offset corrected. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25˚C (Note 7).

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS					
HS2	Second Harmonic	f_{IN} = 1.0 MHz, V_{IN} = FSR −0.1 dB	−84		dB
		f_{IN} = 4.7 MHz, V_{IN} = FSR −0.1 dB	−92		dB
		f_{IN} = 9.5 MHz, V_{IN} = FSR −0.1 dB	−87		dB
		f_{IN} = 19.5 MHz, V_{IN} = FSR −0.1 dB	−87		dB
HS3	Third Harmonic	f_{IN} = 1.0 MHz, V_{IN} = FSR −0.1 dB	−78		dB
		f_{IN} = 4.7 MHz, V_{IN} = FSR −0.1 dB	−80		dB
		f_{IN} = 9.5 MHz, V_{IN} = FSR −0.1 dB	−80		dB
		f_{IN} = 19.5 MHz, V_{IN} = FSR −0.1 dB	−78		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 1.0 MHz, V_{IN} = FSR −0.1 dB	76		dB
		f_{IN} = 4.7 MHz, V_{IN} = FSR −0.1 dB	75		dB
		f_{IN} = 9.5 MHz, V_{IN} = FSR −0.1 dB	75		dB
		f_{IN} = 19.5 MHz, V_{IN} = FSR −0.1 dB	74		dB
IMD	Intermodulation Distortion	f_{IN1} < 4.0 MHz, V_{IN} = FSR −6.1 dB f_{IN2} < 6.0 MHz, V_{IN} = FSR −6.1 dB	60		dB
	Overrange Output Code	(V_{IN+}−V_{IN-}) > 1.1V		**1023**	
	Underrange Output Code	(V_{IN+}−V_{IN-}) < −1.1V		**0**	
FPBW	Full Power Bandwidth		140		MHz
INTER-CHANNEL CHARACTERISTICS					
	Channel - Channel Isolation	1 MHz input to tested channel, 4.75 MHz input to other channel	90		dB
	Channel - Channel Aperture Delay Match	f_{IN} = 8 MHz	8.5		ps
	Channel - Channel Gain Matching		0.03		%FS
REFERENCE AND ANALOG CHARACTERISTICS					
V_{IN}	Analog Differential Input Range	Gain Pin = AGND	1		V_{P-P}
		Gain Pin = V_A	2		V_{P-P}
C_{IN}	Analog Input Capacitance (each input)	Clock High	5		pF
		Clock Low	3		pF
R_{IN}	Analog Differential Input Resistance		90		kΩ
V_{REF}	Reference Voltage		1.0	**0.8**	V(min)
				1.5	V(max)
I_{REF}	Reference Input Current		1		µA
V_{CMO}	Common Mode Voltage Output	1 mA load to ground (sourcing current)	1.5	**1.35**	V(min)
				1.6	V(max)
TC V_{CMO}	Common Mode Voltage Temperature Coefficient		20		ppm/˚C
DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Logical “1” Input Voltage	V_A = +2.7V		**2.0**	V(min)
V_{IL}	Logical “0” Input Voltage	V_A = +3.6V		**0.5**	V(max)
I_{IH}	Logical “1” Input Current	V_{IH} = V_A	1		µA
I_{IL}	Logical “0” Input Current	V_{IL} = DGND	−1		µA
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Logical “1” Output Voltage	DR V_D = +2.7V, I_{OUT} = −0.5 mA		**DR V_D −0.3V**	V(min)
V_{OL}	Logical “0” Output Voltage	DR V_D = +2.7V, I_{OUT} = 1.6 mA		**0.4**	V(max)

Converter Electrical Characteristics (Continued)

The following specifications apply for V_A = +3.0 V_{DC}, V_D = +3.0 V_{DC}, DR V_D = +3.0 V_{DC}, V_{REF} = 1.0 V_{DC}, GAIN = OF = 0V, OS = 3.0V, V_{IN} (ac coupled) = FSR = 1.0 V_{P-P}, C_L = 15 pF, f_{CLK} = 20 MHz, 50% Duty Cycle, R_S = 50Ω, t_{rc} = t_{fc} = 2 ns, NOT offset corrected. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25˚C (Note 7).

Symbol	Parameter	Conditions		Typical (Note 8)	Limits (Note 9)	Units (Limits)
DIGITAL OUTPUT CHARACTERISTICS						
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V	Parallel Mode	−7		mA
			Multiplexed Mode	−14		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = DR V_D	Parallel Mode	7		mA
			Multiplexed Mode	14		mA
POWER SUPPLY CHARACTERISTICS						
$I_A + I_D$	Core Supply Current	PD = LOW, STBY = LOW, dc input		47.6	**55**	mA(max)
		PD = LOW, STBY = HIGH		8.8		mA
		PD = HIGH, STBY = LOW or HIGH		0.22		mA
DR I_D	Digital Output Driver Supply Current (Note 10)	PD = LOW, STBY = LOW, dc input		1.3	1.4	mA(max)
		PD = LOW, STBY = HIGH		0.1		mA
		PD = HIGH, STBY = LOW or HIGH		0.1		mA
PWR	Power Consumption	PD = LOW, STBY = LOW, dc input		150	169	mW(max)
		PD = LOW, STBY = LOW, 1 MHz Input		178		mW
		PD = LOW, STBY = HIGH		27		mW
		PD = HIGH, STBY = LOW or HIGH		1		mW
PSRR1	Power Supply Rejection Ratio	Change in Full Scale with 2.7V to 3.6V Supply Change		90		dB
PSRR2	Power Supply Rejection Ratio	Rejection at output of 20 MHz, 250 mV_{P-P} Riding on V_A and V_D		52		dB

AC Electrical Characteristics OS = Low (Multiplexed Mode)

The following specifications apply for V_A = +3.0 V_{DC}, V_D = +3.0 V_{DC}, DR V_D = +3.0V_{DC}, V_{REF} = 1.0 V_{DC}, GAIN = OF = 0V, OS = 0V, V_{IN} (ac coupled) = FSR = 1.0 V_{P-P}, C_L = 15 pF, f_{CLK} = 20 MHz, 50% Duty Cycle, R_S = 50Ω, t_{rc} = t_{fc} = 2 ns, NOT offset corrected. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25˚C (Note 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
f_{CLK}[1]	Maximum Clock Frequency		30	**20**	MHz(min)
f_{CLK}[2]	Minimum Clock Frequency		1		MHz
	Duty Cycle		50	**30** **70**	%(min) %(max)
	Pipeline Delay (Latency) I Data			**2.5**	Clock Cycles
	Q Data			**3.0**	Clock Cycles
t_r, t_f	Output Rise and Fall Times		4		ns
t_{OC}	Offset Correction Pulse Width			**10**	ns(min)
t_{OD}	Output Delay from CLK Edge to Data Valid		13	**18**	ns(max)
t_{DIQ}	I/O Output Delay		17		ns
t_{DIQD}	I/Q to Data Delay	Load on I/Q pin = 30 pF	3		ns
t_{AD}	Sampling (Aperture) Delay		1		ns
t_{AJ}	Aperture Jitter		<10		ps(rms)
t_{VALID}	Data Valid Time		4.5		ns
	Overrange Recovery Time	Differential V_{IN} step from 1.5V to 0V	50		ns
t_{WUPD}	PD Low to 1/2 LSB Accurate Conversion (Wake-Up Time)		4		µs

AC Electrical Characteristics OS = Low (Multiplexed Mode) (Continued)

The following specifications apply for V_A = +3.0 V_{DC}, V_D = +3.0 V_{DC}, DR V_D = +3.0V_{DC}, V_{REF} = 1.0 V_{DC}, GAIN = OF = 0V, OS = 0V, V_{IN} (ac coupled) = FSR = 1.0 V_{P-P}, C_L = 15 pF, f_{CLK} = 20 MHz, 50% Duty Cycle, R_S = 50Ω, t_{rc} = t_{fc} = 2 ns, NOT offset corrected. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25˚C (Note 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
t_{WUSB}	STBY Low to 1/2 LSB Accurate Conversion (Wake-Up Time)		450		ns

AC Electrical Characteristics OS = High (Parallel Mode)

The following specifications apply for V_A = +3.0 V_{DC}, V_D = +3.0 V_{DC}, DR V_D = +3.0V_{DC}, V_{REF} = 1.0 V_{DC}, GAIN = OF = 0V, OS = 3.0V, V_{IN} (ac coupled) = FSR = 1.0 V_{P-P}, C_L = 15 pF, f_{CLK} = 20 MHz, 50% Duty Cycle, R_S = 50Ω, t_{rc} = t_{fc} = 2 ns, NOT offset corrected. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25˚C (Note 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
f_{CLK}[1]	Maximum Clock Frequency		30	**20**	MHz(min)
f_{CLK}[2]	Minimum Clock Frequency		1		MHz
	Duty Cycle		50	**30** **70**	%(min) %(max)
	Pipeline Delay (Latency)			**2.5**	Conv Cycles
t_r, t_f	Output Rise and Fall Times		7		ns
t_{oc}	OC Pulse Width			**10**	ns
t_{OD}	Output Delay from CLK Edge to Data Valid		15	**21**	ns(max)
t_{DIQ}	I/O Output Delay		16		ns
t_{DIQD}	I/Q to Data Delay	Load on I/Q pin = 30 pF	1		ns
t_{AD}	Sampling (Aperture) Delay		1		ns
t_{AJ}	Aperture Jitter		<10		ps(rms)
t_{VALID}	Data Valid Time		11		ns
	Overrange Recovery Time	Differential V_{IN} step from 1.5V to 0V	50		ns
t_{WUPD}	PD Low to 1/2 LSB Accurate Conversion (Wake-Up Time)		4		µs
t_{WUSB}	STBY Low to 1/2 LSB Accurate Conversion (Wake-Up Time)		450		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

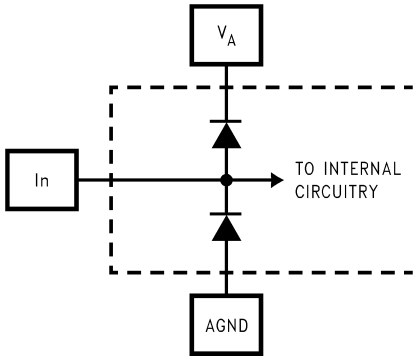
Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150˚C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max - T_A)/θ_{JA}. In the 48-pin TQFP, θ_{JA} is 76˚C/W, so P_DMAX = 1,645 mW at 25˚C and 855 mW at the maximum operating ambient temperature of 85˚C. Note that the power dissipation of this device under normal operation will typically be about 170 mW (150 mW quiescent power + 20 mW due to 1 LVTTL load on each digital output). The values for maximum power dissipation listed above will be reached only when the ADC10D020 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.

Note 6: See AN450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The inputs are protected as shown below. Input voltage magnitude up to 300 mV beyond the supply rails will not damage this device. However, errors in the A/D conversion can occur if the input goes beyond the limits given in these tables.

AC Electrical Characteristics OS = High (Parallel Mode) (Continued)



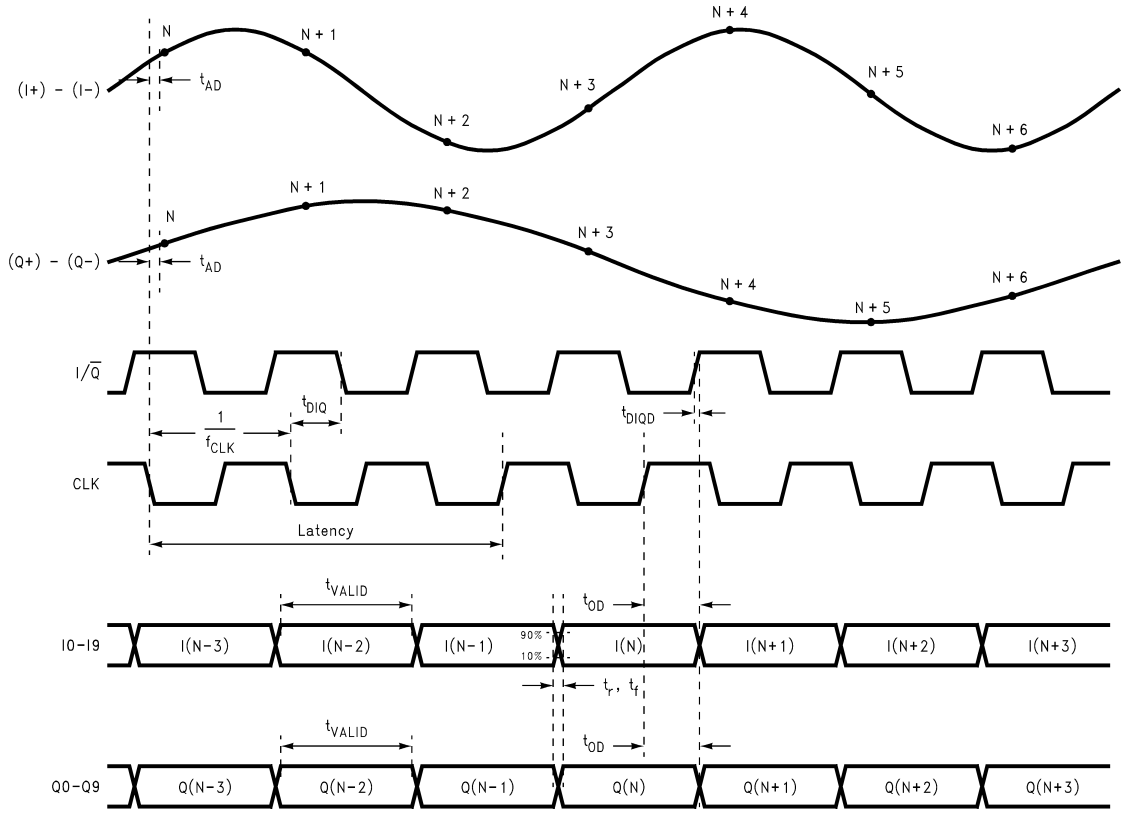
20025506

Note 8: Typical figures are at T_J = 25˚C, and represent most likely parametric norms.

Note 9: Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level). Performance is guaranteed only at V_{REF} = 1.0V and a clock duty cycle of 50%. The limits for V_{REF} and clock duty cycle specify the range over which reasonable performance is expected.

Note 10: DR I_D is the current consumed by the switching of the output drivers and is primarily determined by the load capacitance on the output pins, the supply voltage, DR V_D, and the rate at which the outputs are switching (which is signal dependent). DR I_D = DR V_D (C_O x f_O + C_1 x f_1 + ... + C_{11} x f_{11}) where DR V_D is the output driver power supply voltage, C_n is the total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.

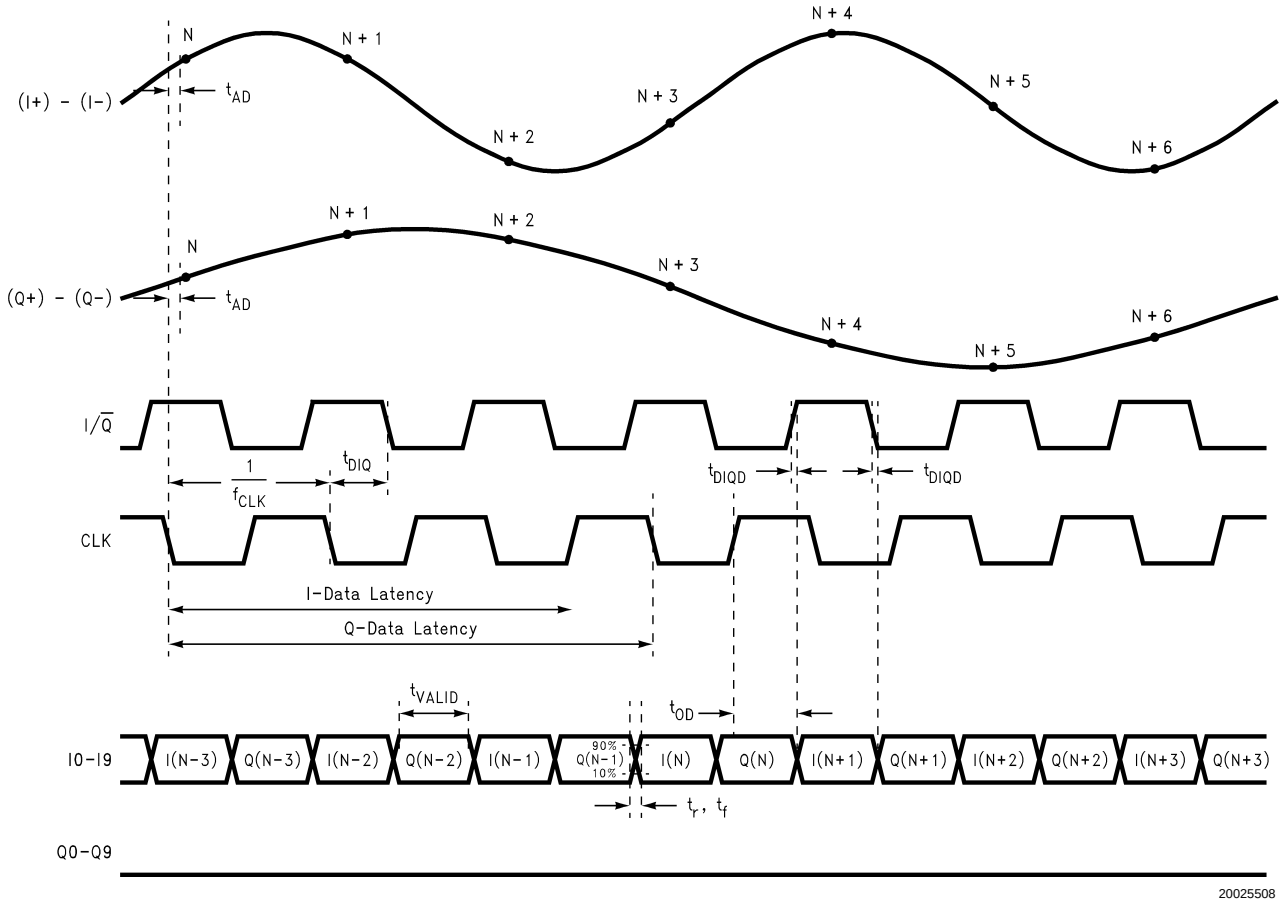
Timing Diagrams



20025507

ADC10D020 Timing Diagram for Parallel Mode

Timing Diagrams (Continued)



ADC10D020 Timing Diagram for Multiplexed Mode

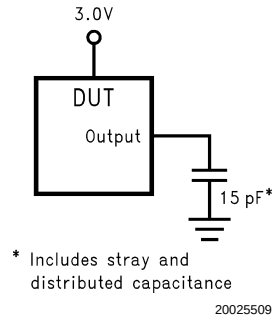


FIGURE 1. AC Test Circuit

Specification Definitions

APERTURE (SAMPLING) DELAY is that time required after the fall of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode t_{AD} after the clock goes low.

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is high to the total time of one clock period.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 20 MSPS with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD − 1.76)/6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is the frequency at which the reconstructed output fundamental drops 3 dB below its 1 MHz value for a full scale input.

GAIN ERROR is the difference between the ideal and actual differences between the input levels at which the first and last code transitions occur. That is, how far this difference is from Full Scale.

INTEGRAL NON LINEARITY (INL) is a measure of the maximum deviation of each individual code from a line drawn from zero scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. Measured at 20 MSPS with a ramp input.

INTERMODULATION DISTORTION (IMD) is the creation of spectral components that are not present in the input as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the first and second order intermodulation products to the total power in one of the original frequencies. IMD is usually expressed in dB.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value of weight of all bits. This value is

$$m * V_{REF}/2^n$$

where "m" is the reference scale factor and "n" is the ADC resolution, which is 10 in the case of the ADC10D020. The value of "m" is determined by the logic level at the gain pin and has a value of 1 when the gain pin is at a logic low and a value of 2 when the gain pin is at a logic high.

MISSING CODES are those output codes that are skipped or will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

OFFSET ERROR is a measure of how far the mid-scale transition point is from the ideal zero voltage input.

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data update is present at the output pins.

OVERRANGE RECOVERY TIME is the time required after the differential input voltages goes from 1.5V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data output lags the input by the Pipelined Delay plus the Output Delay.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in full scale gain error that results from a power supply voltage change from 2.7V to 3.6V. PSRR2 (AC PSRR) is measured with a 20 MHz, 250 mV_{P-P} signal riding upon the power supply and is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

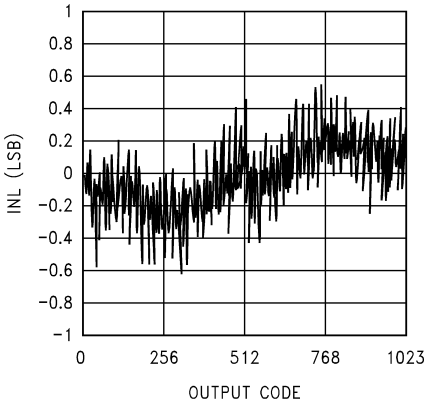
SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first six harmonic components to the rms value of the input signal at the output.

Typical Performance Characteristics

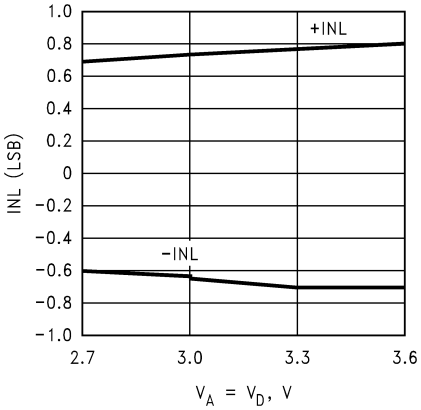
$V_A = V_D = DR\ V_D = 3.0V$, $f_{CLK} = 20$ MHz, unless otherwise specified

Typical INL



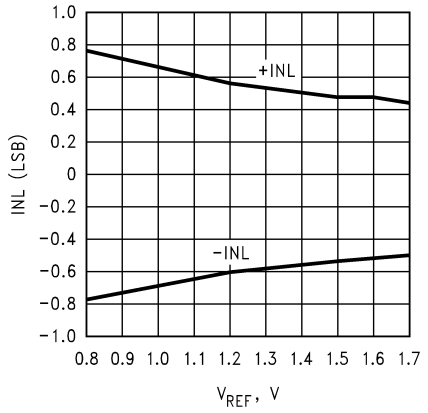
20025511

INL vs. Supply Voltage



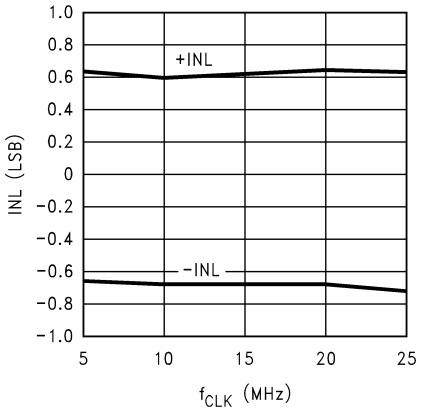
20025512

INL vs. V_{REF}



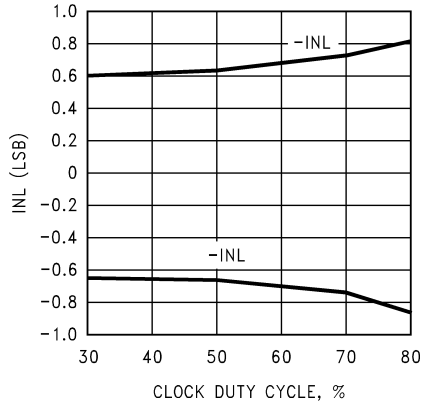
20025513

INL vs. f_{CLK}



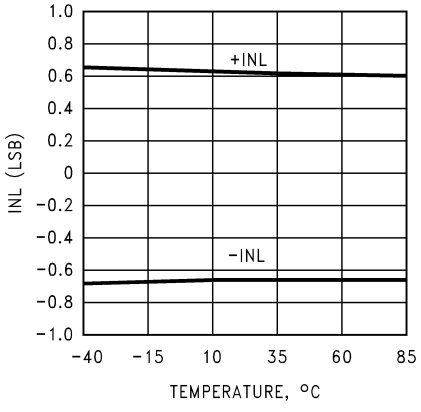
20025514

INL vs. Clock Duty Cycle



20025515

INL vs. Temperature

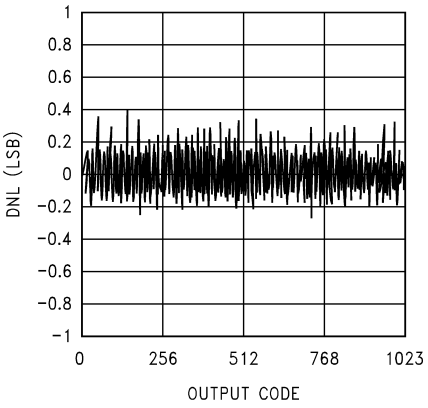


20025516

Typical Performance Characteristics

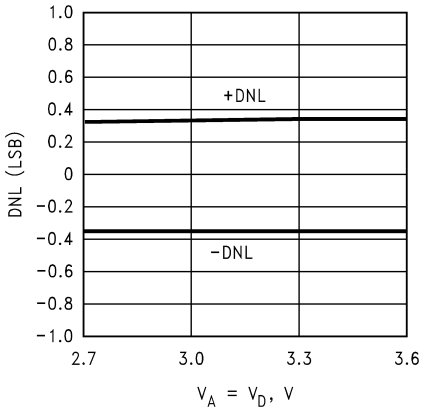
$V_A = V_D = DR\ V_D = 3.0V$, $f_{CLK} = 20$ MHz, unless otherwise specified (Continued)

Typical DNL



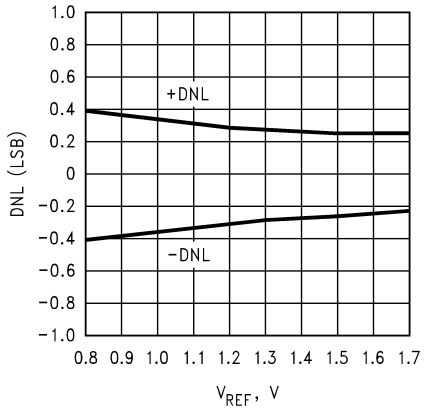
20025517

DNL vs. Supply Voltage



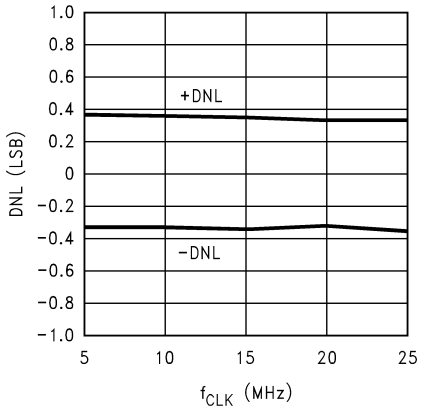
20025518

DNL vs. V_{REF}



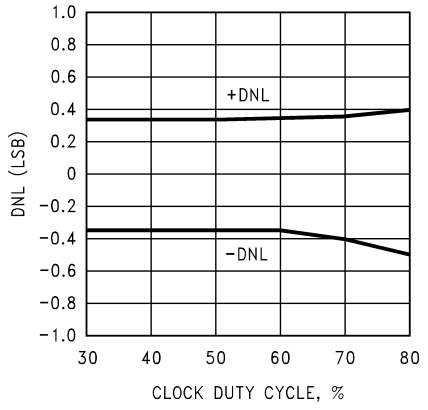
20025519

DNL vs. f_{CLK}



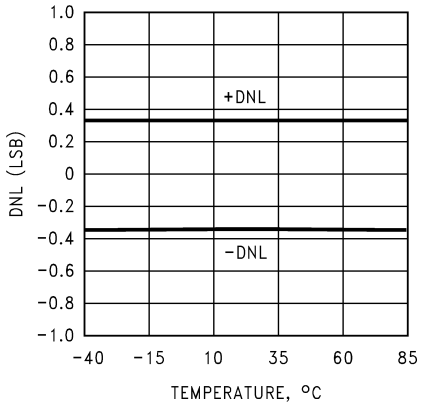
20025520

DNL vs. Clock Duty Cycle



20025521

DNL vs. Temperature

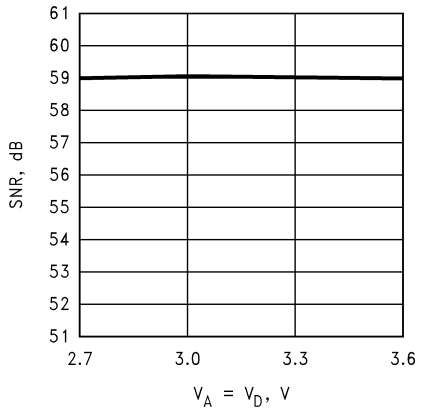


20025522

Typical Performance Characteristics

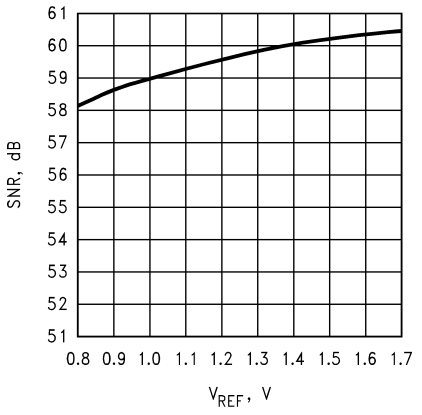
$V_A = V_D = DR\ V_D = 3.0V$, $f_{CLK} = 20$ MHz, unless otherwise specified (Continued)

SNR vs. Supply Voltage @ f_{IN} = 1 MHz to 9.5 MHz



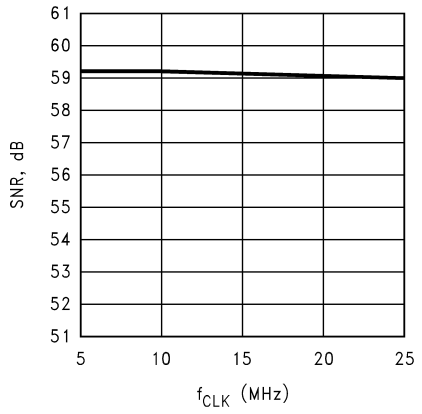
20025523

SNR vs. V_{REF} @ f_{IN} = 4.7 MHz



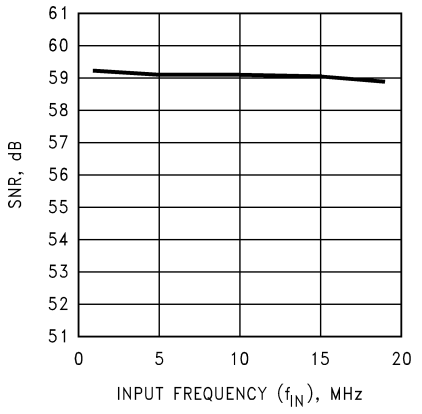
20025524

SNR vs. f_{CLK} @ f_{IN} = 9.5 MHz



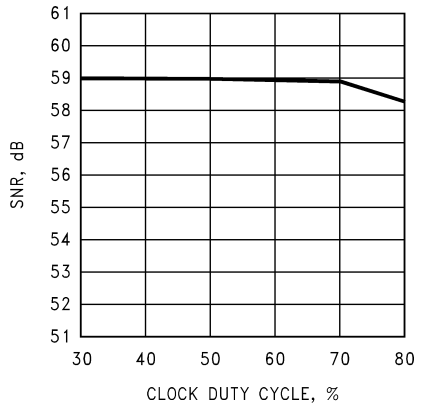
20025525

SNR vs. f_{IN}



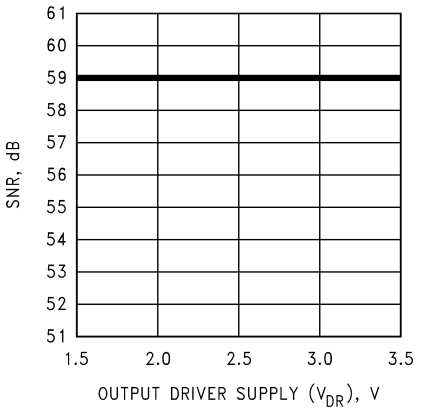
20025526

SNR vs. Clock Duty Cycle @ f_{IN} = 4.7 MHz



20025527

SNR vs. V_{DR} @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz

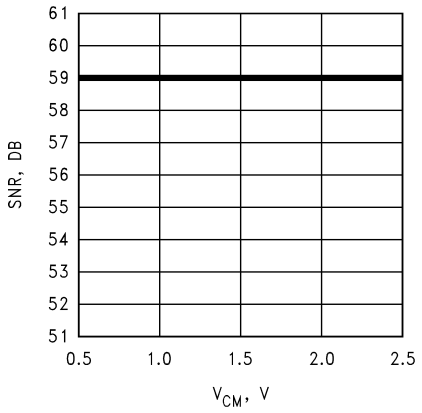


20025528

Typical Performance Characteristics

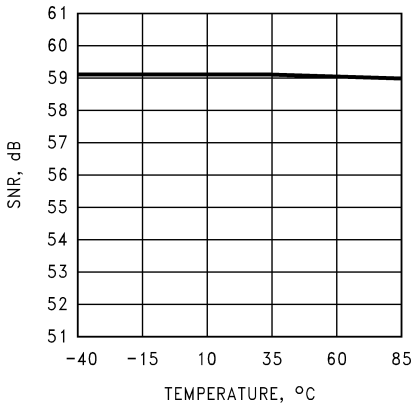
$V_A = V_D = DR\ V_D = 3.0V$, $f_{CLK} = 20$ MHz, unless otherwise specified (Continued)

SNR vs. V_{CM} @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz



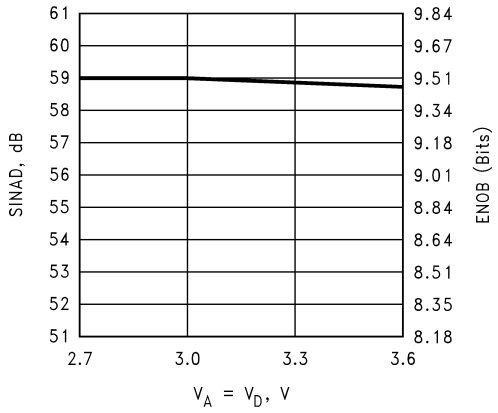
20025529

SNR vs. Temperature @ f_{IN} = 1 MHz to 9.5 MHz



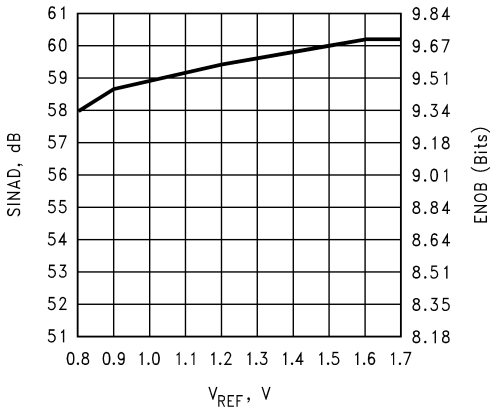
20025530

SINAD & ENOB vs. Supply Voltage @ f_{IN} = 1 MHz to 9.5 MHz



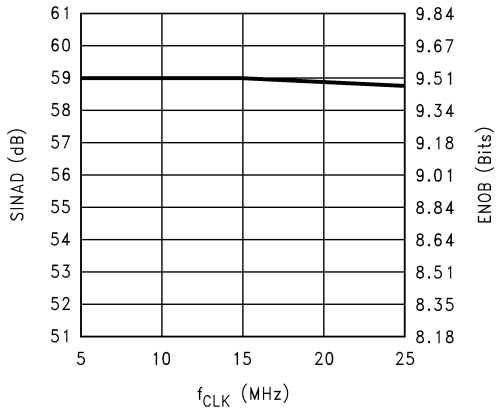
20025531

SINAD & ENOB vs. V_{REF} @ f_{IN} = 4.7 MHz



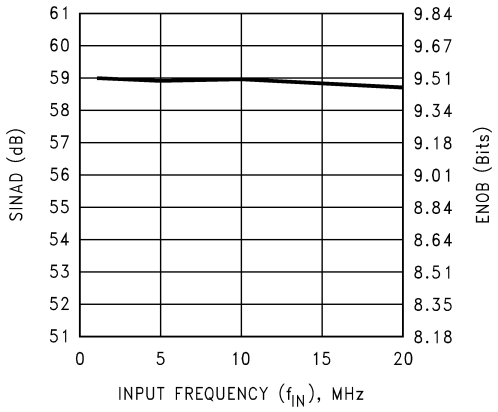
20025532

SINAD & ENOB vs. @ f_{CLK} (f_{IN} = 9.5 MHz)



20025533

SINAD & ENOB vs. f_{IN}

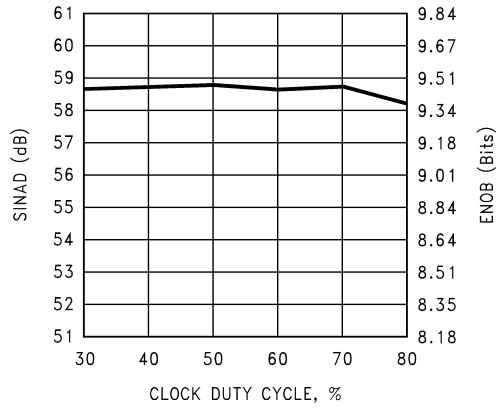


20025534

Typical Performance Characteristics

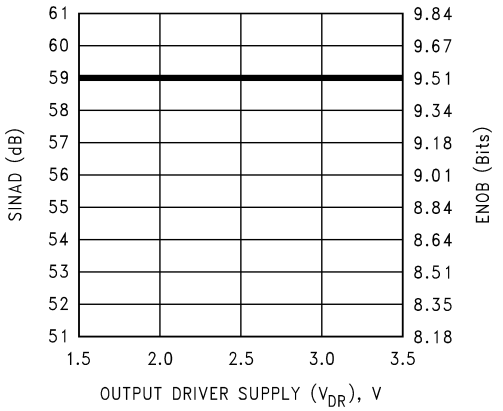
$V_A = V_D = DR\ V_D = 3.0V$, $f_{CLK} = 20$ MHz, unless otherwise specified (Continued)

SINAD & ENOB vs. Clock Duty Cycle @ f_{IN} = 4.7 MHz



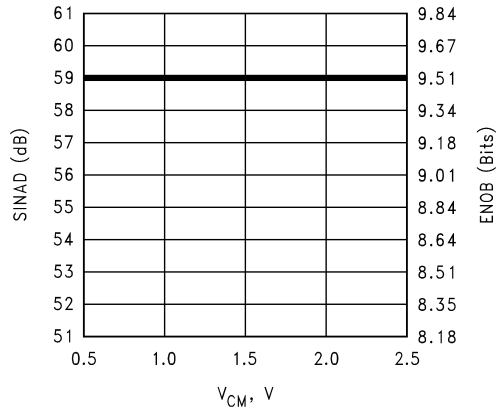
20025535

SINAD & ENOB vs. DR V_D @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz



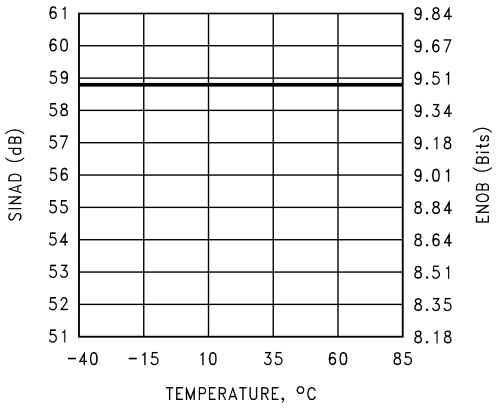
20025536

SINAD & ENOB vs. V_{CM} @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz



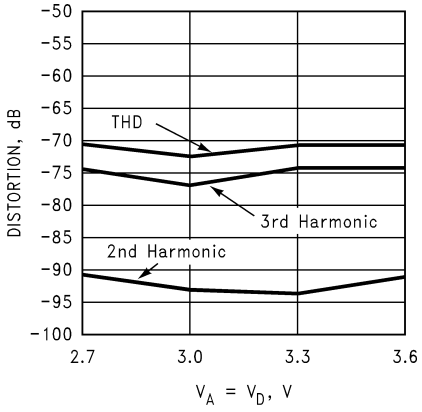
20025537

SINAD & ENOB vs. Temperature @ f_{IN} = 1 MHz to 9.5 MHz



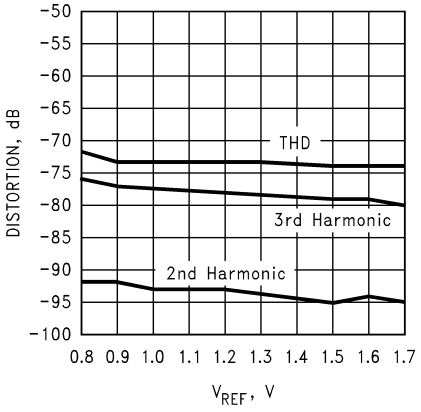
20025538

Distortion vs. Supply Voltage @ f_{IN} = 4.7 MHz



20025539

Distortion vs. V_{REF} @ f_{IN} = 4.7 MHz

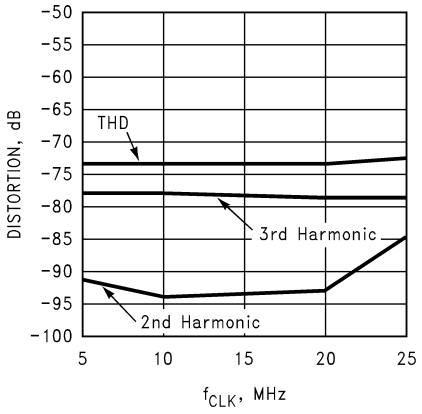


20025540

Typical Performance Characteristics

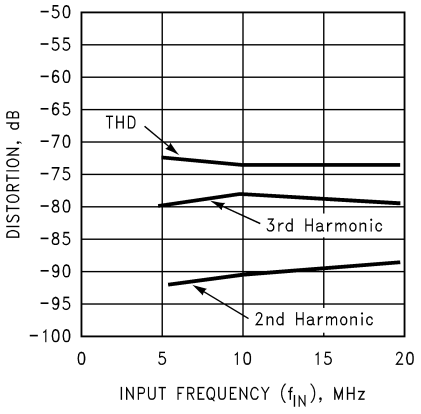
$V_A = V_D = DR\ V_D = 3.0V$, $f_{CLK} = 20$ MHz, unless otherwise specified (Continued)

Distortion vs. f_{CLK} @ f_{IN} = 9.5 MHz



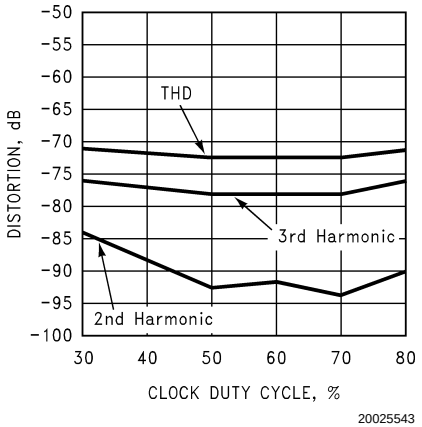
20025541

Distortion vs. f_{IN}



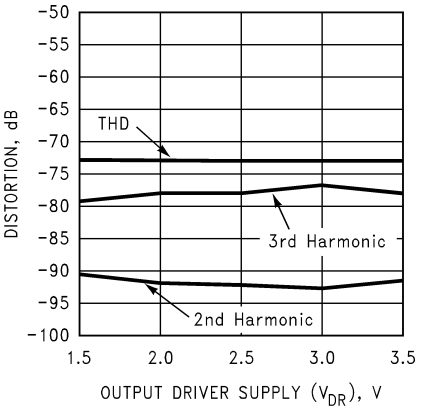
20025542

Distortion vs. Clock Duty Cycle @ f_{IN} = 4.7 MHz



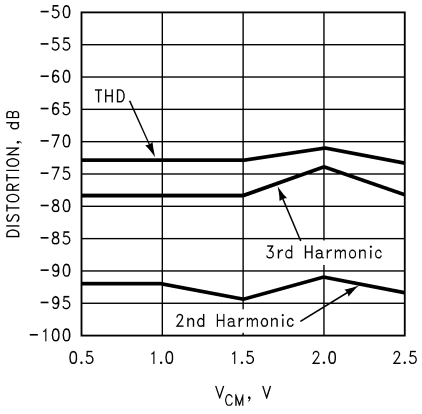
20025543

Distortion vs. DR V_D @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz



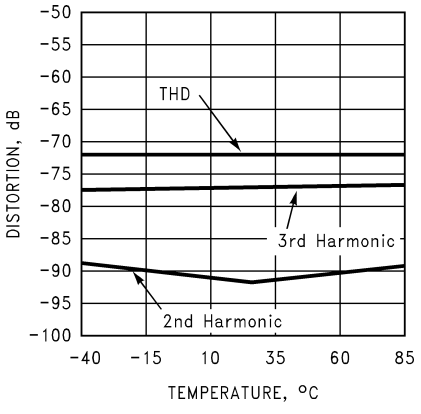
20025544

Distortion vs. V_{CM} @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz



20025545

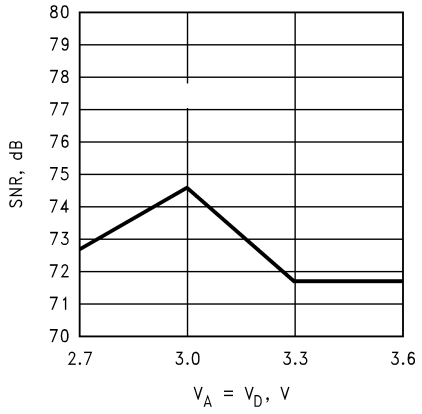
Distortion vs. Temperature



20025546

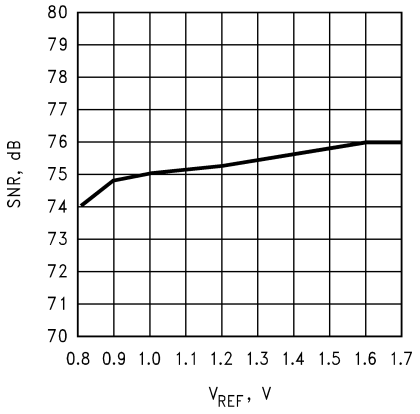
Typical Performance Characteristics $V_A = V_D = DR\ V_D = 3.0V$, $f_{CLK} = 20$ MHz, unless otherwise specified (Continued)

SFDR vs. Supply Voltage @ f_{IN} = 4.7 MHz



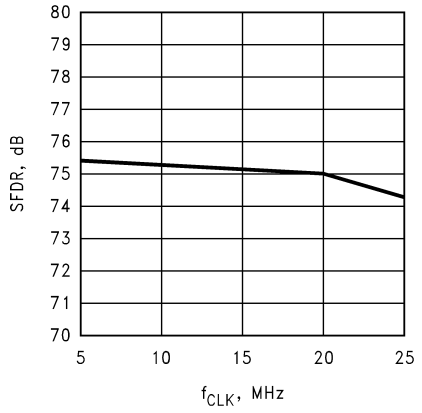
20025547

SFDR vs. V_{REF} @ f_{IN} = 4.7 MHz



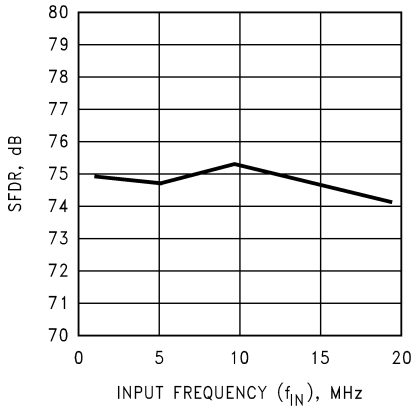
20025548

SFDR vs. f_{CLK} @ f_{IN} = 9.5 MHz



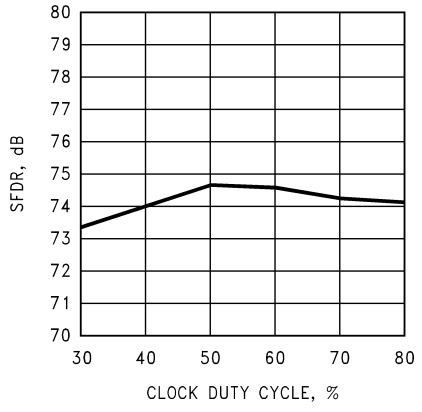
20025549

SFDR vs. f_{IN}



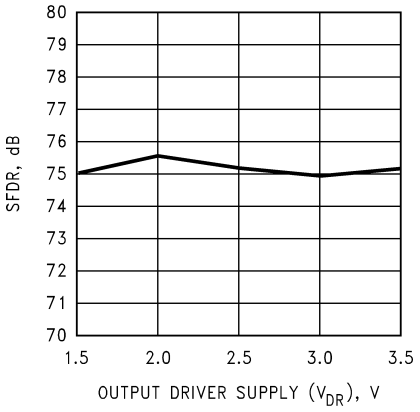
20025550

SFDR vs. Clock Duty Cycle @ f_{IN} = 4.7 MHz



20025551

SFDR vs. DR V_D @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz

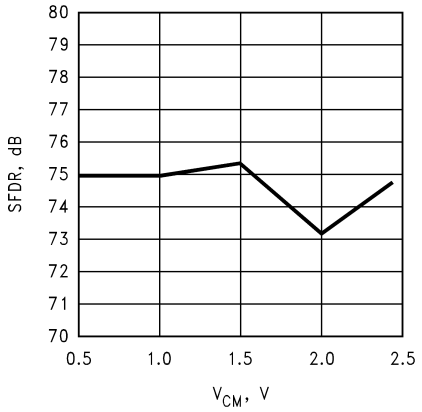


20025552

Typical Performance Characteristics

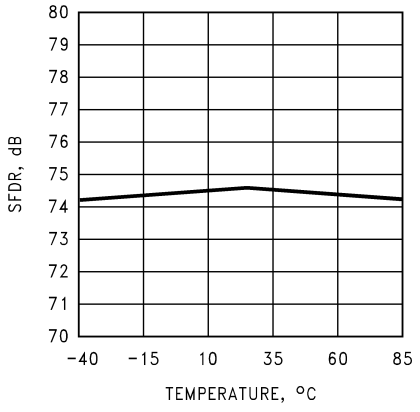
V_A = V_D = DR V_D = 3.0V, f_{CLK} = 20 MHz, unless otherwise specified (Continued)

SFDR vs. V_{CM} @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz



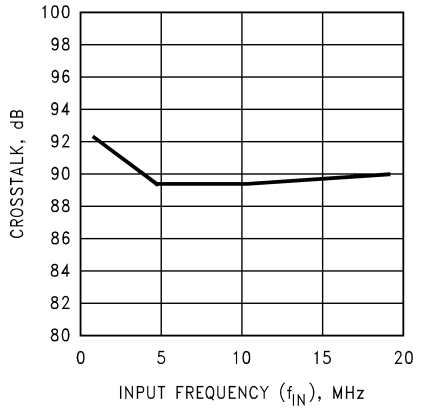
20025553

SFDR vs. Temperature @ fI_{IN} = 4.7 MHz



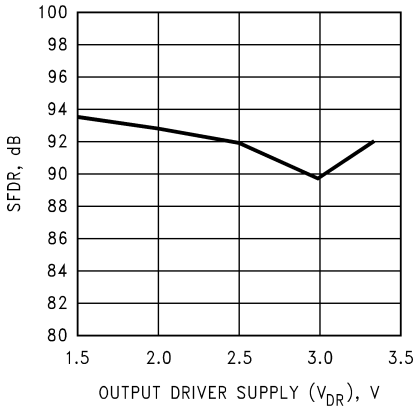
20025554

Crosstalk vs. f_{IN}



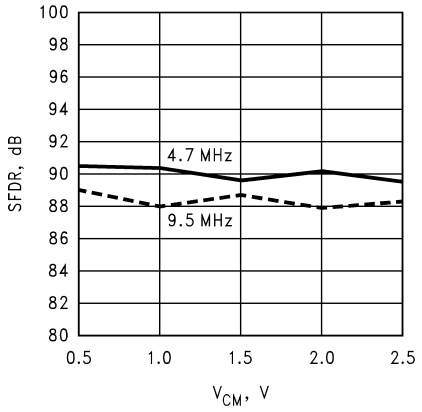
20025555

Crosstalk vs. V_{DR} @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz



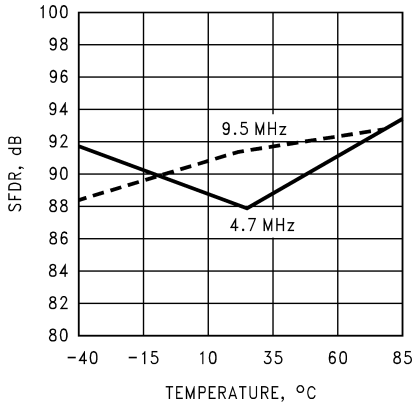
20025556

Crosstalk vs. V_{CM} @ fI_{IN} = 4.7 MHz, fQ_{IN} = 9.5 MHz



20025557

Crosstalk vs. Temperature

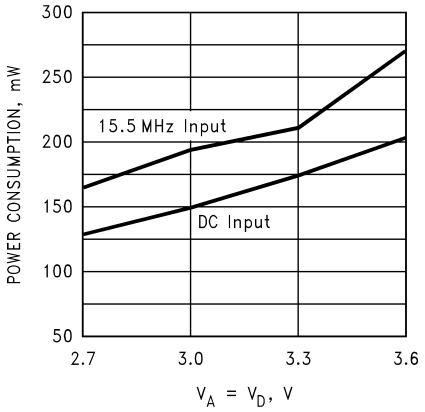


20025558

Typical Performance Characteristics

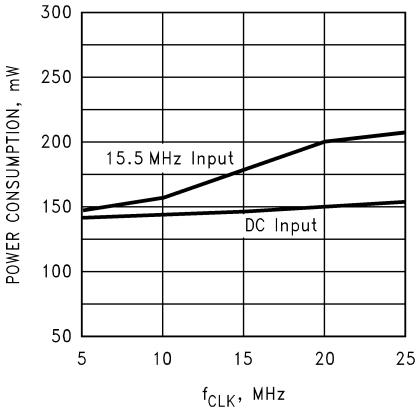
$V_A = V_D = DR\ V_D = 3.0V$, $f_{CLK} = 20$ MHz, unless otherwise specified (Continued)

Power Consumption vs. Supply Voltage



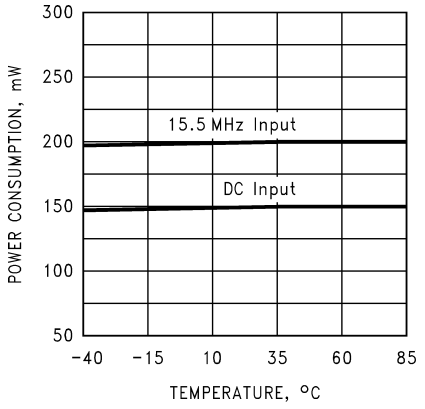
20025559

Power Consumption vs. f_{CLK}



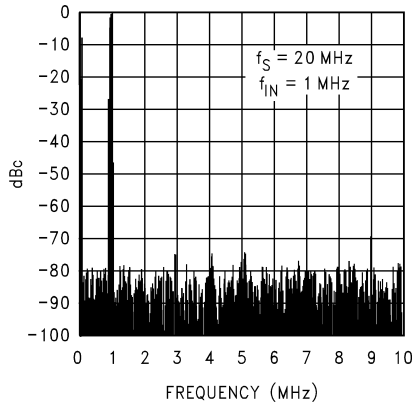
20025560

Power Consumption vs. Temperature



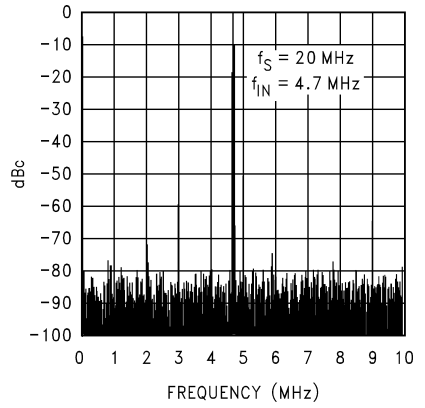
20025561

Spectral Response @ f_{IN} = 1 MHz



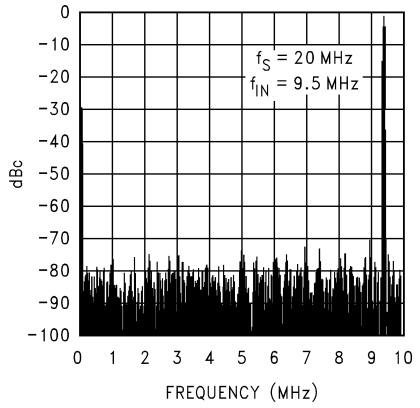
20025562

Spectral Response @ f_{IN} = 4.7 MHz



20025563

Spectral Response @ f_{IN} = 9.5 MHz

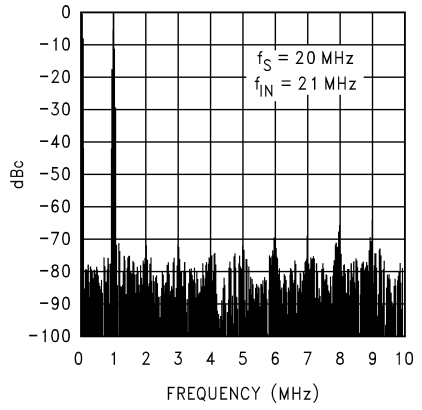


20025564

Typical Performance Characteristics

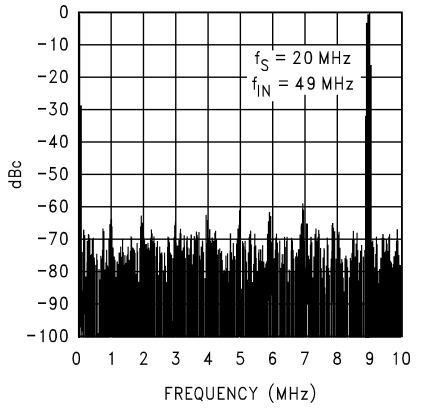
$V_A = V_D = DR\ V_D = 3.0V$, $f_{CLK} = 20$ MHz, unless otherwise specified (Continued)

Spectral Response @ f_{IN} = 21 MHz



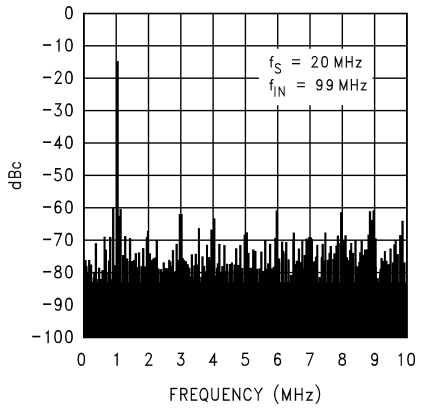
20025565

Spectral Response @ f_{IN} = 49 MHz



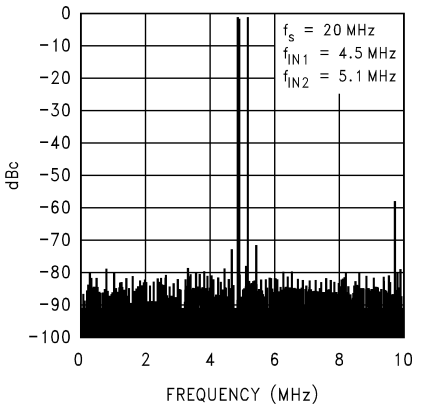
20025566

Spectral Response @ f_{IN} = 99 MHz



20025581

IMD Response @ f_{IN} = 4.9 MHz, 5.1 MHz



20025568

Functional Description

The ADC10D020 uses an internal sample-and-hold amplifier (SHA) to enable sustained dynamic performance for signals of input frequency beyond the clock rate. This SHA also lowers the converter's input capacitance and reduces the number of external components required.

Using a subranging architecture, the ADC10D020 achieves 9.5 effective bits over the entire Nyquist band at 20 MSPS while consuming just 150 mW. The use of an internal sample-and-hold amplifier (SHA) not only enables this sustained dynamic performance, but also lowers the converter's input capacitance and reduces the number of external components required.

Analog signals at the "I" and "Q" inputs that are within the voltage range set by V_{REF} and the GAIN pin are digitized to ten bits at up to 30 MSPS. V_{REF} has a range of 0.8V to 1.5V, providing a differential peak-to-peak input range of 0.8 V_{P-P} to 1.5 V_{P-P} with the GAIN pin at a logic low, or an input range of 1.6 V_{P-P} to 3.0 V_{P-P} with the GAIN pin at a logic high. Differential input voltages less than $-V_{REF}/2$ with the GAIN pin low, or less than $-V_{REF}$ with the GAIN pin high will cause the output word to indicate a negative full scale. Differential input voltages greater than $V_{REF}/2$ with the GAIN pin low, or greater than V_{REF} with the GAIN pin high, will cause the output word to indicate a positive full scale.

Both "I" and "Q" channels are sampled simultaneously on the falling edge of the clock input, while the timing of the data output depends upon the mode of operation.

In the parallel mode, the "I" and "Q" output busses contain the conversion result for their respective inputs. The "I" and "Q" channel data are present and valid at the data output pins t_{OD} after the rising edge of the input clock. In the multiplexed mode, "I" channel data is available at the digital outputs t_{OD} after the rise of the clock edge, while the "Q" channel data is available at the digital outputs t_{OD} after the fall of the clock.

Data latency in the parallel mode is 2.5 clock cycles. In the multiplexed mode data latency is 2.5 clock cycles for the "I" channel and 3.0 clock cycles for the "Q" channel. The ADC10D020 will convert as long as the clock signal is present and the PD and STBY pins are low.

Throughout this discussion, V_{CM} refers to the Common Mode input voltage of the ADC10D020 while V_{CMO} refers to its Common Mode output voltage.

Applications Information

1.0 THE ANALOG INPUTS

Each of the analog inputs of the ADC10D020 consists of a switch (transmission gate) followed by a switched capacitor amplifier. The capacitance seen at each input pin changes

Applications Information (Continued)

with the clock level, appearing as about 3 pF when the clock is low, and about 5 pF when the clock is high. A switched capacitance is harder to drive that is a larger, fixed capacitance.

The CLC409 and the CLC428 dual op amp have been found to be a good amplifiers to drive the ADC10D020 because of their wide bandwidth and low distortion. They also have good Differential Gain and Differential Phase performance.

Care should be taken to avoid driving the input beyond the supply rails, even momentarily, as during power-up.

The ADC10D020 is designed for differential input signals for best performance. With a 1.0V reference and the GAIN pin at a logic low, differential input signals up to 1.0 V_{P-P} are digitized. See *Figure 2*. For differential signals, the input common mode is expected to be about 1.5V, but the inputs are not sensitive to the common-mode voltage and can be anywhere within the supply rails (ground to V_A) with little or no performance degradation, as long as the signal swing at the individual input pins is no more than 300 mV beyond the supply rails. For single ended drive, operate the ADC10D020 with the GAIN pin at a logic low, connect one pin of the input pair to 1.5V (V_{CM}) and drive the other pin of the input pair with 1.0 V_{P-P} centered around 1.5V.

Because of the larger signal swing at one input for single-ended operation, distortion performance will not be as good as with a differential input signal. Alternatively, single-ended to differential conversion with a transformer provides a quick, easy solution for those applications not requiring response to dc and low frequencies. See *Figure 3*. The 330Ω resistors and 10 pF capacitor values are chosen to provide a cutoff frequency near the clock frequency to compensate for the effects of input sampling.

2.0 REFERENCE INPUTS

The V_{RP} and V_{RN} pins should each be bypassed with a 5 µF (or larger) tantalum or electrolytic capacitor and a 0.1 µF ceramic capacitor. Use these pins only for bypassing. DO NOT connect anything else to these pins.

Figure 4 shows a simple reference biasing scheme with minimal components. While this circuit will suffice for many applications, the value of the reference voltage will depend upon the supply voltage.

The circuit of *Figure 5* is an improvement over the circuit of *Figure 4* because the reference voltage is independent of supply voltage. This reduces problems of reference voltage variability. The reference voltage at the V_{REF} pin should be bypassed to AGND with a 5 µF (or larger) tantalum or electrolytic capacitor and a 0.1 µF ceramic capacitor.

The circuit of *Figure 6* may be used if it is desired to obtain a precise reference voltage not available with a fixed reference. The 240Ω and 1k resistors can be replaced with a potentiometer, if desired.

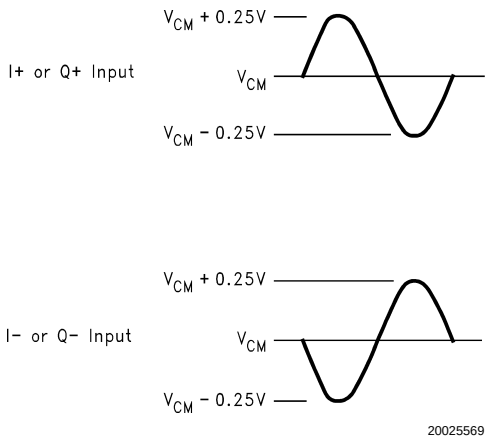


FIGURE 2. The ADC10D020 is designed for use with differential signals of 1.0 V_{P-P} with a common mode voltage of 1.5V. The signal swing should not cause any pin to experience a swing more than 300 mV beyond the supply rails.

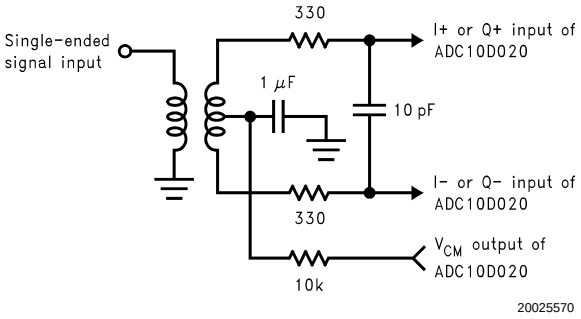


FIGURE 3. Use of an input transformer for single-ended to differential conversion can simplify circuit design for single-ended signals.

Applications Information (Continued)

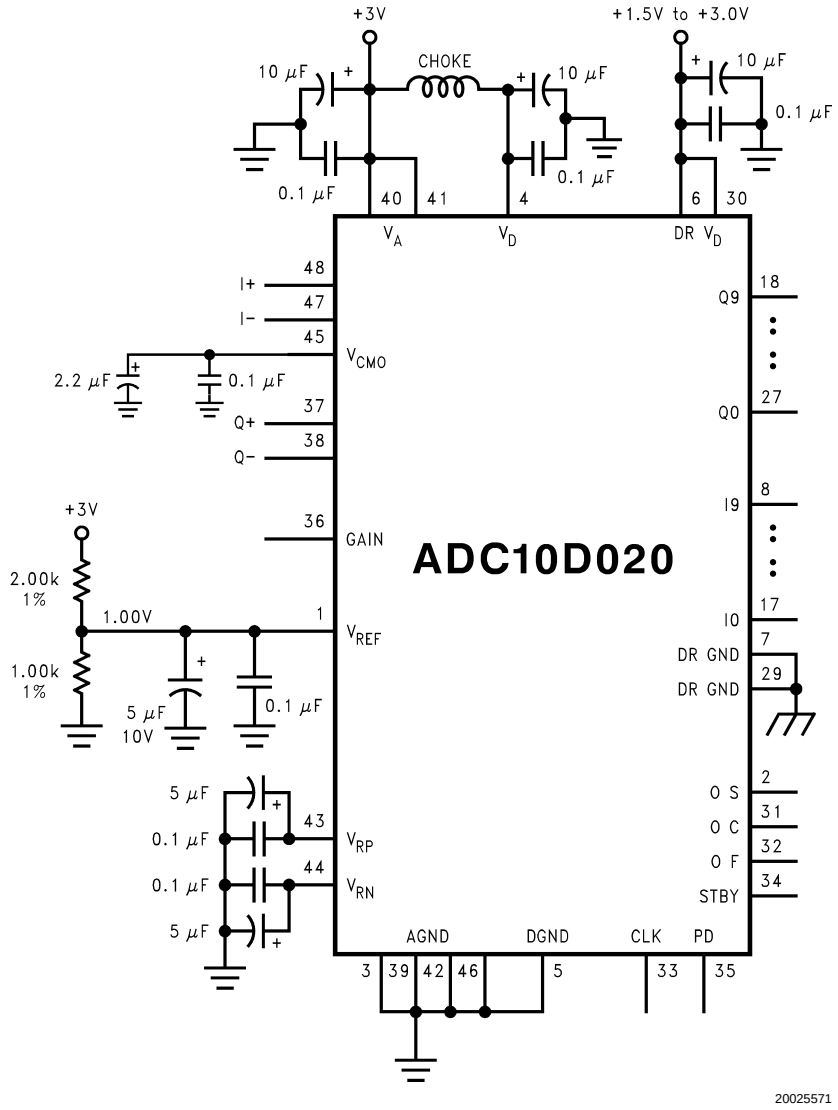


FIGURE 4. Simple Reference Biasing

Applications Information (Continued)

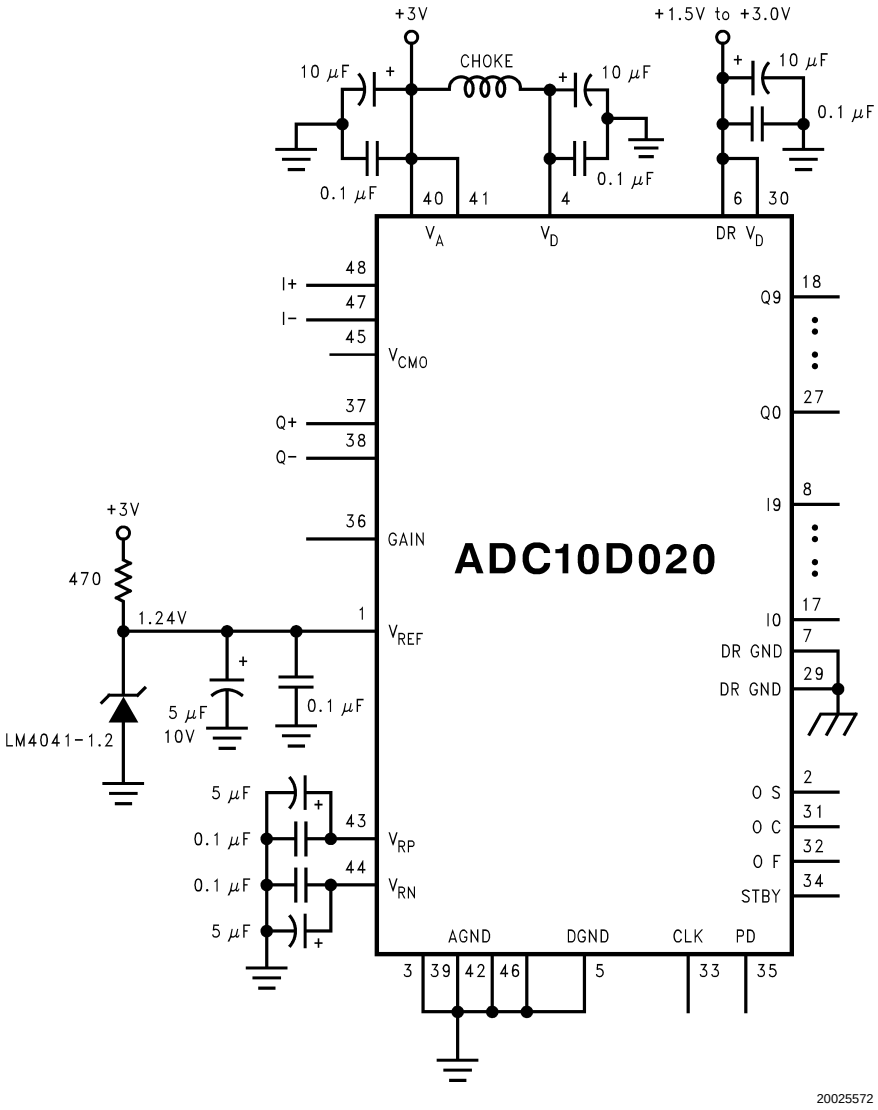


FIGURE 5. Improved Low Component Count Reference Biasing

The V_{CMO} output can be used as the ADC reference source as long as care is taken to prevent excessive loading of this pin. Since the reference input of the ADC10D020 is buffered, there is virtually no loading on the V_{CMO} output by the V_{REF} pin. While the ADC10D040 will work with a 1.5V reference voltage, it is fully specified for a 1.0V reference. To use the V_{CMO} for a reference voltage at 1.0V, the 1.5V V_{CMO} output may need to be divided down. The divider resistor values need to be carefully chosen to prevent excessive V_{CMO} loading. See *Figure 7*. While the average temperature coefficient of V_{CMO} is 20 ppm/˚C, that temperature coefficient can be broken down to a typical 50 ppm/˚C between −40˚C and +25˚C and a typical −12 ppm/˚C between +25˚C and +85˚C.

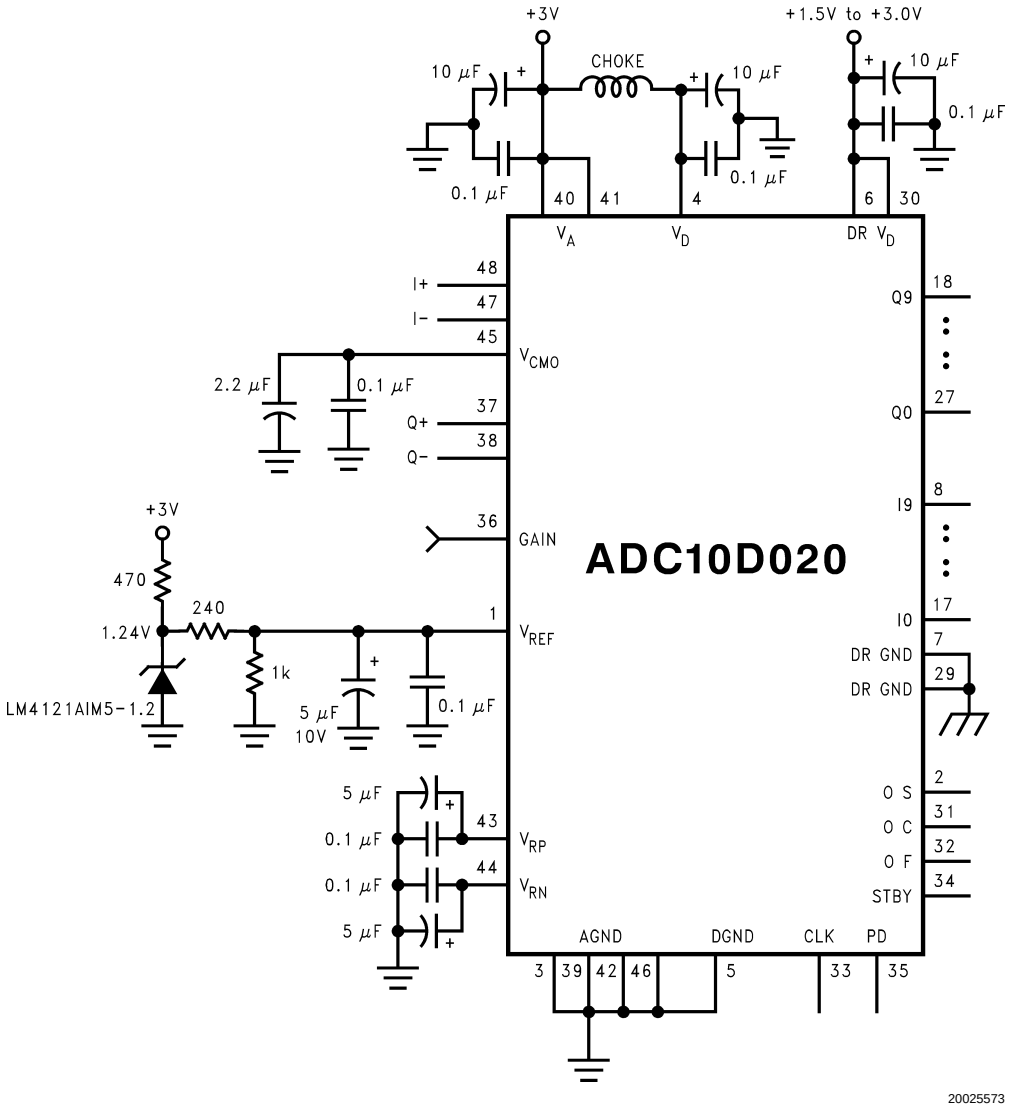


FIGURE 6. Setting An Accurate Reference Voltage

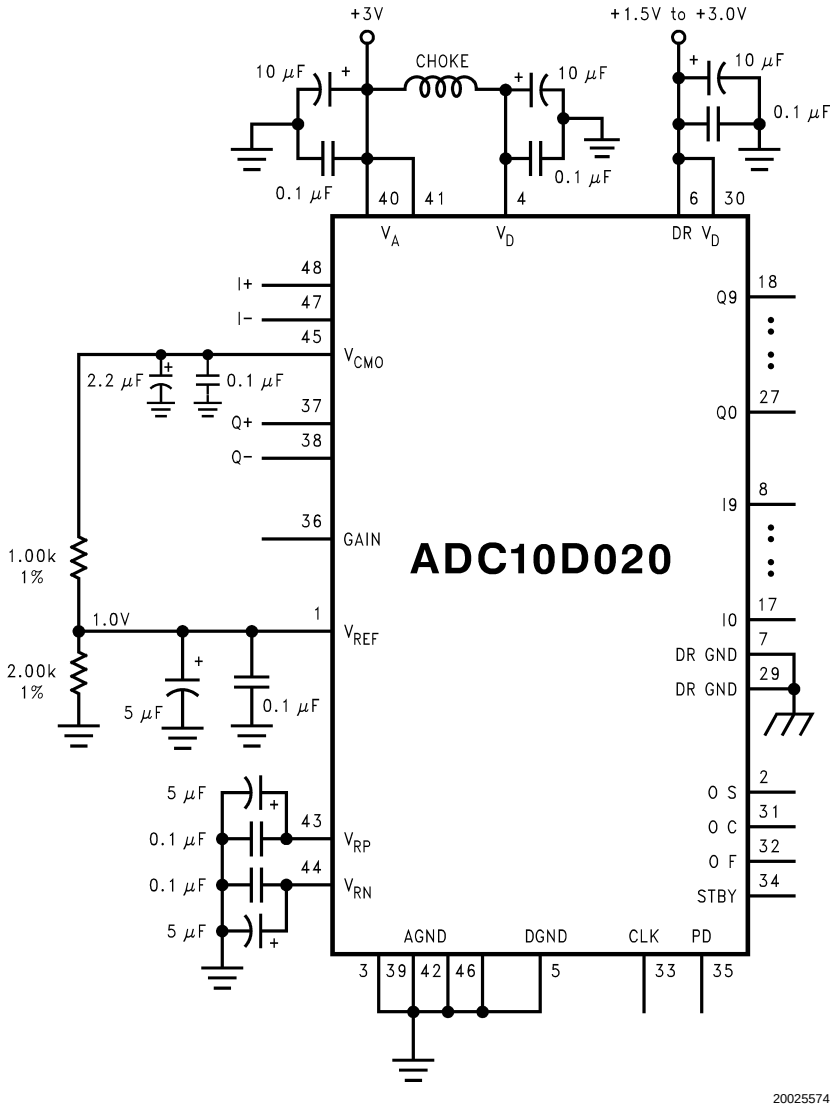


FIGURE 7. The V_{CMO} output pin may be used as an internal reference source if its output is divided down and not loaded excessively.

2.1 REFERENCE VOLTAGE

The reference voltage should be within the range specified in the Operating Ratings table (0.8V to 1.5V). A reference voltage that is too low could result in a noise performance that is less than desired because the quantization level falls below other noise sources. On the other hand, a reference voltage that is too high means that an input signal that produces a full scale output uses such a large input range that the input stage is less linear, resulting in a degradation of distortion performance. Also, for large reference voltages, the internal ladder buffer runs out of head-room, leading to a reduction of gain in that buffer and causing gain error.

The Reference bypass pins V_{RP} and V_{RN} are output compensated and should each be bypassed with a parallel combination of a 5 µF (minimum) and 0.1 µF capacitors.

As mentioned in the previous section, the V_{CMO} output can be used as the ADC reference.

2.2 V_{CMO} OUTPUT

The V_{CMO} output pin is intended to provide a common mode bias for the differential input pins of the ADC10D020. It can also be used as a voltage reference source. Care should be taken, however, to avoid loading this pin with more than 1 mA. A load greater than this could result in degraded long term and temperature stability of this voltage. The V_{CMO} pin is output compensated and should be bypassed with a 2 µF/0.1 µF combination, minimum. See *2.0 REFERENCE INPUTS* for more information on using the V_{CMO} output as a reference source.

3.0 DIGITAL INPUT PINS

The seven digital input pins are used to control the function of the ADC10D020.

Applications Information (Continued)

3.1 CLOCK (CLK) INPUT

The clock (CLK) input is common to both A/D converters. This pin is CMOS/LVTTL compatible with a threshold of about $V_A/2$. Although the ADC10D020 is tested and its performance is guaranteed with a 20 MHz clock, it typically will function well with low-jitter clock frequencies from 1 MHz to 30 MHz. The clock source should be series terminated and the ADC clock pin should be shunt terminated with a 100Ω resistor in series with a capacitor whose impedance is 60Ω to 90Ω at the fundamental of the clock frequency. The rise and fall times of the clock supplied to the ADC clock pin should be no more than 2 ns. The analog inputs I = (I+) – (I−) and Q = (Q+) – (Q−) are simultaneously sampled on the falling edge of this input to ensure the best possible aperture delay match between the two channels.

3.2 OUTPUT BUS SELECT (OS) PIN

The Output Bus Select (OS) pin determines whether the ADC10D020 is in the parallel or multiplexed mode of operation. A logic high at this pin puts the device into the parallel mode of operation where "I" and "Q" data appear at their respective output buses. A logic low at this pin puts the device into the multiplexed mode of operation where the "I" and "Q" data are multiplexed onto the "I" output bus and the "Q" output lines all remain at a logic low.

3.3 OFFSET CORRECT (OC) PIN

The Offset Correct (OC) pin is used to initiate an offset correction sequence. This procedure should be done after power up and need not be performed again unless power to the ADC10D020 is interrupted. An independent offset correction sequence for each converter is initiated when there is a low-to-high transition at the OC pin. This sequence takes 34 clock cycles to complete, during which time 32 conversions are taken and averaged. The result is subtracted from subsequent conversions. Because the offset correction is performed digitally at the output of the ADC, the output range of the ADC is reduced by the offset amount.

Each input pair should have a 0V differential voltage value during this entire 34 clock period, but the "I" and "Q" input voltages do not have to be equal to each other. Because of the uncertainty as to exactly when the conversion sequence starts, it is best to allow 35 clock periods for this sequence.

3.4 OUTPUT FORMAT (OF) PIN

The Output Format (OF) pin provides a choice of straight binary or 2's complement output formatting. With this pin at a logic low, the output format is straight binary. With this pin at a logic high, the output format is 2's complement.

3.5 STANDBY (STBY) PIN

The Standby (STBY) pin may be used to put the ADC10D020 into a low power mode where it consumes just 27 mW and can quickly be brought to full operation. The device operates normally with a logic low on this and the PD pins.

3.6 POWER DOWN (PD) PIN

The Power Down (PD) pin puts the device into a low-power "sleep" state where it consumes just 1 mW when at a logic high. Power consumption is reduced more when the PD pin is high than when the STBY pin is high, but recovery to full operation is much quicker from the standby state than it is from the power down state. When the STBY and PD pins are both high, the ADC10D020 is in the power down mode.

3.7 GAIN PIN

The GAIN pin sets the internal signal gain of the "I" and "Q" inputs. With this pin at a logic low, the full scale differential peak-to-peak input signal is equal to V_{REF}. With the GAIN pin at a logic high, the full scale differential peak-to-peak input signal is equal to 2 times V_{REF}.

4.0 INPUT/OUTPUT RELATIONSHIP ALTERNATIVES

The GAIN pin of the ADC10D020 offers input range selection, while the OF pin offers a choice of straight binary or 2's complement output formatting.

The relationship between the GAIN, OF, analog inputs and the output code are as defined in *Table 1*. Keep in mind that the input signals must not exceed the power supply rails.

TABLE 1. ADC10D020 Input/Output Relationships

GAIN	OF	I+/Q+	I−/Q−	Output Code
0	0	$V_{CM} + 0.25*V_{REF}$	$V_{CM} - 0.25*V_{REF}$	11 1111 1111
0	0	V_{CM}	V_{CM}	10 0000 0000
0	0	$V_{CM} + 0.25*V_{REF}$	$V_{CM} - 0.25*V_{REF}$	00 0000 0000
0	1	$V_{CM} + 0.25*V_{REF}$	$V_{CM} - 0.25*V_{REF}$	01 1111 1111
0	1	V_{CM}	V_{CM}	00 0000 0000
0	1	$V_{CM} + 0.25*V_{REF}$	$V_{CM} - 0.25*V_{REF}$	10 0000 0000
1	0	$V_{CM} + 0.5*V_{REF}$	$V_{CM} - 0.5*V_{REF}$	11 1111 1111
1	0	V_{CM}	V_{CM}	10 0000 0000
1	0	$V_{CM} + 0.5*V_{REF}$	$V_{CM} - 0.5*V_{REF}$	00 0000 0000
1	1	$V_{CM} + 0.5*V_{REF}$	$V_{CM} - 0.5*V_{REF}$	01 1111 1111
1	1	V_{CM}	V_{CM}	00 0000 0000
1	1	$V_{CM} + 0.5*V_{REF}$	$V_{CM} - 0.5*V_{REF}$	10 0000 0000

Applications Information (Continued)

5.0 POWER SUPPLY CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10 µF to 50 µF tantalum or aluminum electrolytic capacitor should be placed within half an inch (1.2 centimeters) of the A/D power pins, with a 0.1 µF ceramic chip capacitor placed as close as possible to each of the converter's power supply pins. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source should be used for the analog and digital supplies of the ADC10D020, these supply pins should be well isolated from each other to prevent any digital noise from being coupled to the analog power pins. A choke is recommended between the V_A and V_D supply lines. A choke should also be used between V_A and DR V_D when the same supply source is used for both V_A and DR V_D. Be sure to bypass DR V_D.

The DR V_D pins are completely isolated from the other supply pins. Because of this isolation, a separate supply can be used for these pins. This DR V_D supply can be significantly lower than the three volts used for the other supplies, easing the interface to lower voltage digital systems. Using a lower voltage for this supply can also reduce the power consumption and noise associated with the output drivers.

The converter digital supply should **not** be the supply that is used for other digital circuitry on the board. It should be the same supply used for the ADC10D020 analog supply.

As is the case with all high speed converters, the ADC10D020 should be assumed to have little high frequency power supply rejection. A clean analog power source should be used.

No pin should ever have a voltage on it that is more than 300 mV in excess of the supply voltages or below ground, not even on a transient basis. This can be a problem upon application of power to a circuit and upon turn off of the power source. Be sure that the supplies to circuits driving the CLK, or any other digital or analog inputs do not come up any faster than does the voltage at the ADC10D020 power pins.

6.0 LAYOUT AND GROUNDING

Proper routing of all signals and proper ground techniques are essential to ensure accurate conversion. Separate analog and digital ground planes may be used if adequate care is taken with signal routing, but may result in EMI/RFI. A single ground plane with proper component placement will yield good results while minimizing EMI/RFI.

Analog and digital ground current paths should not coincide with each other as the common impedance will cause digital noise to be added to analog signals. Accordingly, traces carrying digital signals should be kept as far away from traces carrying analog signals as is possible. Power should be routed with traces rather than the use of a power plane. The analog and digital power traces should be kept well away from each other. All power to the ADC10D020 should be considered analog. The DR GND pin should be considered a digital ground and not be connected to the ground plane in close proximity with the other ground pins of the ADC10D020.

Each bypass capacitor should be located as close to the appropriate converter pin as possible and connected to the pin and the appropriate ground plane with short traces. The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground return.

The clock line should be properly terminated, as discussed in Section 3.1, and be as short as possible.

Figure 8 gives an example of a suitable layout and bypass capacitor placement. All analog circuitry (input amplifiers, filters, reference components, etc.) and interconnections should be placed in an area reserved for analog circuitry. All digital circuitry and I/O lines should be placed in an area reserved for digital circuitry. Violating these rules can result in digital noise getting into the analog circuitry, which will degrade accuracy and dynamic performance (THD, SNR, SINAD).

Applications Information (Continued)

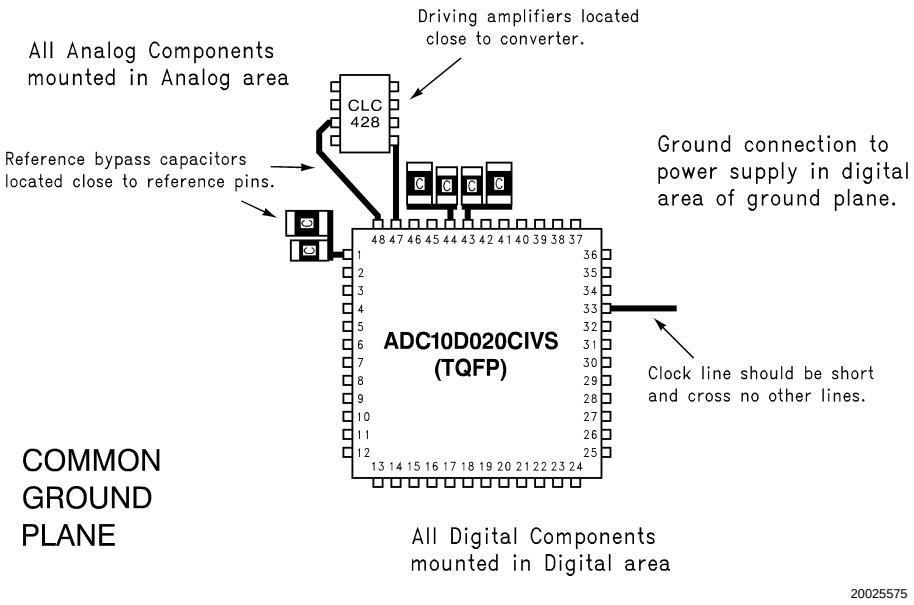


FIGURE 8. An Acceptable Layout Pattern

Applications Information (Continued)

7.0 DYNAMIC PERFORMANCE

The ADC10D020 is ac tested and its dynamic performance is guaranteed. To meet the published specifications, the clock source driving the CLK input must be free of jitter. For best dynamic performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See *Figure 9*.

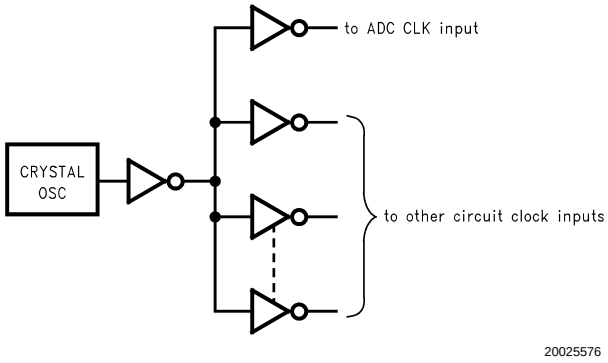


FIGURE 9. Isolating the ADC Clock from Digital Circuitry

8.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, no input should not go more than 300 mV beyond the supply pins. Exceeding these limits on even a transient basis can cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes a few hundred millivolts below ground. A resistor of 50Ω to 100Ω in series with the offending digital input, close to the source, will usually eliminate the problem.

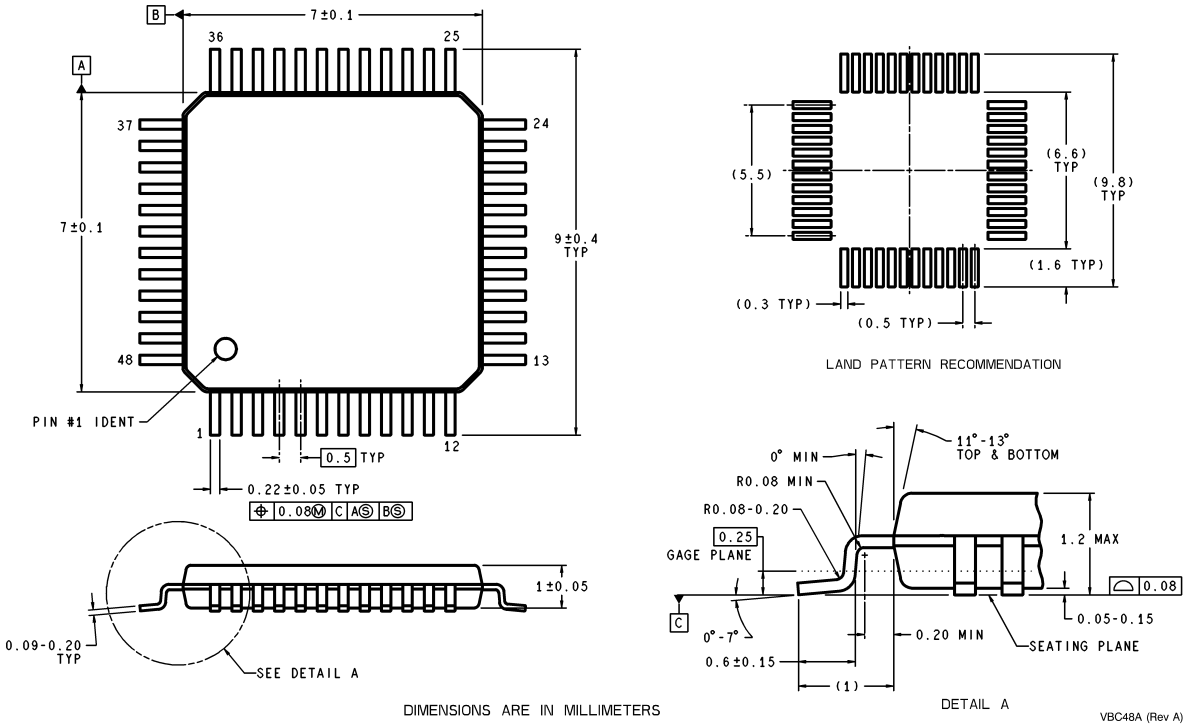
Care should be taken not to overdrive the inputs of the ADC10D020 (or any device) with a device that is powered from supplies outside the range of the ADC10D020 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers has to charge for each conversion, the more instantaneous digital current is required from DR V_D and DR GND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Adequate bypassing and attention to board layout will reduce this problem. Buffering the digital data outputs (with a 74ACTQ821, for example) may be necessary if the data bus to be driven is heavily loaded. Dynamic performance can also be improved by adding series resistors of 47Ω to 56Ω at each digital output, close to the ADC output pins.

Using a clock source with excessive jitter. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance. The use of simple gates with RC timing as a clock source is generally inadequate.

Using the same voltage source for V_D and digital logic. As mentioned in Section 5.0, V_D should use the same power source used by V_A and other analog components, but should be decoupled from V_A.

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead TQFP Package
Ordering Number ADC10D020CIVS
NS Package Number VBA48A

NOTES UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH
   7.62 MICROMETERS MINIMUM SOLDER PLATING (85/15)
   THICKNESS ON ALLOY 42/COPPER.
2. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION.
   MAXIMUM ALLOWABLE MOLD PROTRUSION 0.15 mm PER SIDE.
3. REFERENCE JEDEC REGISTRATION MS-026, VARIATION ABC,
   DATED FEBRUARY 1999.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507