

**32MB (4M x 64) SDRAM SO-DIMM MODULE****Features**

- JEDEC standard 144 pins, small-outline, dual in-line memory module (SODIMM)
- Utilizes 100 MHz SDRAM components
- Unbuffered SO-DIMM
- Auto Refresh and Self Refresh
- CAS latency: 2 and 3
- Burst Length: 1, 2, 4, 8 and full page
- 4k refresh cycles / 64ms
- Interface: LVTTTL
- Serial Presence Detect with EEPROM
- Single 3.3V±0.3V power supply
- PCB: height (1,062 mil) single sided component

Part Number

Module Part Number	Speed Grade	Self-Refresh Current
W9832AASA-10	PC66 CL=2, 3	8mA
W9832AASA10L	PC66 CL=2, 3	1.8mA

General Description

The Winbond W9832AASA is a 4M x 64 Synchronous Dynamic RAM memory module. This module consists of four pieces of W986416AH (4M x 16 bit) SDRAMs in 54-pin TSOP-II 400mil package, and a 2K EEPROM in 8-pin SOP package on a 144-pin 6-layer PCB. A 0.1 uF decoupling capacitor is used for each SDRAM.

The W9832AASA is a Small Out-line Dual In-line Memory Module for mounting into 72-pin dual readout zigzag edge connector sockets. It is designed to operate in 3.3V, low-power memory systems.

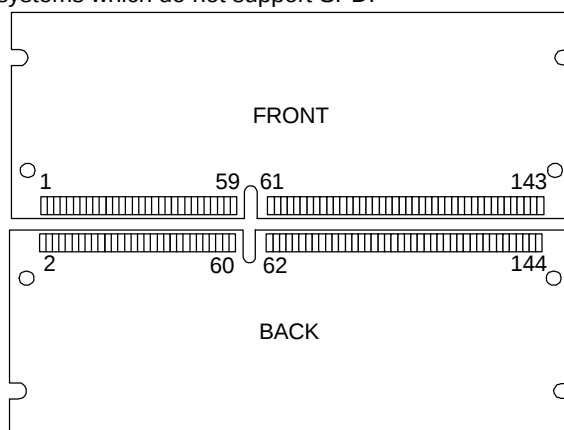
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Pin Assignment

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38					111	A10/AP	112	A11
19	DQ7	20	DQ39	61	CLK0	62	CKE0	113	VDD	114	VDD
21	VSS	22	VSS	63	VDD	64	VDD	115	DQM2	116	DQM6
23	DQM0	24	DQM4	65	RAS#	66	CAS#	117	DQM3	118	DQM7
25	DQM1	26	DQM5	67	WE#	68	*CKE1	119	VSS	120	VSS
27	VDD	28	VDD	69	CS0#	70	A12	121	DQ24	122	DQ56
29	A0	30	A3	71	*CS1#	72	*A13	123	DQ25	124	DQ57
31	A1	32	A4	73	NC	74	CLK1	125	DQ26	126	DQ58
33	A2	34	A5	75	VSS	76	VSS	127	DQ27	128	DQ59
35	VSS	36	VSS	77	NC	78	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	79	NC	80	NC	131	DQ28	132	DQ60
39	DQ9	40	DQ41	81	VDD	82	VDD	133	DQ29	134	DQ61
41	DQ10	42	DQ42	83	DQ16	84	DQ48	135	DQ30	136	DQ62
43	DQ11	44	DQ43	85	DQ17	86	DQ49	137	DQ31	138	DQ63
45	VDD	46	VDD	87	DQ18	88	DQ50	139	VSS	140	VSS
47	DQ12	48	DQ44	89	DQ19	90	DQ51	141	**SDA	142	**SCL
49	DQ13	50	DQ45	91	VSS	92	VSS	143	VDD	144	VDD
				93	DQ20	94	DQ52				

* These pins are not used in this module.

** These pins should be NC in systems which do not support SPD.



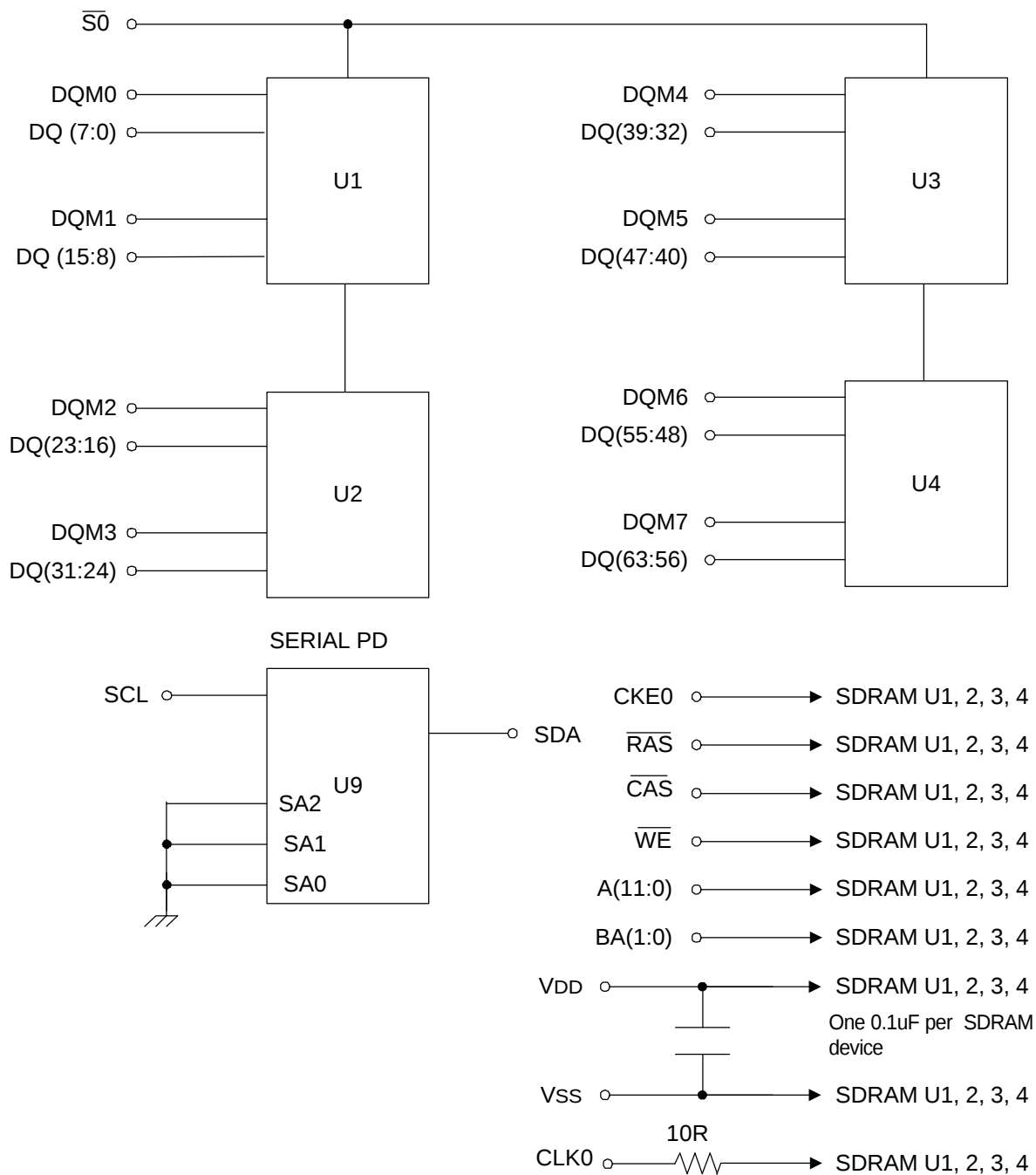
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Pin Description

Pin	Name	Function Description
CLKn	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
CSn#	Chip select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
CKEn	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self-Refresh mode is entered.
A0~A11	Address	Multiplexed pins for row and column address. Row address: A0~A11. Column address: A0~A7.
BA0~BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
RAS#	Row Address Strobe	Command input. When sampled at the rising edge of the clock, RAS#, CAS# and WE# define the operation to be executed.
CAS#	Column Address Strobe	Referred to RAS#
WE#	Write Enable	Referred to RAS#
DQM0~7	Input/Output Mask	The output buffer is placed at Hi-Z when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write data.
DQ0~63	Data Input/Output	Multiplexed pins for data output and input
VDD	Power (+3.3 V)	Power for input buffers and logic circuit inside SDRAM.
VSS	Ground	Ground for input buffers and logic circuit inside SDRAM.
SCL	Serial Clock	Clock for serial presence detection
SDA	Serial Data I/O	Data line for serial presence detection
NC	No Connection	No connection

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}, V_{OUT}	Input, column Output Voltage	$-0.3 \sim V_{CC} + 0.3$	V	
V_{DD}	Power Supply Voltage	$-0.3 \sim 4.6$	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	-55~125	°C	
P_D	Power Dissipation	9	W	
I_{OUT}	Short Circuit Output Current	50	mA	

Note: Operation exceeds "ABSOLUTE MAXIMUM RATING" may cause permanent damage to the devices.

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V	
V_{IH}	Input High Voltage	2.0	-	$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	

Note: $V_{IH}(\text{max}) = V_{DD} + 1.2\text{V}$ for pulse width $\leq 5\text{ns}$
 $V_{IL}(\text{min}) = V_{SS} - 1.2\text{V}$ for pulse width $\leq 5\text{ns}$
 All Voltages are referenced to V_{SS}

CAPACITANCE ($V_{CC}=3.3\text{V}$, $f = 1\text{MHz}$, $T_a=25^{\circ}\text{C}$)

PIN	SYMBOL	MIN	MAX	UNIT
Address(A0~A11, BA0~BA1)	C_{add}	-	16	pf
RAS#, CAS#, WE#	C_{cmd}	-	16	pf
CKE	C_{cke}	-	16	pf
CLK0	C_{cle}	-	24	pf
CS0#	C_{cs}	-	16	pf
DQM0~DQM7	C_{dqm}	-	4	pf
DQ0~DQ63	C_{io}	-	5	pf

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DC CHARACTERISTICS

(VCC = 3.3V ± 0.3V, Ta=0°~70°C)

SYMBOL	ITEMS		-10		10L		UNIT	NOTES
			MIN	MAX	MIN	MAX		
I _{CC1}	OPERATING CURRENT t _{CK} =min, t _{RC} =min Active Precharge command cycling without Burst operation	1 bank operation		440		440	mA	1
I _{CC2}	STANDBY CURRENT t _{CK} =min, CS#=V _{IH}	CKE=V _{IH}		200		200	mA	1
I _{CC2P}	V _{IH} /L=V _{IH} (min)/V _{IL} (max) Bank: inactive state	CKE=V _{IL} (Power Down mode)		12		12		
I _{CC2S}	STANDBY CURRENT CLK=V _{IL} , CS#=V _{IH}	CKE=V _{IH}		20		20	mA	
I _{CC2PS}	V _{IH} /L=V _{IH} (min)/V _{IL} (max) BANK: inactive state	CKE=V _{IL} (Power Down mode)		8		8		
I _{CC3}	No OPERATING CURRENT T _{CK} =min0, CS#=V _{IH} (min)	CKE=V _{IH}		280		280	mA	1
I _{CC3P}	BANK: active state (4 banks)	CKE=V _{IL} (Power Down mode)		32		32	mA	
I _{CC4}	BURST OPERATING CURRENT T _{CK} =min Read/Write command cycling			760		760	mA	1, 2
I _{CC5}	AUTO REFRESH CURRENT T _{CK} =min Auto Refresh command cycling			520		520	mA	1
I _{CC6}	SELF REFRESH CURRENT Self Refresh mode CKE=0.2V			8		1.8	mA	

Note: 1. These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.
2. These parameters depend on the output loading conditions. Specified values are obtained with output open.

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AC CHARACTERISTICS AND OPERATING CONDITION

(Vcc=3.3V±0.3V, Ta=0° to 70°C)

SYMBOL	PARAMETER	- 10		10L		UNIT
		MIN	MAX	MIN	MAX	
t _{RC}	Ref/Active to Ref/Active Command Period	90		90		ns
t _{AS}	Active to precharge Command Period	60	100000	60	100000	
t _{RCD}	Active to Read/Write Command Delay Time	30		30		
t _{CCD}	Read/Write(a) to Read/Write(b) Command Period	1		1		cycle
t _{RP}	Precharge to Active(b) Command Period	30		30		ns
t _{RRD}	Active(a) to Active(b) Command Period	20		20		
t _{WR}	Write Recovery Time	CL*=2	15	1000	15	1000
		CL*=3	10	1000	10	1000
t _{CK}	CLK Cycle Time	CL*=2	15		15	
		CL*=3	10		10	
t _{CH}	CLK High Level	3		3		
t _{CL}	CLK Low Level	3		3		
t _{AC}	Access Time from CLK	CL*=2		9		9
		CL*=3		8		8
t _{OH}	Output Data Hold Time	3		3		
t _{HZ**}	Output Data High Impedance Time	3	10	3	10	
t _{LZ}	Output Data Low Impedance Time	0		0		
t _{SB}	Power Down Mode Entry Time	0	10	0	10	
t _T	Transition Time of CLK (Rise and Fall)	0.5	10	0.5	10	
t _{DS}	Data-in-Set-up Time	3		3		
t _{DH}	Data-in Hold Time	1		1		
t _{AS}	Address Set-up Time	3		3		
t _{AH}	Address Hold Time	1		1		
t _{CKS}	CKE Set-up Time	3		3		
t _{CKH}	CKE Hold Time	1		1		
t _{CMS}	Command Set-up Time	3		3		
t _{CMH}	Command Hold Time	1		1		
t _{REF}	Refresh Time		64		64	ms
t _{RSC}	Mode register Set Cycle Time	20		20		ns

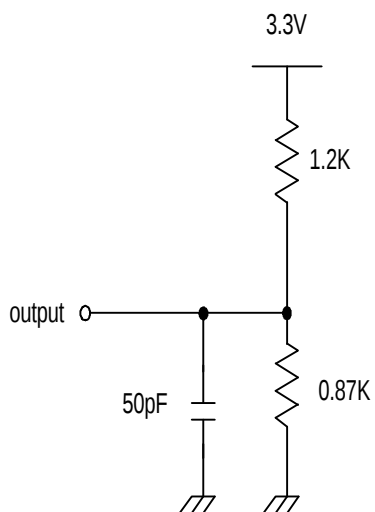
Note: *CL= CAS Latency

** t_{HZ} defines the time at which the outputs achieve the open circuit condition and is not referenced to output level.
Refer to the individual component

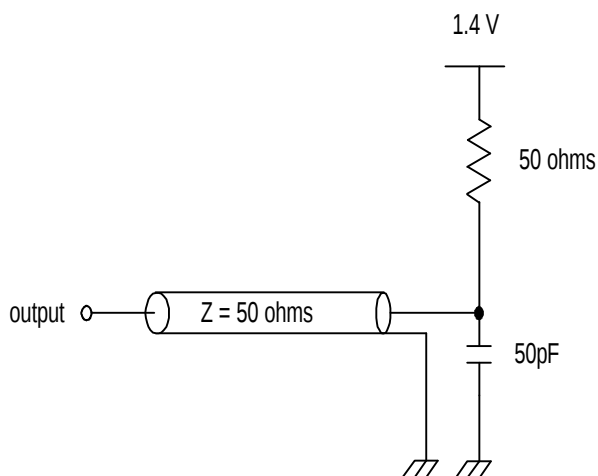
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AC TESTING CONDITIONS

Output Timing Measurement Reference Level	1.4V/1.4V
Output Load	See diagram B Below
Input Signal Levels	2.4V/0.4V
Transition Time (Rise and Fall) of Input Signal	2ns
Input Reference Level	1.4V



AC TEST LOAD (A)



AC TEST LOAD (B)

Note: Transition times are measured between V_{IH} and V_{IL}

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Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 1 shows the truth table for the operation commands.

Table 1: Truth Table (note (1), (2))

COMMAND	Device state	CKEn-1	CKEn	DQM	BA0, BA1	A10	A11, A9-0	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$
Bank Active	Idle	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active (3)	H	X	X	V	L	V	L	H	L	L
Write with Autoprecharge	Active (3)	H	X	X	V	H	V	L	H	L	L
Read	Active (3)	H	X	X	V	L	V	L	H	L	H
Read with Autoprecharge	Active (3)	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No – Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active (4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto – Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self - Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	idle (S.R.)	L L	H H	X X	X X	X X	X X	H L	X H	X H	X X
Clock suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Idle Active (5)	H H	L L	X X	X X	X X	X X	H L	X H	X H	X X
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (power down)	L L	H H	X X	X X	X X	X X	H L	X H	X H	X X
Data write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes: (1) V= Valid X= Don't care L= Low Level H= High Level

(2) CKEn signal is input level when commands are provided.

(3) These are state of bank designated by BA0, BA1 signals.

(4) Device state is full page burst operation.

(5) Power Down Mode can not be entered in the burst cycle. When this command asserts in the burst cycle, device state is clock suspend mode

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Serial Presence Detect EEPROM

The Serial Presence Detect (SPD) function is implemented using a 2,408-bit EEPROM component. This nonvolatile storage device contains data for identifying the module type and various SDRAM organization and timing parameters. System read operations to the EEPROM device occur using the DIMM SCL(clock) and SDA (data) signals, together with SA(2:0) which provide the EEPROM Device Address.

SPD EEPROM DC OPERATING CONDITIONS

(V_{cc}=3.3V±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNIT	NOTES
Supply Voltage	V _{cc}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V _{IH}	V _{cc} ×.7	V _{cc} + .5	V	
Input Low (Logic 0) Voltage, all inputs	V _{IL}	-0.3	V _{cc} ×.3	V	
OUTPUT LOW VOTAGE, I _{out} =3 mA	V _{OL}		0.4	V	I _{OL} =3mA
INPUT LEAKGE CURRENT, V _{in} =GND to V _{cc}	I _{LI}		1	uA	
OUTPUT LEAKAGE CURRENT, V _{OUT} =GND to V _{cc}	I _{LO}		1	uA	
STANDBY CURRENT SCL=SDA V _{cc} -0.3V, All other inputs=GND or 3.3V +10%	I _{SB}		10	uA	
POWER SUPPLY CURRENT SCL clock frequency =100KHz	I _{cc}		1	mA	

SPD AC OPERATING CONDITIONS

(V_{cc}=3.3V±0.3V)

AC CHRRACTERICS					
PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
SCL clock frequency	f _{SCL}		100	KHz	
Noise Suppression Time Constant at SCL,SDA Inputs	t _i		100	ns	
SCL Low to SDA Data Out Valid	t _{AA}	0.3	3.5	us	
Time the bus must be free before a new transition can start	t _{BUF}	4.7		us	
Start Condition Hold Time	t _{HD:STA}	4.0		us	
Clock Low Period	t _{LOW}	4.7		us	
Clock High Period	t _{HIGH}	4.0		us	
Start Condition Setup Time	t _{SU:STA}	4.7		us	
Data in Hold Time	t _{HD:DAT}	0		us	
Data in Setup Time	t _{SU:DAT}	250		ns	
SDA and SCL Rise time	t _R		1	us	
SDA and SCL Fall Time	t _F		300	ns	
Stop Condition Setup Time	t _{SU:STO}	4.7		us	
Data Out Hold Time	t _{DH}	300		ns	
Write Cycle Time	t _{WR}		15	ms	

Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle the EEPROM bus interface circuits are disabled, SDA is allowed to remain high the bus level pull-up resistor, and the device does not respond to its slave address.

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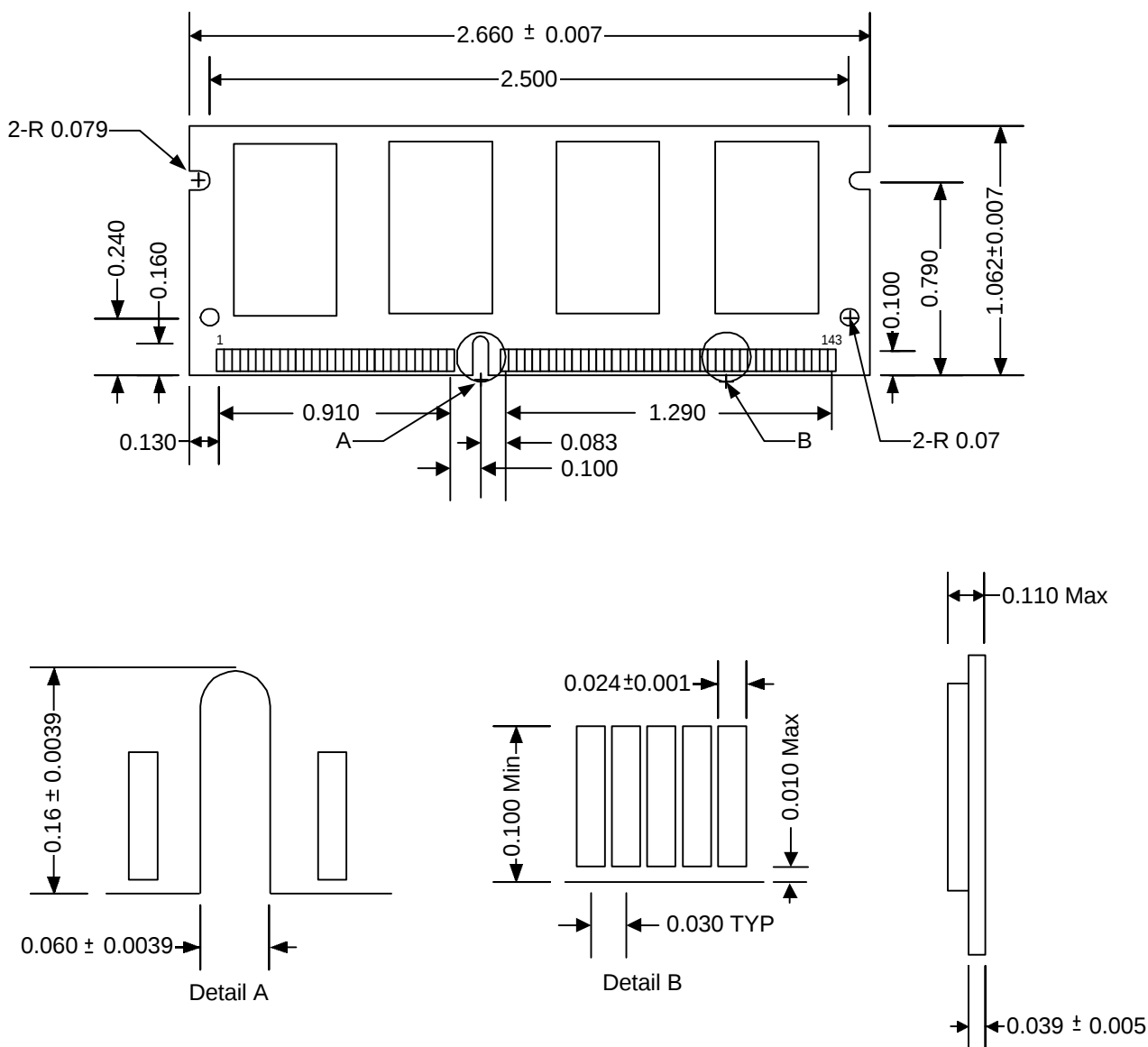
CONTENTS OF EEPROM

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION SUPPORTED	HEX VALUE
		-10/10L	-10/10L
0	Defines # bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # bytes of SPD memory device	256 bytes (2K- bit)	08h
2	Fundamental memory type (FPM, EDO, SDRAM..)	SDRAM	04h
3	# Row Addresses on this assembly	12	0Ch
4	# Column Addresses on this assembly	8	08h
5	# Module Rows on this assembly	1 row	01h
6	Data Width of this assembly...	64 bits	40h
7	Data Width continuation	-	00h
8	Voltage interface standard of this assembly	LVTTL	01h
9	SDRAM Cycle time @CAS latency of 3	10ns	A0h
10	SDRAM Access time form clock @CAS latency of 3	8ns	80h
11	DIMM Configuration type (Non-parity, Parity ECC)	Non parity	00h
12	Refresh Rate/Type	15.625 us, support self refresh	80h
13	SDRAM width, Primary DRAM	X16	10h
14	Error Checking SDRAM data width	None	00h
15	Minimum Clock Delay, Back Random Column Addresses	TCCD=1 CLK	01h
16	Burst Lengths supported	1, 2, 4, 8 & full page	8Fh
17	#Bank on Each SDRAM device	4 banks	04h
18	CAS# Latencies Supported	2 & 3	06h
19	CS# Latency	0 CLK	01h
20	Write Latency	0 CLK	01h
21	SDRAM Module Attributes	Non-buffered Non –registered & redundant addressing	00h
22	SDRAM Device Attributes: General	+/-10% voltage tolerance, Burst Read, Single bit Write, precharge all, auto precharge	0Eh
23	SDRAM cycle time @ CAS latency of 2	15ns	F0h
24	SDRAM access time form clock @CAS latency of 2	9ns	90h
25	SDRAM cycle time @ CAS latency of 1	-	00h
26	SDRAM access time from clock @CAS latency of 1	-	00h
27	Precharge to active command period (t _{RP})	30ns	1Eh
28	Active to Active command period (t _{RRD})	20ns	14h
29	Active to Read/Write command delay time(t _{RCD})	30ns	1Eh
30	Minimum Active to precharge period (t _{RAS})	60ns	3Ch
31	Density of each Row on Module	1 row of 32MB .	08h
32	Command and Address signal input setup time	3ns	30h
33	Command and Address signal input hold time	1ns	10h
34	Data signal input setup time	3ns	30h
35	Data signal input hold time	1ns	10h
36-61	Superset Information(may be used in future)	-	00h
62	SPD Revision	Current release Intel spd 1.2	12h
63	Checksum for Bytes 0-62	-	E2h
64-71	Manufacturers code		MFG Dep
72	Manufacturing location		MFG Dep
73-90	Manufacturer's Part Number		MFG Dep
91-92	Revision Code		MFG Dep
93-94	Manufacturing Date		MFG Dep
95-98	Assembly Serial Number		MFG Dep
99-125	Manufacturer Specific Data		MFG Dep
126	Intel specification for frequency	66MHz	66h
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h
128+	Unused storage locations		FFh

32MB (4M x 64) SDRAM SO-DIMM MODULE

PACKGE DIMENSIONS

Units:Inches



Tolerance : ± 0.005 unless otherwise specified
The used device is 4Mx16 SDRAM,TSOP