

HD74HC373 ● Octal D-type Transparent Latches (with 3-state outputs) **HD74HC533** ● Octal D-type Transparent Latches (with inverted 3-state outputs)

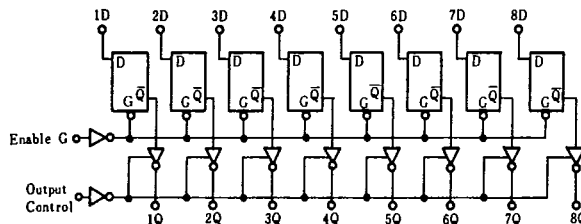
When the latch enable input is high, the Q outputs of HD74HC373 will follow the D inputs and the Q outputs of HD74HC533 will follow the inversion of the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

FEATURES

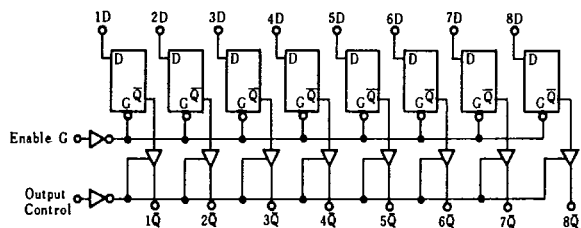
- High Speed Operation: t_{pd} (D to Q) = 16ns typ. ($C_L = 50\text{pF}$)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{cc} = 2 \sim 6\text{V}$
- Low Input Current: $1\mu\text{A}$ max.
- Low Quiescent Supply Current: I_{cc} (static) = $4\mu\text{A}$ max. ($T_a = 25^\circ\text{C}$)

BLOCK DIAGRAM

● HD74HC373

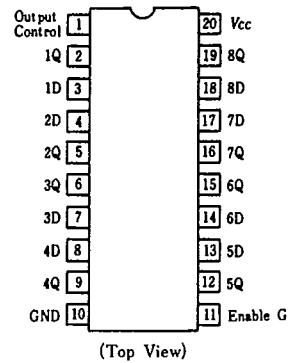


● HD74HC533

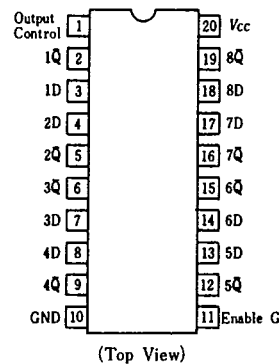


PIN ARRANGEMENT

● HD74HC373



● HD74HC533



FUNCTION TABLE

Output Control	Enable G	D	HD74HC373 Q	HD74HC533 $\bar{Q}$
L	H	H	H	L
L	H	L	L	H
L	L	X	No Change	No Change
H	X	X	Z	Z

Notes) X: irrelevant

Z: Off (high-impedance) state of a 3-state output.



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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage Range	V_{CC}	$-0.5 \sim +7.0$	V
Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
DC Current Drain per pin	I_{OUT}	± 35	mA
DC Current Drain per V_{CC} , GND	I_{CC}, I_{GND}	± 75	mA
DC Input Diode Current	I_{IK}	± 20	mA
DC Output Diode Current	I_{OK}	± 20	mA
Power Dissipation per Package	P_T	500	mW
Storage Temperature	T_{stg}	$-65 \sim +150$	°C

■ DC CHARACTERISTICS

Item	Symbol	$V_{CC}(V)$	Test Conditions	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim +85^\circ\text{C}$		Unit
				min	typ	max	min	max	
Input Voltage	V_{IH}	2.0		1.5	—	—	1.5	—	V
		4.5		3.15	—	—	3.15	—	
		6.0		4.2	—	—	4.2	—	
	V_{IL}	2.0		—	—	0.5	—	0.5	V
		4.5		—	—	1.35	—	1.35	
		6.0		—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$		1.9	2.0	—	V
		4.5				4.4	4.5	—	
		6.0				5.9	6.0	—	
		4.5		$I_{OH} = -6 \text{mA}$		4.18	—	—	
		6.0		$I_{OH} = -7.8 \text{mA}$		5.68	—	—	
		6.0				—	—	5.63	
	V_{OL}	2.0	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$		—	0.0	0.1	V
		4.5				—	0.0	0.1	
		6.0				—	0.0	0.1	
		4.5		$I_{OL} = 6 \text{mA}$		—	—	0.26	
		6.0		$I_{OL} = 7.8 \text{mA}$		—	—	0.26	
		6.0				—	—	0.33	
Off-state Output Current	I_{OZ}	6.0	$V_{in} = V_{IH} \text{ or } V_{IL}, V_{out} = V_{CC} \text{ or } \text{GND}$	—	—	± 0.5	—	± 5.0	μA
Input Current	I_{in}	6.0	$V_{in} = V_{CC} \text{ or } \text{GND}$	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	6.0	$V_{in} = V_{CC} \text{ or } \text{GND}, I_{out} = 0 \mu\text{A}$	—	—	4.0	—	40	μA

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■ AC CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6\text{ns}$)

Item	Symbol	$V_{CC}(\text{V})$	Test Conditions	$T_a=25^\circ\text{C}$			$T_a=-40\sim+85^\circ\text{C}$		Unit
				min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	G to Q	—	—	150	—	190	ns
		4.5		—	18	30	—	38	
		6.0		—	—	26	—	33	
	t_{PLH} t_{PHL}	2.0	D to Q	—	—	125	—	155	ns
		4.5		—	16	25	—	31	
		6.0		—	—	21	—	26	
Output Enable Time	t_{ZL}	2.0		—	—	150	—	190	ns
		4.5		—	12	30	—	38	
		6.0		—	—	26	—	33	
	t_{ZH}	2.0		—	—	150	—	190	ns
		4.5		—	15	30	—	38	
		6.0		—	—	26	—	33	
Output Disable Time	t_{LZ}	2.0		—	—	150	—	190	ns
		4.5		—	13	30	—	38	
		6.0		—	—	26	—	33	
	t_{HZ}	2.0		—	—	150	—	190	ns
		4.5		—	16	30	—	38	
		6.0		—	—	26	—	33	
Setup Time	t_{su}	2.0		100	—	—	125	—	ns
		4.5		20	1	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0		50	—	—	65	—	ns
		4.5		10	1	—	13	—	
		6.0		9	—	—	11	—	
Pulse Width	t_w	2.0		80	—	—	100	—	ns
		4.5		16	6	—	20	—	
		6.0		14	—	—	17	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	60	—	75	ns
		4.5		—	4	12	—	15	
		6.0		—	—	10	—	13	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF



PACKAGE INFORMATION

T-90-20

In the HD74HC series of HS-CMOS logic, either of plastic DIP and small outline packages can be selected.
For your ordering, please refer to the following package code.

● Package code of HS-CMOS Logic

HD74HC XXXXP

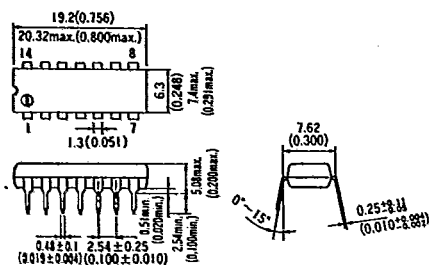
Package code (P : Plastic DIP, FP : Small outline package)
Individual device code
Series code of HS-CMOS logic
Initial code of Hitachi digital IC

■ PLASTIC DIP PACKAGE [Unit: mm (inch), scale: $\frac{1}{1}$]

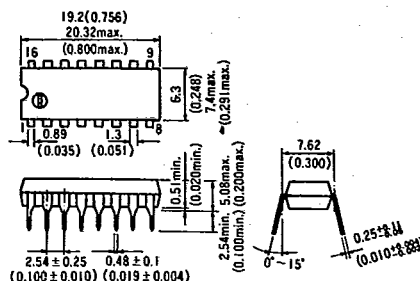
● 14-pin type

● 16-pin type

DP-14



DP-16

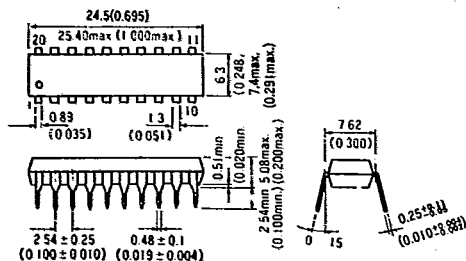


Note) For the present, both packages of 0.89 and 1.3 can be used. Please refer to the Technical Marketing Dept. for further details.

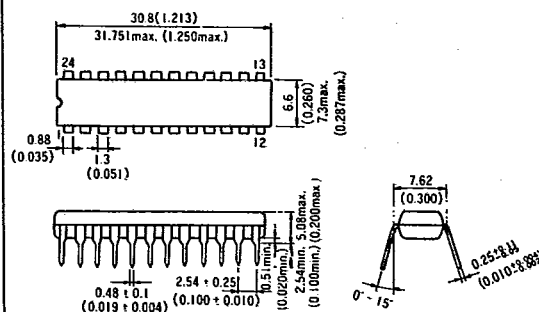
● 20-pin type

● 24-pin type

DP-20N



DP-24N



Note) Because this is under development, the dimensions may be changed partly.

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F-06



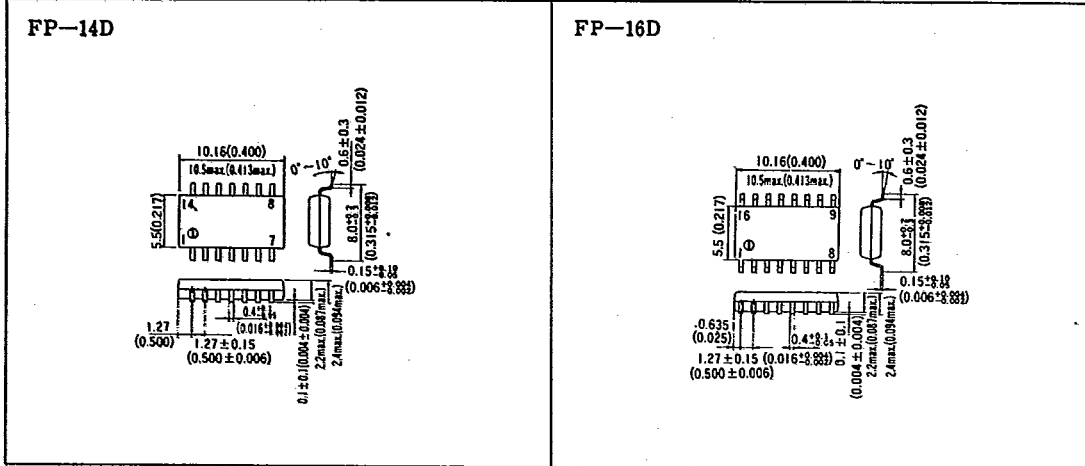
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■ SMALL OUTLINE PACKAGE [Unit: mm (inch), scale: 1½]

● 14—pin type

● 16—pin type



● 20—pin type

