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# HN62W448N Series

524288-word  $\times$  16-bit/1048576-word  $\times$  8-bit CMOS Mask  
Programmable ROM

# HITACHI

ADE-203-484(A) (Z)  
Preliminary  
Rev. 0.1  
Jun. 20, 1996

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## Description

The Hitachi HN62W448N is a 8-Mbit CMOS mask-programmable ROM organized either as 524288-words by 16-bits or as 1048576-words by 8-bits. Realizing low power consumption with low voltage operation, this memory is allowed for battery operation. And low voltage high speed page access of 60/70 ns and normal access of 120/150 ns are realized.

## Features

- Low voltage operation :  $3.3\text{ V} \pm 0.3\text{ V}$
- Access time:
  - Normal access time: 120/150 ns (max)
  - Page access time: 60/70 ns (max)
- Low power dissipation
  - Active: 220 mW (max)
  - Standby: 3  $\mu$ W (max)
- Byte-wide or word-wide data organization (Switched by BHE terminal)
- 4-word page access mode
- Three-state data output for wired or-tying
- Directly LVTTL compatible (All inputs and outputs)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

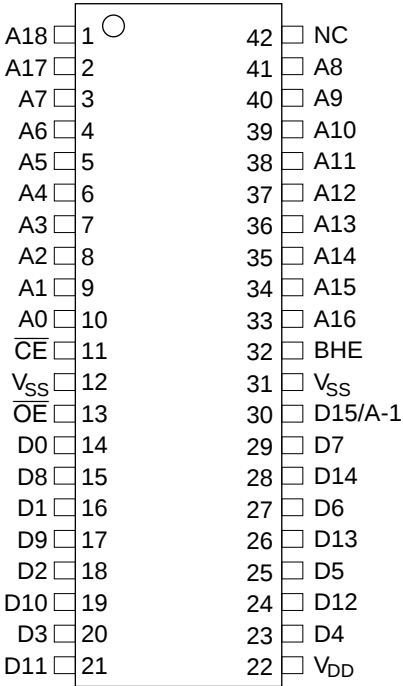
# HN62W448N Series

## Ordering Information

| Type No.       | Access time | Package                           |
|----------------|-------------|-----------------------------------|
| HN62W448NP-12  | 120 ns      | 600mil 42-pin plastic DIP (DP-42) |
| HN62W448NP-15  | 150 ns      |                                   |
| HN62W448NFB-12 | 120 ns      | 44-pin plastic SOP (FP-44D)       |
| HN62W448NFB-15 | 150 ns      |                                   |
| HN62W448NTT-12 | 120 ns      | 44-pin plastic TSOP II (TTP-44D)  |
| HN62W448NTT-15 | 150 ns      |                                   |

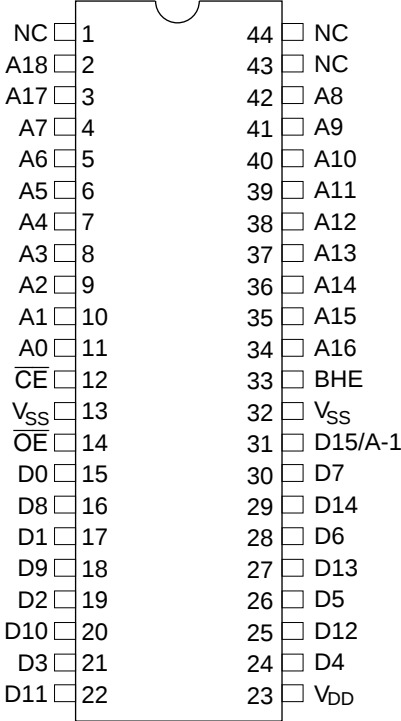
## Pin Arrangement

HN62W448NP Series



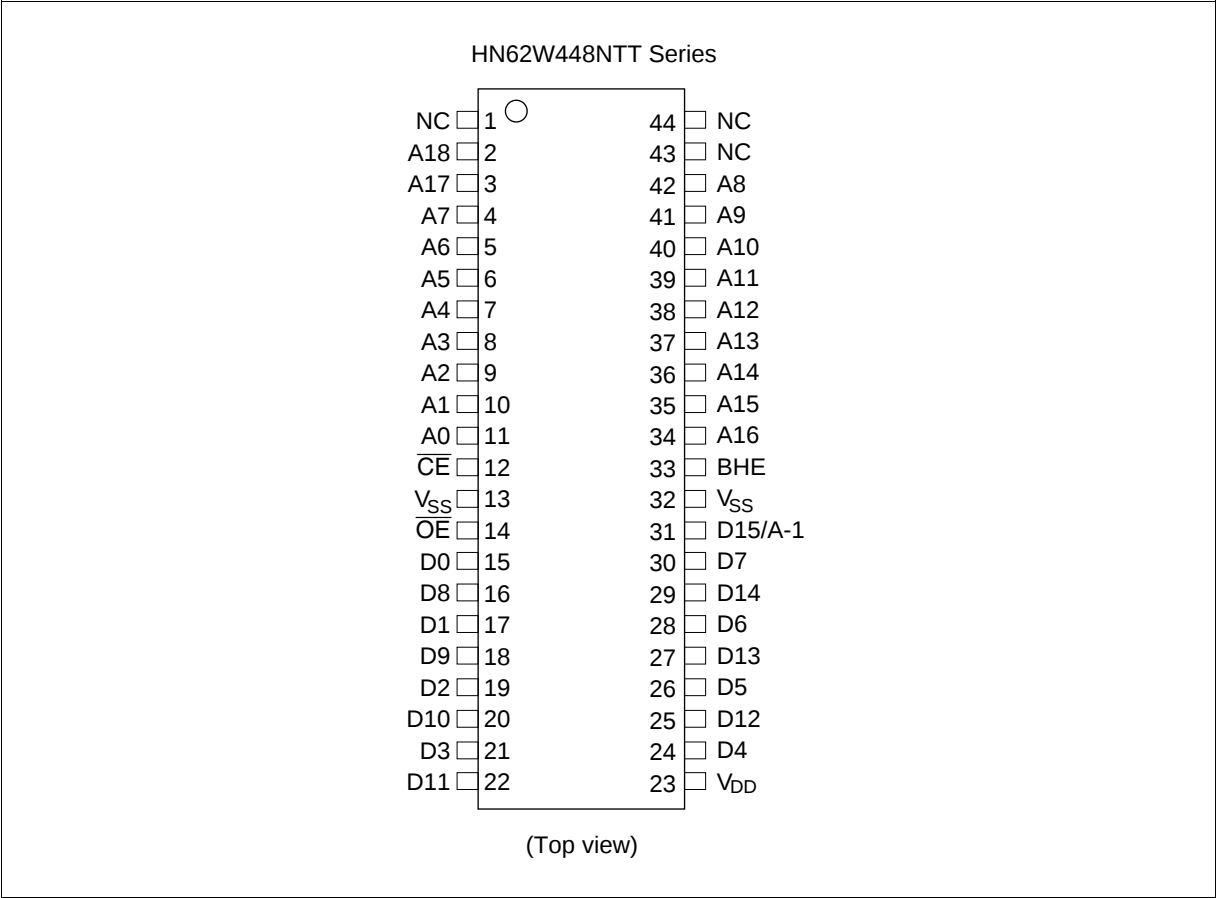
(Top view)

HN62W448NFB Series



(Top view)

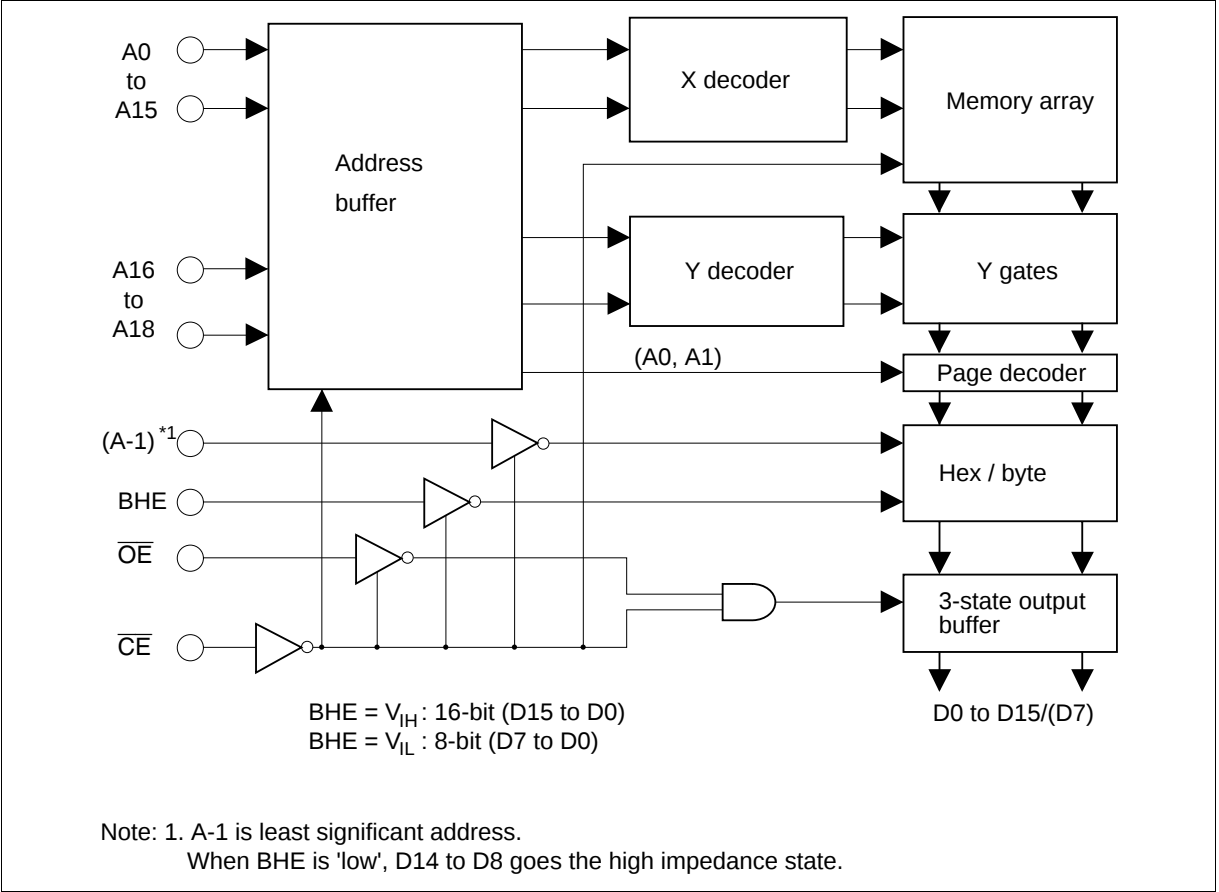
Pin Arrangement (cont.)



Pin Description

| Pin name        | Function            |
|-----------------|---------------------|
| A0 to A18       | Address             |
| D0 to D14       | Output              |
| D15/A-1         | Output/address      |
| OE              | Output enable       |
| CE              | Chip enable         |
| BHE             | Byte/word selection |
| V <sub>DD</sub> | Power supply        |
| V <sub>SS</sub> | Ground              |
| NC              | No connection       |

Block Diagram



Absolute Maximum Ratings

| Parameter                    | Symbol            | Value                  | Unit | Note |
|------------------------------|-------------------|------------------------|------|------|
| Supply voltage               | $V_{DD}$          | -0.3 to +5.5           | V    | 1    |
| All input and output voltage | $V_{in}, V_{out}$ | -0.3 to $V_{DD} + 0.3$ | V    | 1    |
| Operating temperature range  | $T_{opr}$         | 0 to 70                | °C   |      |
| Storage temperature range    | $T_{stg}$         | -55 to +125            | °C   |      |
| Temperature under bias       | $T_{bias}$        | -20 to +85             | °C   |      |

Note: 1. With respect to  $V_{SS}$ .

Recommended DC Operating Conditions ( $T_a = 0$  to  $+70^{\circ}\text{C}$ )

| Parameter      | Symbol   | Min  | Typ | Max            | Unit |
|----------------|----------|------|-----|----------------|------|
| Supply voltage | $V_{DD}$ | 3.0  | 3.3 | 3.6            | V    |
|                | $V_{SS}$ | 0    | 0   | 0              | V    |
| Input voltage  | $V_{IH}$ | 2.2  | —   | $V_{DD} + 0.3$ | V    |
|                | $V_{IL}$ | -0.3 | —   | 0.8            | V    |

DC Characteristics ( $V_{DD} = 3.3\text{ V} \pm 0.3\text{V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0$  to  $+70^{\circ}\text{C}$ )

| Parameter              |         | Symbol     | Min | Max | Unit          | Test conditions                                                                   |
|------------------------|---------|------------|-----|-----|---------------|-----------------------------------------------------------------------------------|
| Supply current         | Active  | $I_{DD}$   | —   | 60  | mA            | $V_{DD} = 3.6\text{ V}$ , $I_{DOUT} = 0\text{ mA}$ , $t_{RC} = 120/150\text{ ns}$ |
|                        | Standby | $I_{SB1}$  | —   | 30  | $\mu\text{A}$ | $V_{DD} = 3.6\text{ V}$ , $\overline{CE} \geq V_{DD} - 0.2\text{ V}$              |
|                        | Standby | $I_{SB2}$  | —   | 3   | mA            | $V_{DD} = 3.6\text{ V}$ , $\overline{CE} = 2.2\text{ V}$                          |
| Input leakage current  |         | $ I_{IL} $ | —   | 10  | $\mu\text{A}$ | $V_{in} = 0$ to $V_{DD}$                                                          |
| Output leakage current |         | $ I_{OL} $ | —   | 10  | $\mu\text{A}$ | $\overline{CE} = 2.2\text{ V}$ , $V_{OUT} = 0$ to $V_{DD}$                        |
| Output voltage         |         | $V_{OH}$   | 2.4 | —   | V             | $I_{OH} = -2.0\text{ mA}$                                                         |
|                        |         | $V_{OL}$   | —   | 0.4 | V             | $I_{OL} = 2.0\text{ mA}$                                                          |

Capacitance ( $V_{DD} = 3.3\text{ V} \pm 0.3\text{V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 25^{\circ}\text{C}$ ,  $V_{in} = 0\text{ V}$ ,  $f = 1\text{ MHz}$ )

| Parameter                        | Symbol    | Min | Max | Unit |
|----------------------------------|-----------|-----|-----|------|
| Input capacitance <sup>*1</sup>  | $C_{in}$  | —   | 10  | pF   |
| Output capacitance <sup>*1</sup> | $C_{out}$ | —   | 15  | pF   |

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics ( $V_{DD} = 3.3\text{ V} \pm 0.3\text{V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0\text{ to } +70^{\circ}\text{C}$ )

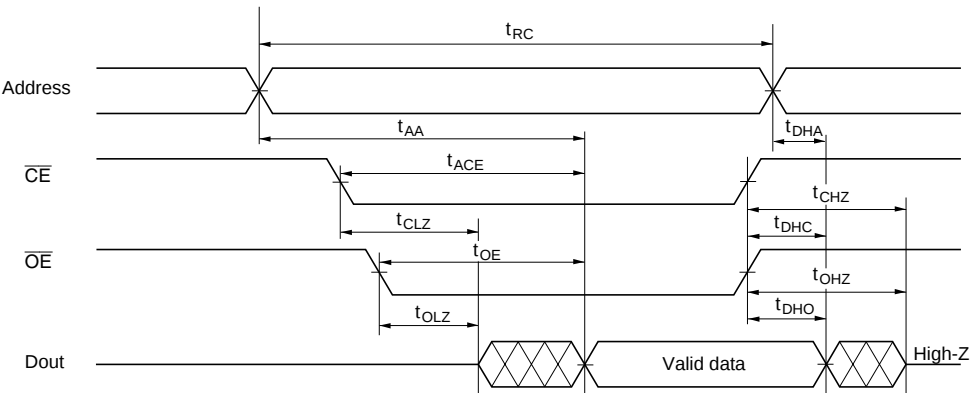
- Output load: 1TTL gate +  $C_L = 50\text{ pF}$  (including scope & jig)
- Input pulse levels: 0.4 to 2.4 V
- Input and output timing reference levels: 1.4V
- Input rise and fall time: 5 ns

| Parameter                             | Symbol         | HN62W448N-12 |     | HN62W448N-15 |     | Unit |
|---------------------------------------|----------------|--------------|-----|--------------|-----|------|
|                                       |                | Min          | Max | Min          | Max |      |
| Read cycle time                       | $t_{RC}$       | 120          | —   | 150          | —   | ns   |
| Page read cycle time                  | $t_{PC}$       | 50           | —   | 70           | —   | ns   |
| Address access time                   | $t_{AA}$       | —            | 120 | —            | 150 | ns   |
| Page address access time              | $t_{PA}$       | —            | 50  | —            | 70  | ns   |
| $\overline{CE}$ access time           | $t_{ACE}$      | —            | 120 | —            | 150 | ns   |
| $\overline{OE}$ access time           | $t_{OE}$       | —            | 50  | —            | 70  | ns   |
| BHE access time                       | $t_{BHE}$      | —            | 120 | —            | 150 | ns   |
| Output hold time from address change  | $t_{DHA}$      | 0            | —   | 0            | —   | ns   |
| Output hold time from $\overline{CE}$ | $t_{DHC}$      | 0            | —   | 0            | —   | ns   |
| Output hold time from $\overline{OE}$ | $t_{DHO}$      | 0            | —   | 0            | —   | ns   |
| Output hold time from BHE             | $t_{DHB}$      | 0            | —   | 0            | —   | ns   |
| $\overline{CE}$ to output in high-Z   | $t_{CHZ}^{*1}$ | —            | 50  | —            | 70  | ns   |
| $\overline{OE}$ to output in high-Z   | $t_{OHZ}^{*1}$ | —            | 50  | —            | 70  | ns   |
| BHE to output in high-Z               | $t_{BHZ}^{*1}$ | —            | 50  | —            | 70  | ns   |
| $\overline{CE}$ to output in low-Z    | $t_{CLZ}$      | 5            | —   | 5            | —   | ns   |
| $\overline{OE}$ to output in low-Z    | $t_{OLZ}$      | 5            | —   | 5            | —   | ns   |
| BHE to output in low-Z                | $t_{BLZ}$      | 5            | —   | 5            | —   | ns   |

Note: 1.  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{BHZ}$  are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

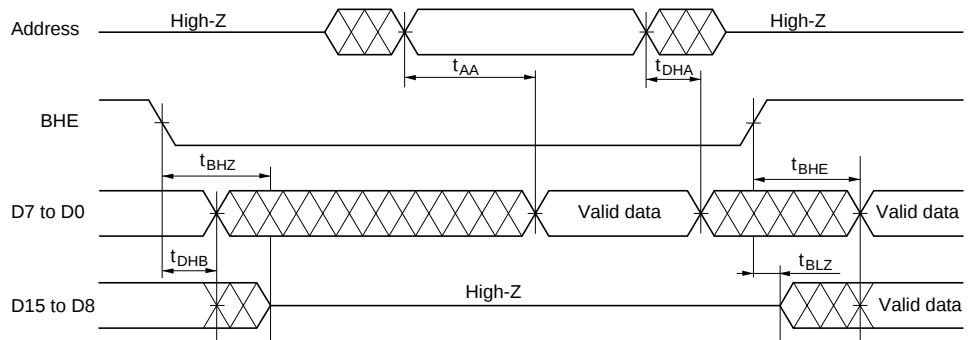
Timing Waveforms

Word Mode (BHE = 'V<sub>IH</sub>') or Byte Mode (BHE = 'V<sub>IL</sub>')



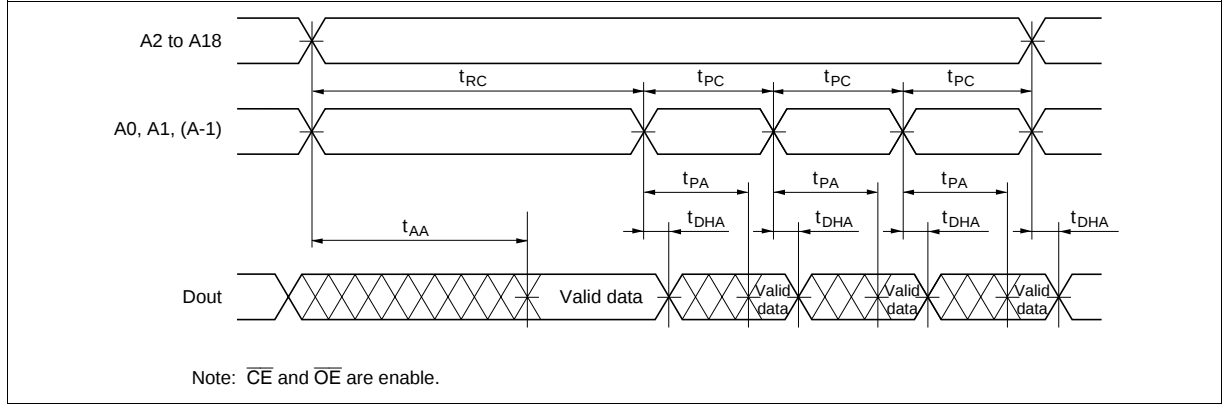
- Notes:
- 1.  $t_{DHA}$ ,  $t_{DHC}$ ,  $t_{DHO}$ : Determined by faster.
  - 2.  $t_{AA}$ ,  $t_{ACE}$ ,  $t_{OE}$ : Determined by slower.
  - 3.  $t_{CLZ}$ ,  $t_{OLZ}$ : Determined by slower.

Word Mode, Byte Mode Switch



- Notes:
- 1.  $\overline{CE}$  and  $\overline{OE}$  are enable A18 to A0 are valid.
  - 2. D15/A-1 pin is in the output state when BHE is high,  $\overline{CE}$  and  $\overline{OE}$  are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.

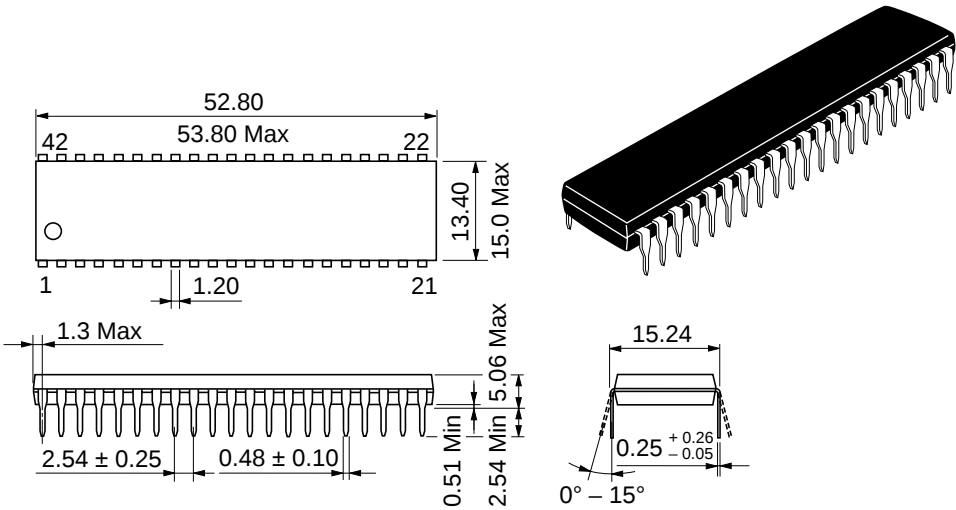
Page Mode



Package Dimensions

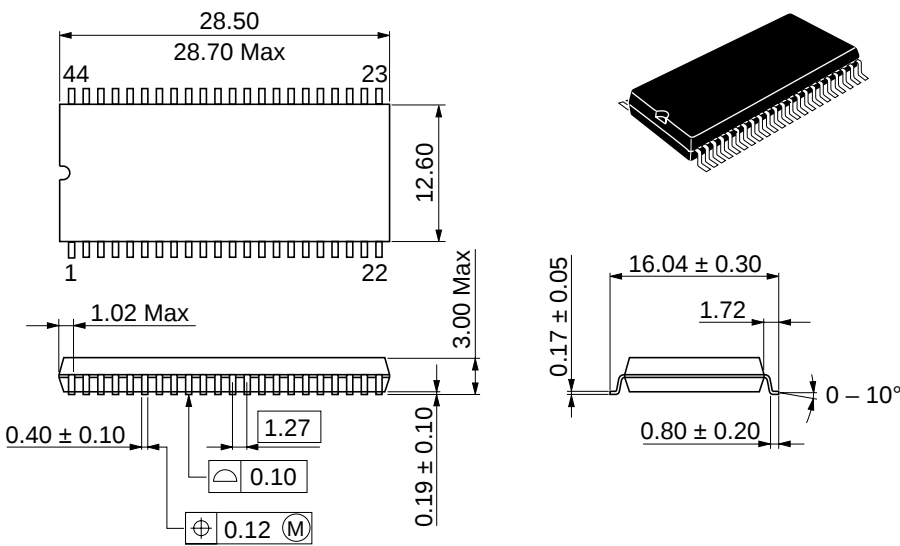
HN62W448NP Series (DP-42)

Unit: mm



HN62W448NFB Series (FP-44D)

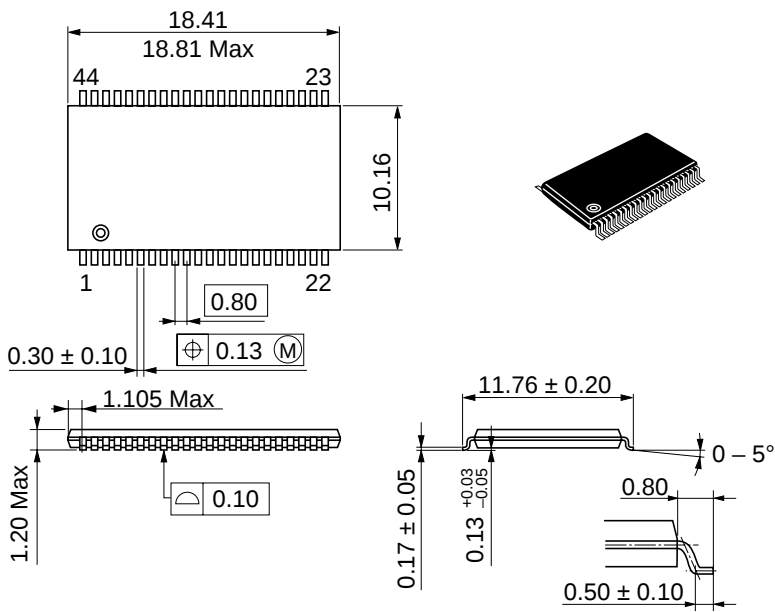
Unit: mm



Package Dimensions (cont.)

HN62W448NTT Series (TTP-44D)

Unit: mm



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Revision Record

| Rev. | Date          | Contents of Modification                                                                                                                                                                                                                                                                                                     | Drawn by  | Approved by |
|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------|
| 0.0  | Nov. 22, 1995 | Initial issue                                                                                                                                                                                                                                                                                                                | Y. Yamada | T. Wada     |
| 0.1  | Jun. 20, 1996 | AC Characteristics<br>Output load: 1TTL + C <sub>L</sub> = 100 pF to 1TTL + C <sub>L</sub> = 50 pF<br>t <sub>PC</sub> min: 60/70 ns to 50/70 ns<br>t <sub>PA</sub> , t <sub>OE</sub> , t <sub>CHZ</sub> , t <sub>OHZ</sub> , t <sub>BHZ</sub> max: 60/70 ns to 50/70 ns<br>Deletion of timing waveform for power up sequence |           |             |