

HM62W256 Series

32,768-word × 8-bit Low Voltage Operation CMOS Static RAM

HITACHI

ADE-203-084G (Z)
Rev. 7.0
Jun. 19, 1995

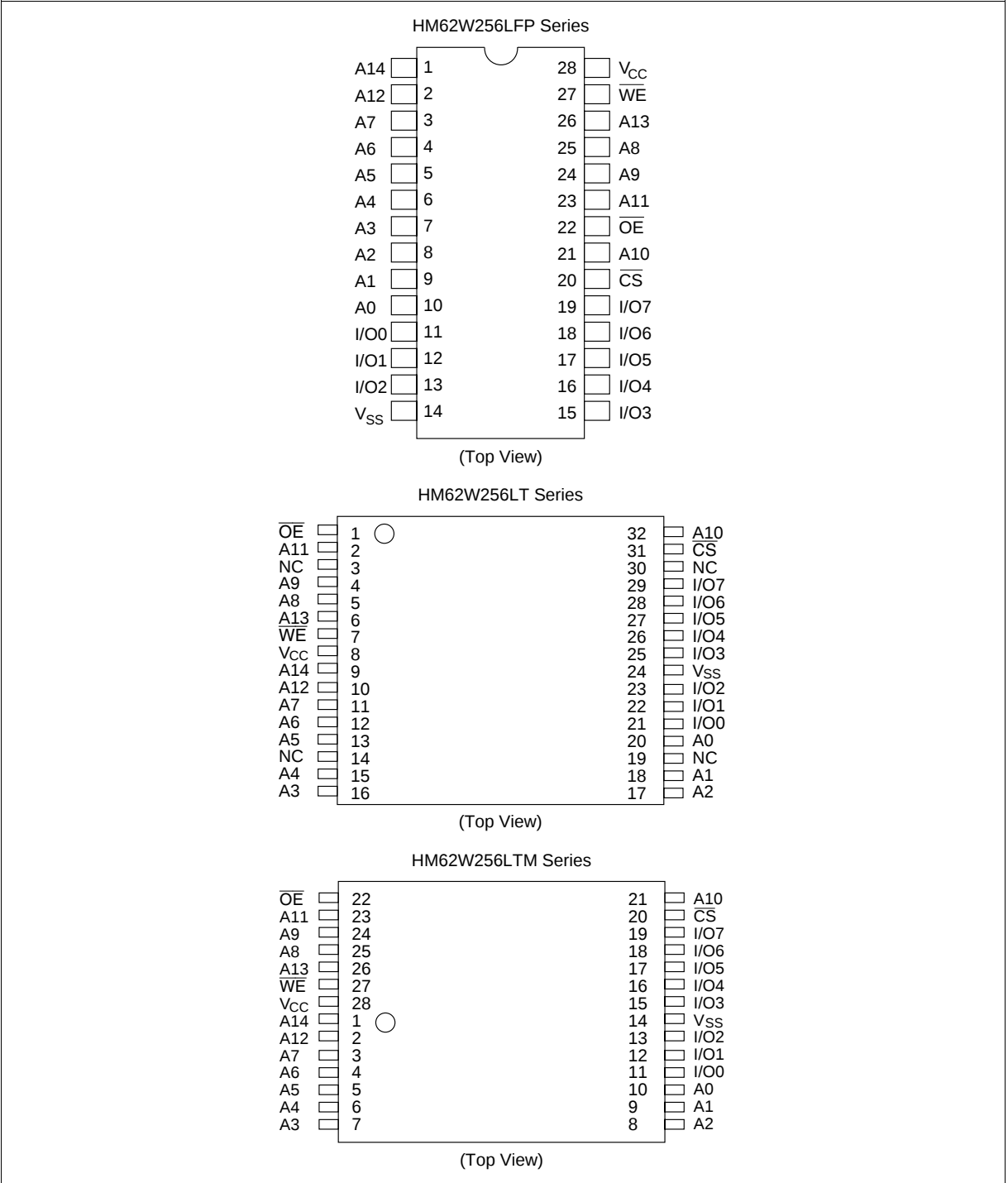
Features

- Low voltage operation SRAM
Operating Supply Voltage: 3.0 V to 3.6 V
- 0.8 μm Hi-CMOS process
- High speed
Access time: 55/70/85 ns (max)
- Low power
Standby: 0.33 μW (typ)
- Completely static memory
No clock or timing strobe required
- Directly LVTTTL compatible: All inputs and outputs

Ordering Information

Type No.	Access Time	Package
HM62W256LFP-7T	70 ns	450 mil 28-pin plastic SOP (FP-28DA)
HM62W256LFP-5SLT	55 ns	
HM62W256LFP-7SLT	70 ns	
HM62W256LFP-8SLT	85 ns	
HM62W256LFP-7ULT	70 ns	8 mm × 14 mm 32-pin TSOP (normal type) (TFP-32DA)
HM62W256LT-7	70 ns	
HM62W256LT-7SL	70 ns	
HM62W256LT-8SL	85 ns	
HM62W256LTM-7	70 ns	8 mm × 13.4 mm 28-pin TSOP (normal type) (TFP-28DA)
HM62W256LTM-5SL	55 ns	
HM62W256LTM-7SL	70 ns	
HM62W256LTM-8SL	85 ns	
HM62W256LTM-7UL	70 ns	

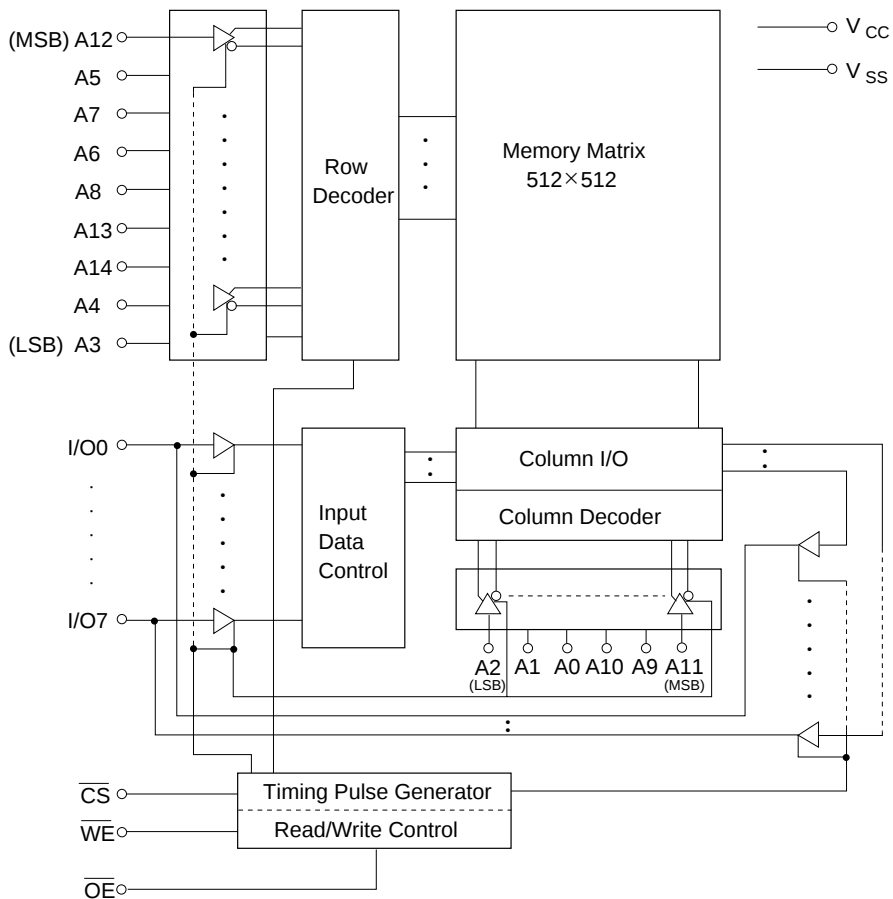
Pin Arrangement



Pin Description

Pin name	Function
A0 – A14	Address inputs
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V _{cc}	Power supply
V _{ss}	Ground

Block Diagram



HM62W256 Series

Function Table

$\overline{\text{WE}}$	$\overline{\text{CS}}$	$\overline{\text{OE}}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
X	H	X	Not selected	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage ^{*1}	V_{CC}	−0.5 to 4.6	V
Terminal voltage ^{*1}	V_{T}	−0.5 ^{*2} to $V_{\text{CC}} + 0.5$ ^{*3}	V
Power dissipation	P_{T}	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias	T_{bias}	−10 to +85	°C

- Notes: 1. Relative to V_{SS}
2. V_{T} min: −3.0 V for pulse half-width ≤ 50 ns
3. Maximum voltage is 4.6 V

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input high(logic 1) voltage	V_{IH}	2.0	—	$V_{\text{CC}}+0.3$	V
Input low(logic 0) voltage	V_{IL}	−0.3 ^{*1}	—	0.8	V

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 50 ns

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{SS} \leq V_{in} \leq V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{SS} \leq V_{I/O} \leq V_{CC}$
Operating power supply current (DC)	I_{CCDC1}	—	—	15	mA	$\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL} $I_{I/O} = 0\text{ mA}$
	I_{CCDC2}	—	—	10	mA	$\overline{CS} \leq 0.2\text{ V}$, $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $V_{IL} \leq 0.2\text{ V}$, $I_{I/O} = 0\text{ mA}$
Average operating power supply current	HM62W256-5 I_{CCAC1}	—	—	30	mA	min cycle, duty = 100 %, $\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL} $I_{I/O} = 0\text{ mA}$
	HM62W256-7 I_{CCAC1}	—	—	30		
	HM62W256-8 I_{CCAC1}	—	—	27		
	I_{CCAC2}	—	—	15	mA	Cycle time $\geq 1\text{ }\mu\text{s}$, duty = 100% $I_{I/O} = 0\text{ mA}$, $\overline{CS} \leq 0.2\text{ V}$, $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $V_{IL} \leq 0.2\text{ V}$
Standby powr supply current	I_{SB}	—	0.1	1	mA	$\overline{CS} = V_{IH}$
	I_{SB1}	—	0.1	50	μA	$V_{in} \geq 0\text{ V}$, $\overline{CS} \geq V_{CC} - 0.2\text{ V}$,
		—	0.1	10^{-2}		
		—	0.1	5^{-3}		
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.0\text{ mA}$
		—	—	0.2	V	$I_{OL} = 100\text{ }\mu\text{A}$
Output high voltage	V_{OH}	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100\text{ }\mu\text{A}$
		2.4	—	—	V	$I_{OH} = -2.0\text{ mA}$

- Notes: 1. Typical values are at $V_{CC} = 3.3\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.
2. This characteristic is guaranteed only for L-SL version.
3. This characteristic is guaranteed only for L-UL version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance ^{*1}	C_{in}	—	—	5	pF	$V_{in} = 0\text{ V}$
Input/output capacitance ^{*1}	$C_{I/O}$	—	—	8	pF	$V_{I/O} = 0\text{ V}$

- Note: 1. This parameter is sampled and not 100% tested.

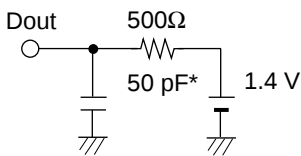
HM62W256 Series

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input reference level: 1.4 V
- Output timing reference level: HM62W256-5: 1.4 V
HM62W256-7/8: 0.8 V/2.0 V

Output Load



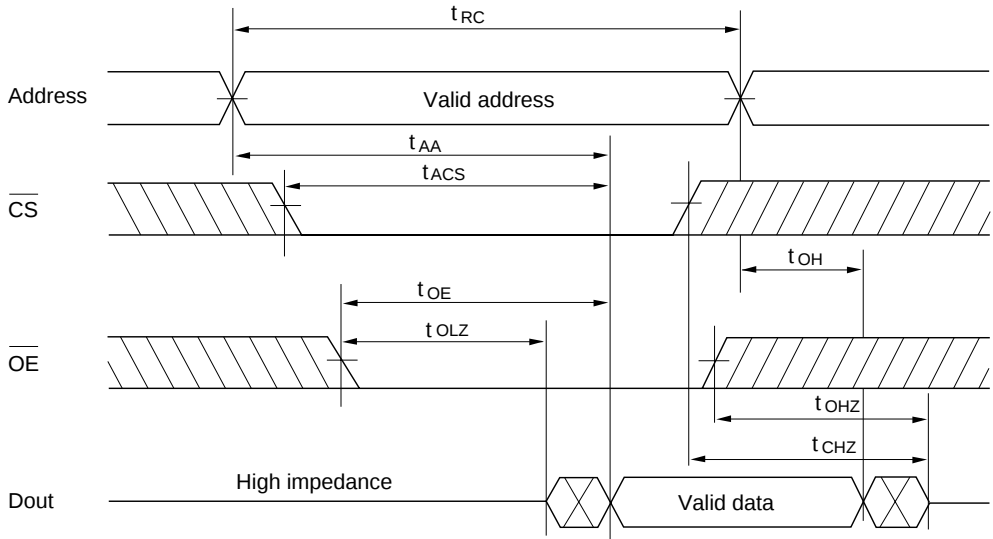
(Including scope & jig)

Read Cycle

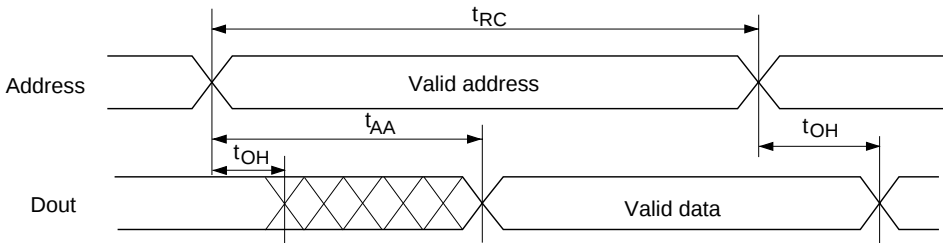
		HM62W256							
		-5		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	55	—	70	—	85	—	ns	
Address access time	t _{AA}	—	55	—	70	—	85	ns	
Chip select access time	t _{ACS}	—	55	—	70	—	85	ns	
Output enable to output valid	t _{OE}	—	30	—	35	—	45	ns	
Chip selection to output in low-Z	t _{CLZ}	5	—	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t _{CHZ}	0	20	0	25	0	30	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	0	30	ns	1, 2
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns	

- Notes: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.

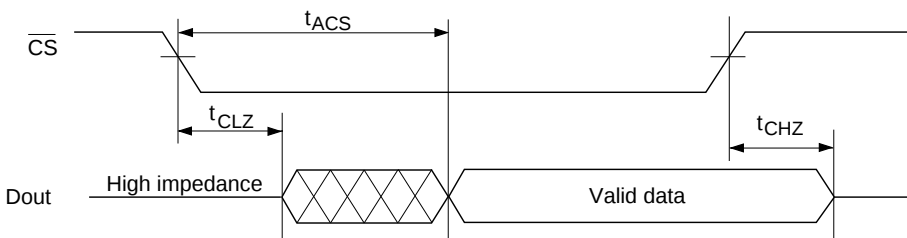
Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)



Read Timing Waveform (2) ($\overline{WE} = V_{IH}$, $\overline{CS} = V_{IL}$, $\overline{OE} = V_{IL}$)



Read Timing Waveform (3) ($\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$)*1



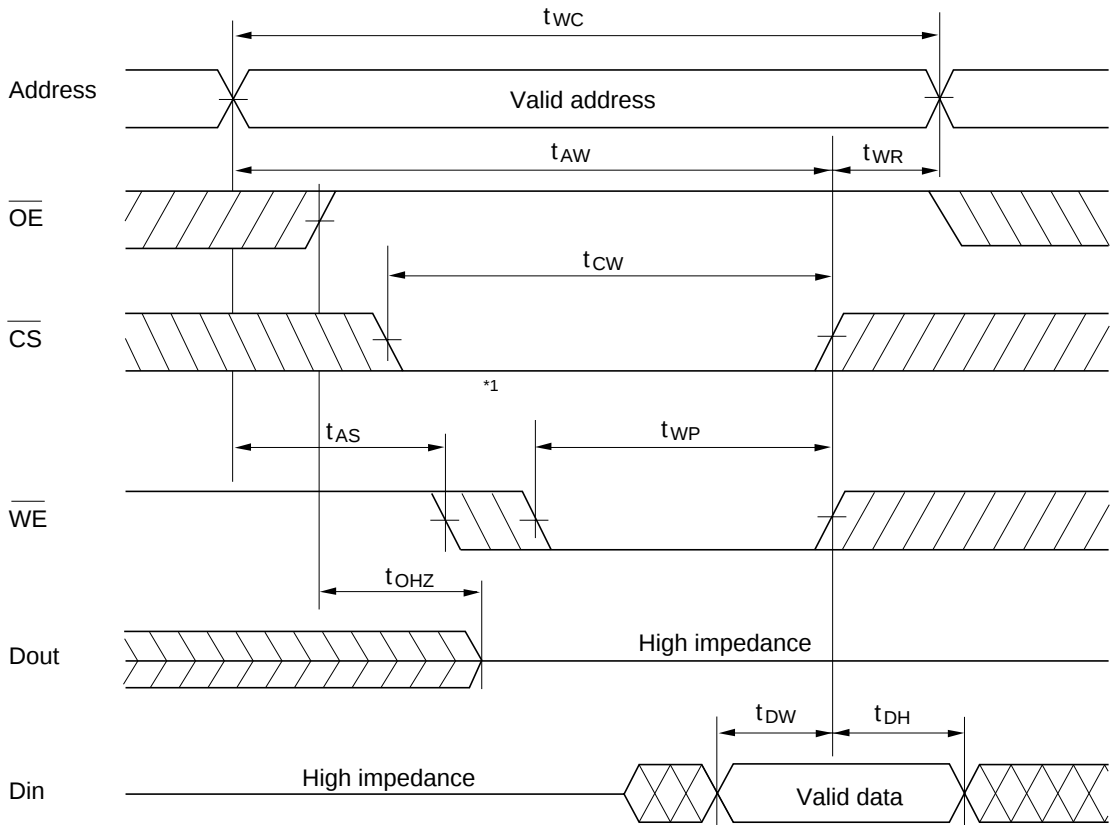
Note: 1. Address must be valid prior to or simultaneously with $\overline{CS}$ going low.

Write Cycle

		HM62W256							
		-5		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	55	—	70	—	85	—	ns	
Chip selection to end of write	t _{CW}	45	—	60	—	75	—	ns	4
Address setup time	t _{AS}	0	—	0	—	0	—	ns	5
Address valid to end of write	t _{AW}	45	—	60	—	75	—	ns	
Write pulse width	t _{WP}	40	—	50	—	55	—	ns	3, 8
Write recovery time	t _{WR}	0	—	0	—	0	—	ns	6
Write to output in high-Z	t _{WHZ}	0	25	0	25	0	30	ns	1, 2, 7
Data to write time overlap	t _{DW}	30	—	30	—	35	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t _{OW}	10	—	10	—	10	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	0	30	ns	1, 2, 7

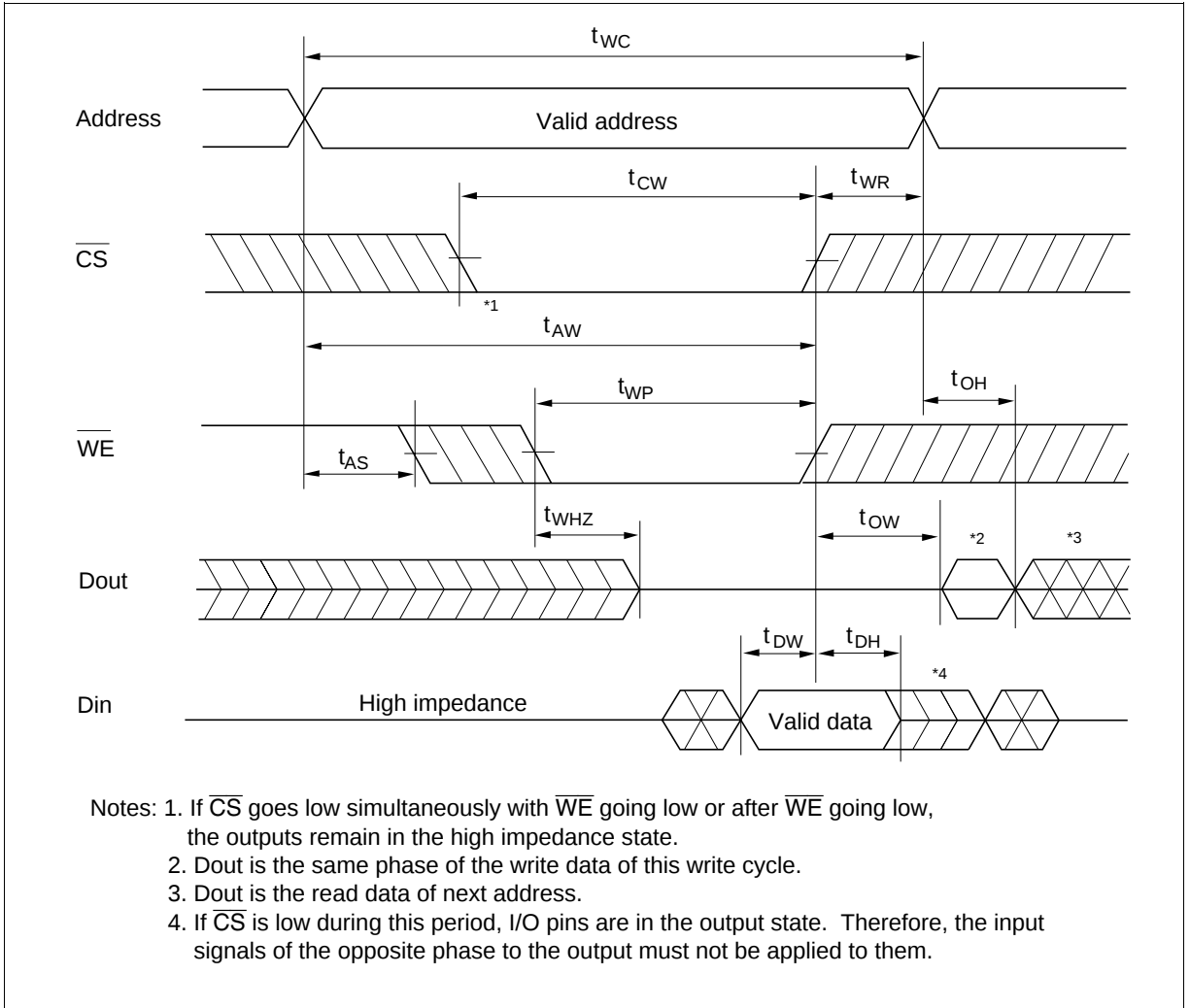
- Notes:
- t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - This parameter is samples and not 100% tested.
 - A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
 - t_{CW} is measured from $\overline{CS}$ going low to the end of write.
 - t_{AS} is measured from the address valid to the beginning of write.
 - t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
 - During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
 - In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention, t_{WP} ≥ t_{WHZ} max + t_{DW} min.

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Notes: 1. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in the high impedance state.

Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)

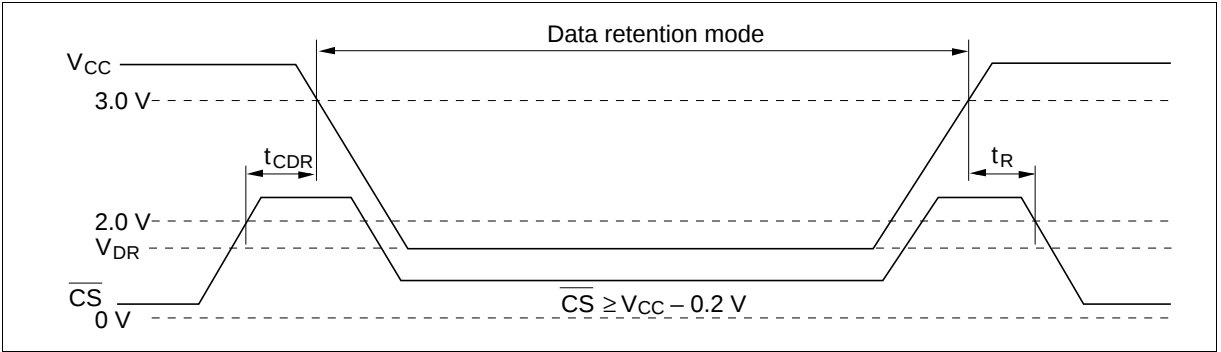


Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions* ⁶
V _{CC} for data retention	V _{DR}	2.0	—	3.6	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, $V_{in} \geq 0\text{ V}$
Data retention current	I _{CDDR}	—	0.05	30* ²	μA	$V_{CC} = 3.0\text{ V}$, $V_{in} \geq 0\text{ V}$ $\overline{CS} \geq V_{CC} - 0.2\text{ V}$,
		—	0.05	8* ³		
		—	0.05	3* ⁴		
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	t _{RC} * ⁵	—	—	ns	

- Notes:
- 1. Typical values are at V_{CC} = 3.0 V, Ta = 25°C and not guaranteed.
 - 2. 10 μA max. at Ta = 0 to +40°C.
 - 3. This characteristics guaranteed for only L-SL version. 2.5 μA max. at Ta = 0 to +40°C.
 - 4. This characteristics guaranteed for only L-UL version. 0.6 μA max. at Ta = 0 to +40°C.
 - 5. t_{RC} = read cycle time.
 - 6. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. If $\overline{CS}$ controls data retention mode, other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform

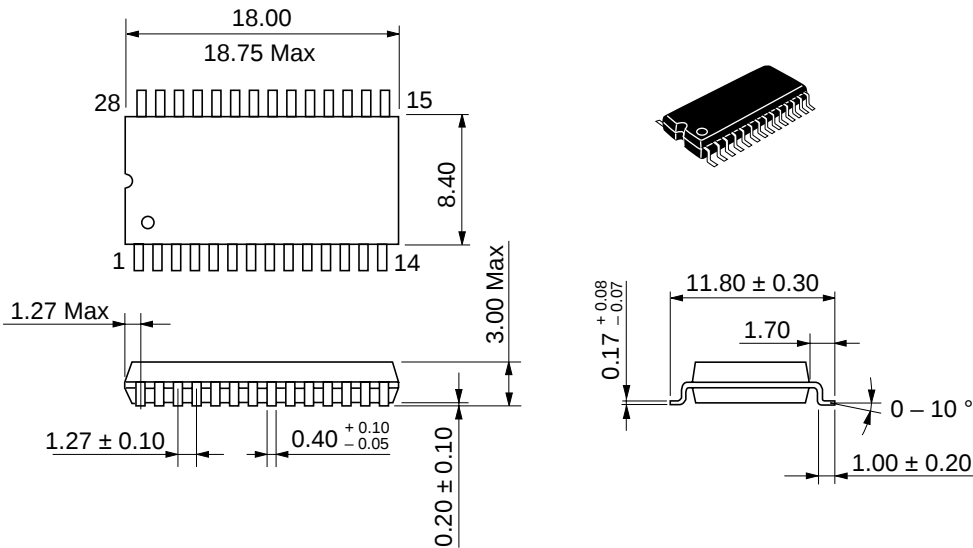


HM62W256 Series

Package Dimensions

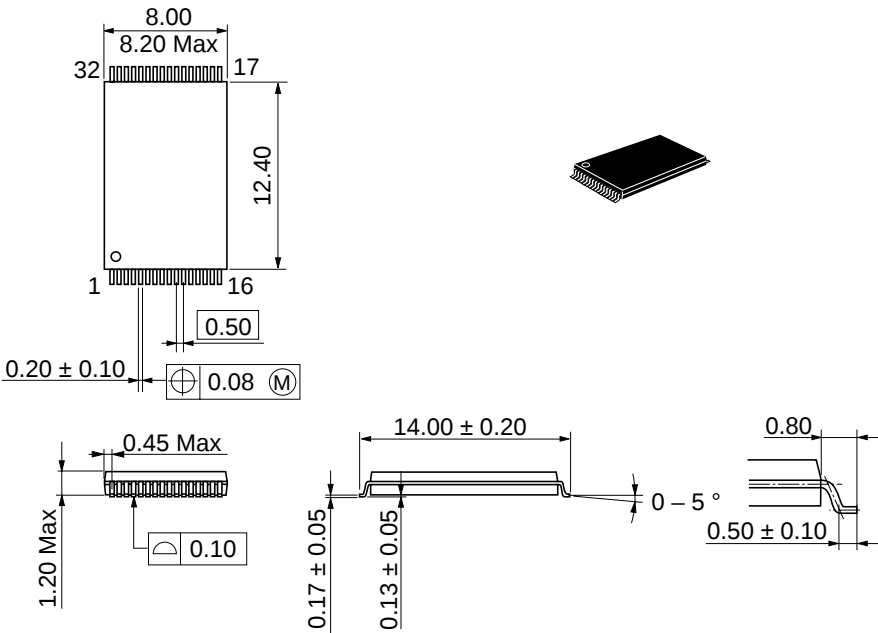
HM62W256LFP Series (FP-28DA)

Unit: mm



HM62W256LT Series (TFP-32DA)

Unit: mm



HM62W256LTM Series (TFP-28DA)

Unit: mm

