
HM62V8128B-SR Series

131,072-word $\times$ 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-597A (Z)

Rev. 1.0

Jan. 16, 1997

Description

The Hitachi HM62V8128B is a CMOS static RAM organized 131,072-word $\times$ 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μ m Hi-CMOS shrink process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 8 mm $\times$ 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting.

Features

- Single 3 V supply
- Fast access time: 120/150 ns (max)
- Power dissipation:
 - Active: 18 mW/MHz (typ)
 - Standby: 3 μ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output. Three state output
- Directry CMOS compatible all inputs and outputs.
- Capability of battery backup operation. 2 chip selection for battery backup

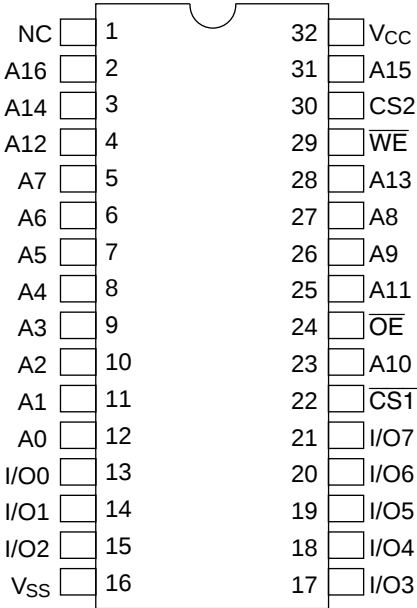
HM62V8128B-SR Series

Ordering Information

Type No.	Access Time	Package
HM62V8128BLFP-12SR	120 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62V8128BLFP-15SR	150 ns	
HM62V8128BLFP-12SRS	120 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62V8128BLFP-15SRS	150 ns	
HM62V8128BLT-12SR	120 ns	8 mm × 20 mm 32-pin plastic TSOP (normal-bend type) (TFP-32D)
HM62V8128BLT-15SR	150 ns	
HM62V8128BLT-12SRS	120 ns	8 mm × 20 mm 32-pin plastic TSOP (normal-bend type) (TFP-32D)
HM62V8128BLT-15SRS	150 ns	

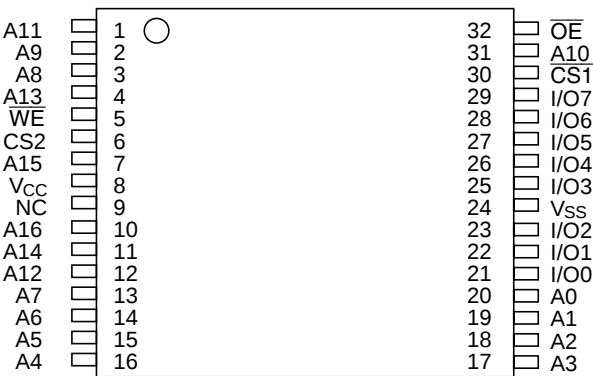
Pin Arrangement

HM62V8128BLFP Series



(Top view)

HM62V8128BLT Series (Normal Type TSOP)

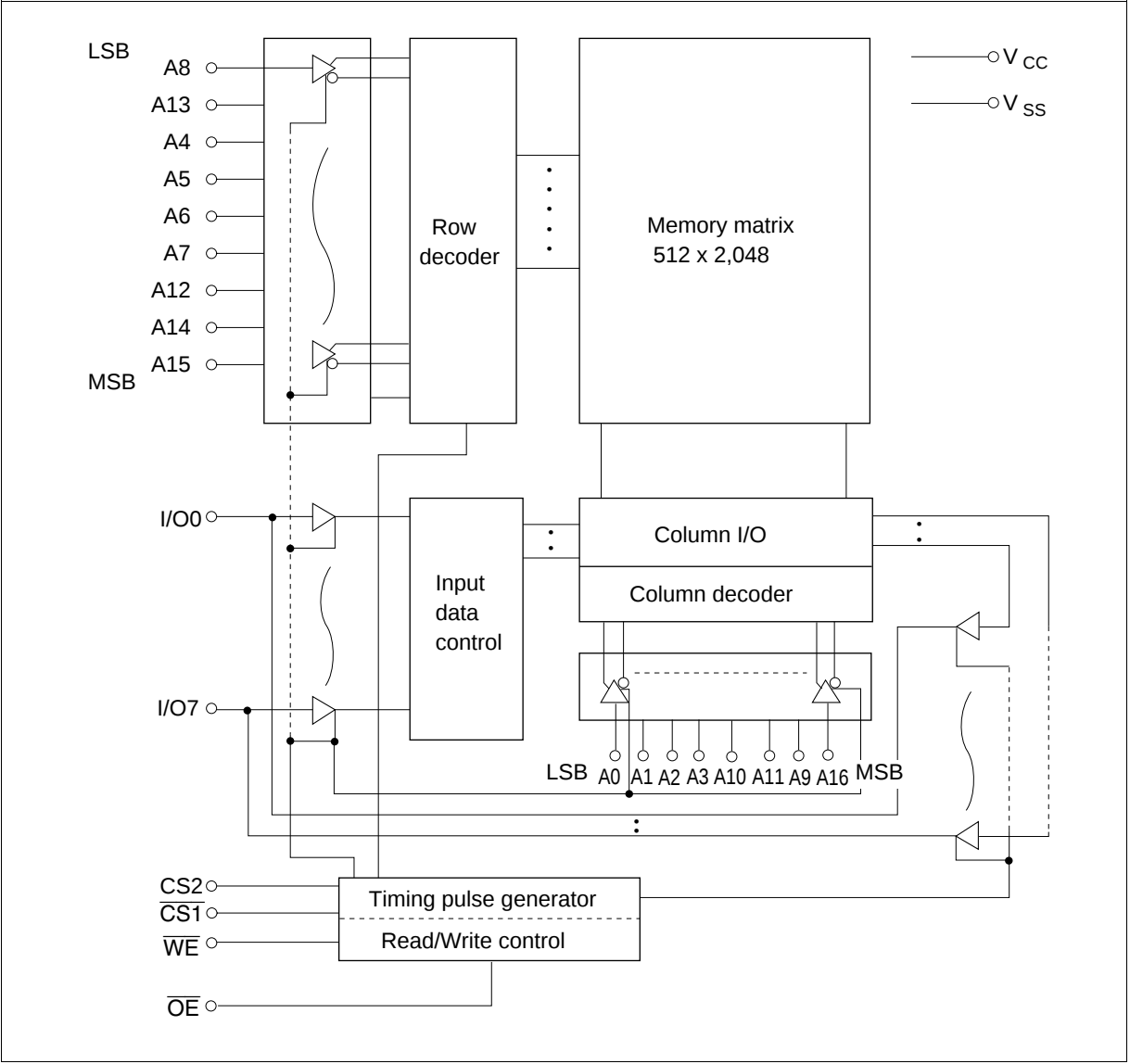


(Top view)

Pin Description

Pin Name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
NC	No connection
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

$\overline{\text{WE}}$	$\overline{\text{CS1}}$	CS2	$\overline{\text{OE}}$	Mode	V_{CC} current	I/O pin	Ref. cycle
x	H	x	x	Standby	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
x	x	L	x	Standby	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: x: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage*1	V_{CC}	−0.5 to + 4.6	V
Terminal voltage*1	V_{T}	−0.5*2 to $V_{\text{CC}} + 0.3$ *3	V
Power dissipation	P_{T}	1.0	W
Operating temperature	T_{opr}	−20 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias	T_{bias}	−20 to +85	°C

- Notes: 1. Relative to V_{SS}
2. V_{T} min: −3.0 V for pulse half-width ≤ 30 ns
3. Maximum voltage is 4.6 V

Recommended DC Operating Conditions ($T_{\text{a}} = -20$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	$0.7 \times V_{\text{CC}}$	—	$V_{\text{CC}} + 0.3$	V
	V_{IL}	−0.3 *1	—	$0.2 \times V_{\text{CC}}$	V

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 30 ns

HM62V8128B-SR Series

DC Characteristics (Ta = -20 to +70°C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS1} = V_{IH}$ or CS2 = V _{IL} or OE = V _{IH} or WE = V _{IL} , V _{I/O} = V _{SS} to V _{CC}
Operating power supply current: DC	I _{CC}	—	5	10	mA	CS1 = V _{IL} , CS2 = V _{IH} , Others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
Operating power supply current	I _{CC1}	—	15	25	mA	Min cycle, duty = 100%, I _{I/O} = 0 mA, $\overline{CS1} = V_{IL}$, CS2 = V _{IH} , Others = V _{IH} /V _{IL}
	I _{CC2}	—	6	10	mA	Cycle time = 1 μs, duty = 100%, I _{I/O} = 0 mA, CS1 ≤ 0.2 V, CS2 ≥ V _{CC} - 0.2 V V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V
Standby power supply current: DC	I _{SB}	—	0.5	1	mA	(1) $\overline{CS1} = V_{IH}$, CS2 = V _{IH} or (2) CS2 = V _{IL}
Standby power supply current (1): DC	I _{SB1}	—	1* ²	70* ²	μA	0 V ≤ V _{in} (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS1} \geq V_{CC} - 0.2 V$, CS2 ≥ V _{CC} - 0.2 V
	I _{SB1}	—	1* ³	30* ³	μA	
Output voltage	V _{OL}	—	—	0.2	V	I _{OL} = 100 μA
	V _{OH}	V _{CC} - 0.2	—	—	V	I _{OH} = -100 μA

- Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
2. This characteristic is guaranteed only for L-SR version.
3. This characteristic is guaranteed only for L-SRS version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

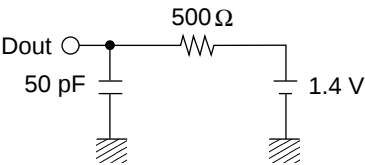
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance* ¹	C _{in}	—	—	8	pF	V _{in} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = -20 to +70°C, V_{CC} = 2.7 V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.4 V
- Output load (Including scope and jig)



Read Cycle

		HM62V8128B					
		-12SR		-15SR			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	120	—	150	—	ns	
Address access time	t _{AA}	—	120	—	150	ns	
Chip selection to output valid	t _{CO1}	—	120	—	150	ns	
	t _{CO2}	—	120	—	150	ns	
Output enable to output valid	t _{OE}	—	60	—	75	ns	
Chip selection to output in low-Z	t _{LZ1}	10	—	15	—	ns	2, 3
	t _{LZ2}	10	—	15	—	ns	
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t _{HZ1}	0	40	0	45	ns	1, 2, 3
	t _{HZ2}	0	40	0	45	ns	
Output disable to output in high-Z	t _{OHZ}	0	40	0	45	ns	1, 2, 3
Output hold from address change	t _{OH}	10	—	10	—	ns	

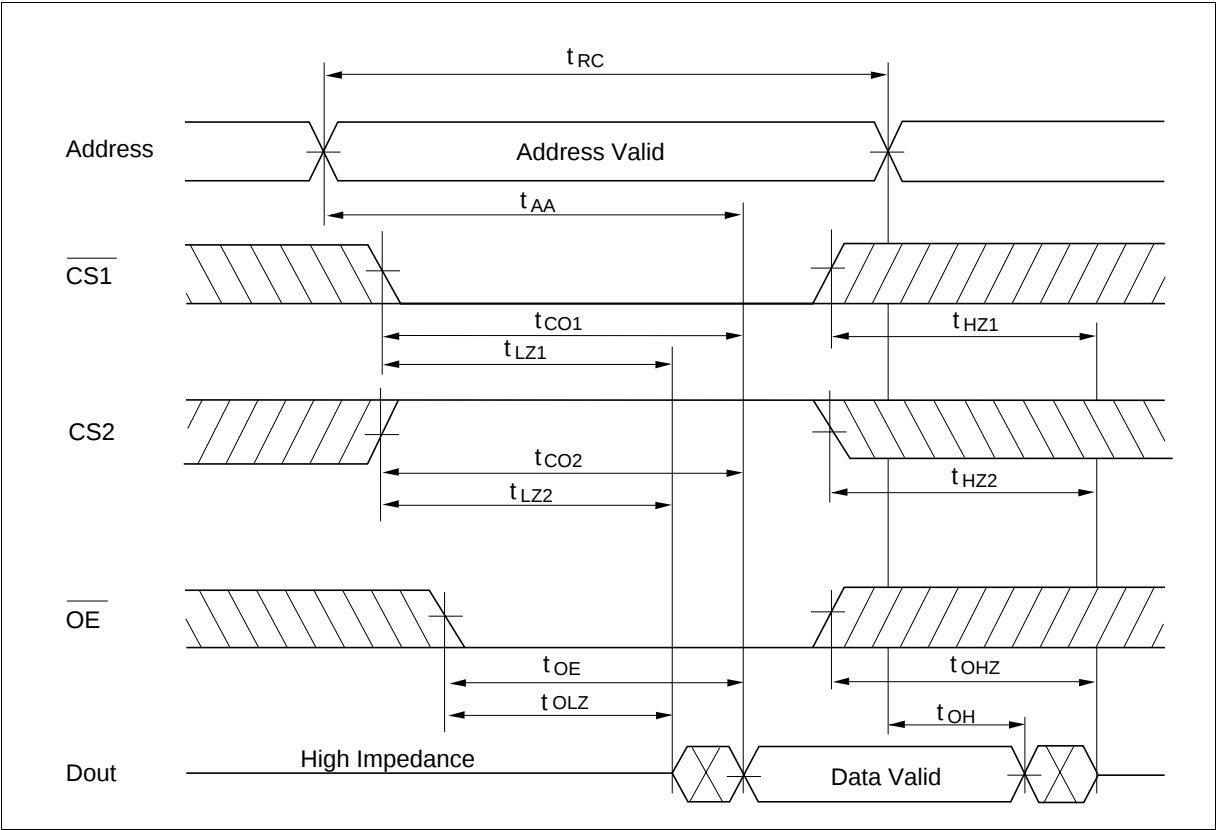
Write Cycle

		HM62V8128B					
		-12SR		-15SR			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	120	—	150	—	ns	
Chip selection to end of write	t _{CW}	85	—	90	—	ns	5
Address setup time	t _{AS}	0	—	0	—	ns	6
Address valid to end of write	t _{AW}	85	—	90	—	ns	
Write pulse width	t _{WP}	65	—	70	—	ns	4, 13
Write recovery time	t _{WR}	0	—	0	—	ns	7
Write to output in high-Z	t _{WHZ}	0	40	0	45	ns	1, 2, 8
Data to write time overlap	t _{DW}	45	—	50	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	ns	
Output active from end of write	t _{OW}	5	—	5	—	ns	2
Output disable to output in High-Z	t _{OHZ}	0	40	0	45	ns	1, 2, 8

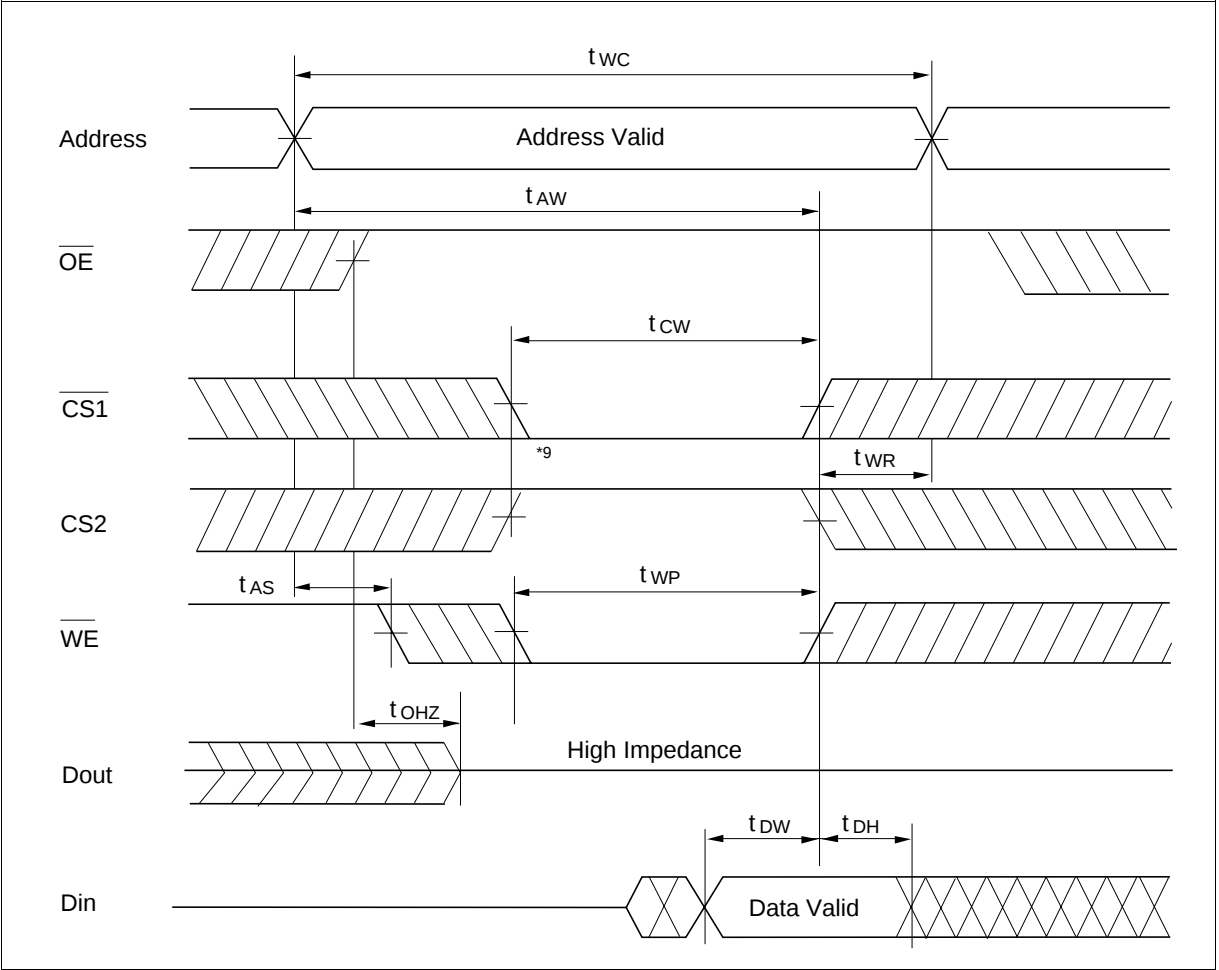
- Notes:
1. t_{HIZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 4. A write occurs during the overlap of a low CS1, a high CS2, and a low WE. A write begins at the latest transition among CS1 going low, CS2 going high, and WE going low. A write ends at the earliest transition among CS1 going high, CS2 going low, and WE going high. t_{WP} is measured from the beginning of write to the end of write.
 5. t_{CW} is measured from the later of CS1 going low or CS2 going high to the end of write.
 6. t_{AS} is measured from the address valid to the beginning of write.
 7. t_{WR} is measured from the earliest of CS1 or WE going high or CS2 going low to the end of write cycle.
 8. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
 9. If CS1 goes low simultaneously with WE going low or after WE going low, the outputs remain in a high impedance state.
 10. Dout is the same phase of the latest written data in this write cycle.
 11. Dout is the read data of next address.
 12. If CS1 is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
 13. In the write cycle with OE low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention.
$$t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$$

Timing Waveform

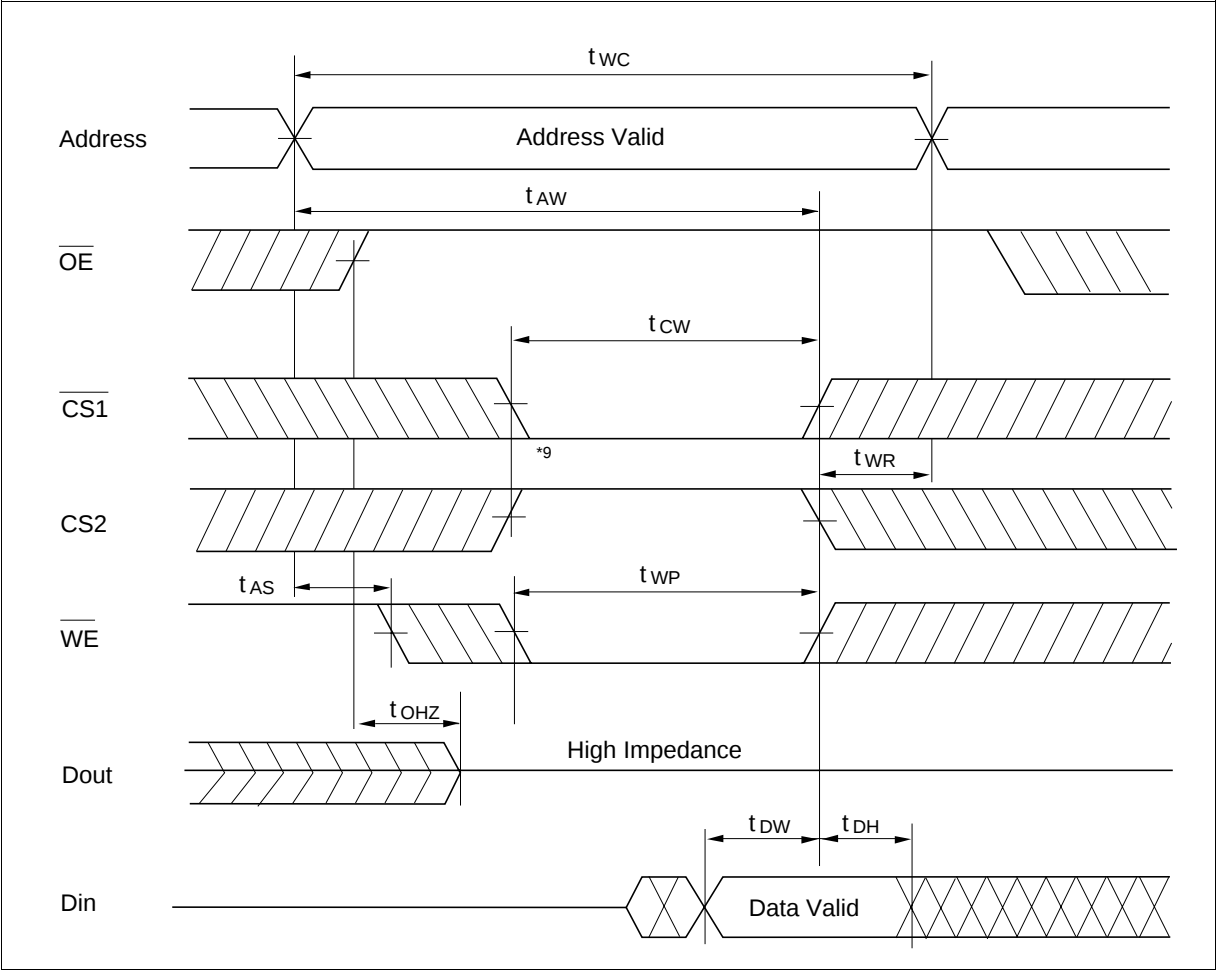
Read Timing Waveform (WE = V_{IH})



Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)

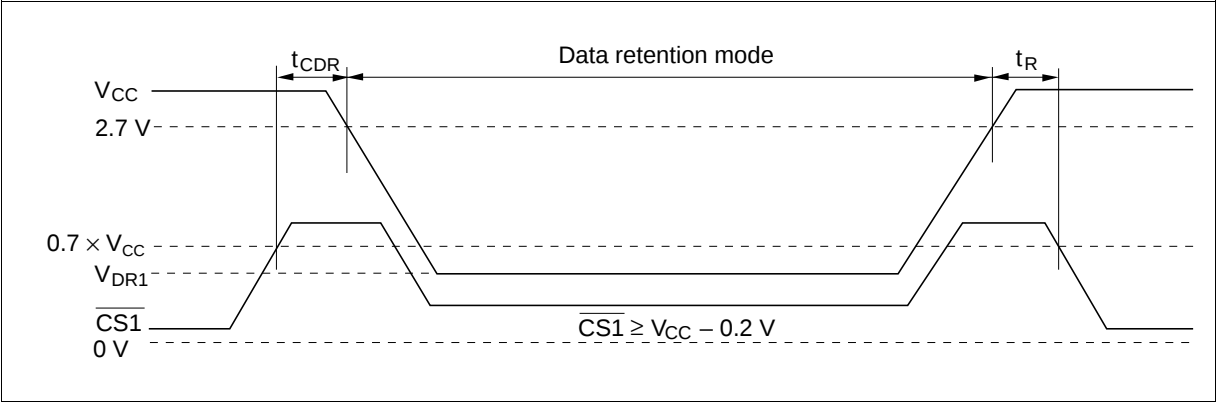


Low V_{CC} Data Retention Characteristics (Ta = -20 to +70°C)

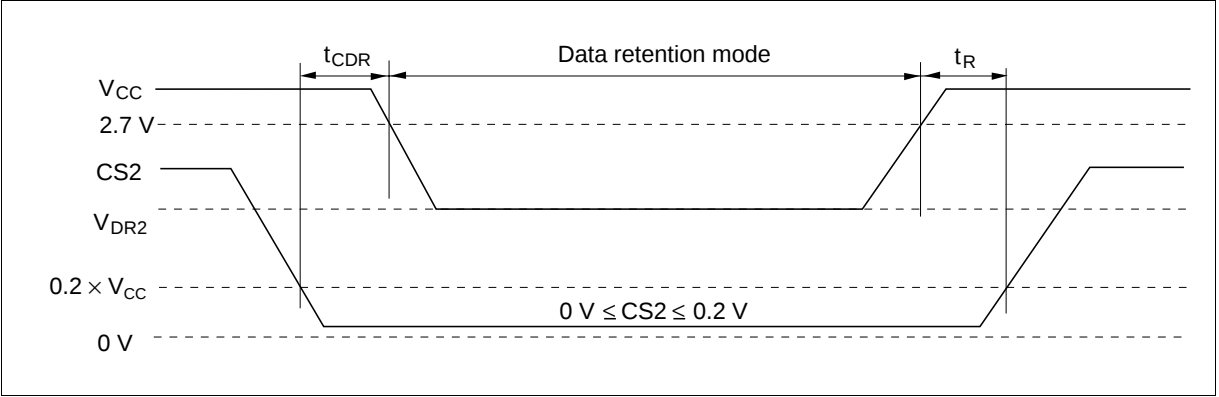
Parameter	Symbol	Min	Typ ^{*5}	Max	Unit	Test conditions ^{*3}
V _{CC} for data retention	V _{DR}	2.0	—	—	V	Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{CC} - 0.2 V CS1 ≥ V _{CC} - 0.2 V
Data retention current	I _{CDDR} (L-SR version)	—	1	50 ^{*1}	μA	V _{CC} = 3.0 V, Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{CC} - 0.2 V, CS1 ≥ V _{CC} - 0.2 V
	I _{CDDR} (L-SRS version)	—	1	15 ^{*2}	μA	
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	5 ^{*4}	—	—	ms	

- Notes:
1. This characteristic is guaranteed only for L-SR version, 20 μA max. at Ta = -20 to 40°C.
 2. This characteristic is guaranteed only for L-SRS version, 3 μA max. at Ta = -20 to 40°C.
 3. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} - 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.
 4. V_{CC} rising time must be more 50 ms. When V_{CC} rising time is less than 50 ms, t_R must be 50 ms or more.
 5. Typical values are at V_{CC} = +3.0 V, Ta = +25°C and not guaranteed.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)

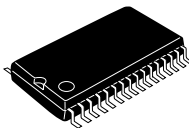


Low V_{CC} Data Retention Timing Waveform (2) ($CS2$ Controlled)



Package Dimensions

Unit: mm



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Aug. 9, 1996	Initial issue	M. Higuchi	K. Imato
1.0	Jan. 16, 1997	Features Active: 21 mW/MHz(typ) to 18 mW/MHz(typ) DC Characteristics I _{CC} typ: 6 mA to 5 mA I _{CC1} typ: 20 mA to 15 mA I _{CC2} typ: 7 mA to 6 mA		