

HM621664HB Series

65536-word $\times$ 16-bit High Speed CMOS Static RAM

HITACHI

ADE-203-349A(Z)

Rev. 1.0

Sep. 11, 1996

Description

The HM621664HB is an asynchronous high speed static RAM organized as 64-kword $\times$ 16-bit. It realize high speed access time (15/20 ns) with employing 0.8 μ m CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The HM621664HB is packaged in 400-mil 44-pin SOJ for high density surface mounting.

Features

- Single 5 V supply
- Access time: 15/20 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- 400-mil 44-pin SOJ package
- Center V_{CC} and V_{SS} type pinout

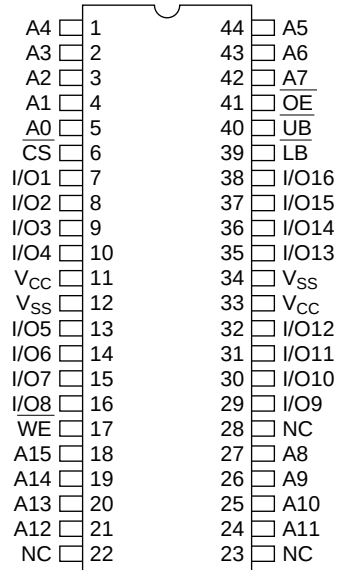
Ordering Information

Type No.	Access time	Package
HM621664HBJP-15	15 ns	400-mil 44-pin plastic SOJ (CP-44D)
HM621664HBJP-20	20 ns	
HM621664HBLJP-15	15 ns	
HM621664HBLJP-20	20 ns	

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Pin Arrangement

HM621664HBJP/HBLJP Series

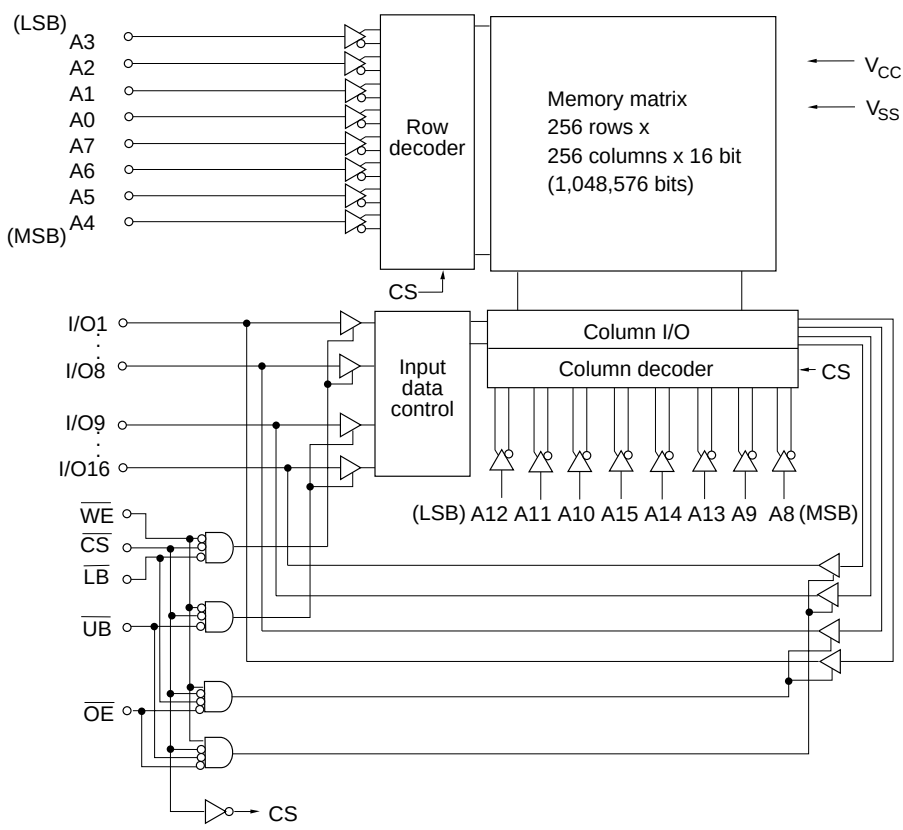


(Top View)

Pin Description

Pin name	Function
A0 – A15	Address input
I/O1 – I/O16	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
UB	Upper byte select
LB	Lower byte select
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



Function Table

CS	OE	WE	LB	UB	Mode	V _{CC} current	I/O1–I/O8	I/O9–I/O16	Ref. cycle
H	x	x	x	x	Standby	I _{SB} , I _{SB1}	High-Z	High-Z	—
L	H	H	x	x	Output disable	I _{CC}	High-Z	High-Z	—
L	L	H	L	L	Read	I _{CC}	Output	Output	Read cycle
L	L	H	L	H	Lower byte read	I _{CC}	Output	High-Z	Read cycle
L	L	H	H	L	Upper byte read	I _{CC}	High-Z	Output	Read cycle
L	L	H	H	H	—	I _{CC}	High-Z	High-Z	—
L	x	L	L	L	Write	I _{CC}	Input	Input	Write cycle
L	x	L	L	H	Lower byte write	I _{CC}	Input	High-Z	Write cycle
L	x	L	H	L	Upper byte write	I _{CC}	High-Z	Input	Write cycle
L	x	L	H	H	—	I _{CC}	High-Z	High-Z	—

Note: x: H or L

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V _{SS}	V _{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V _{SS}	V _T	−0.5* ¹ to V _{CC} + 0.5	V
Power dissipation	P _T	1.0* ² /1.5* ³	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Notes: 1. V_T (min) = −2.5 V for pulse width (under shoot) ≤ 10 ns
2. At still air condition
3. At air flow ≥ 1.0 m/s

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC} * ²	4.5	5.0	5.5	V
	V _{SS} * ³	0	0	0	V
Input voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
	V _{IL}	−0.5* ¹	—	0.8	V

Notes: 1. −2.0 V for pulse width (under shoot) ≤ 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

Parameter		Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current		$ I_{Li} $	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current* ¹		$ I_{Lo} $	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Operating power supply current	15 ns cycle	I_{CC}	—	160	180	mA	$\overline{CS} = V_{IL}$, $I_{out} = 0\text{ mA}$ Other inputs = V_{IH}/V_{IL}
	20 ns cycle	I_{CC}	—	130	150		
Standby power supply current	15 ns cycle	I_{SB}	—	55	100	mA	$\overline{CS} = V_{IH}$, Other inputs = V_{IH}/V_{IL}
	20 ns cycle	I_{SB}	—	45	80		
		I_{SB1}	—	—	2	mA	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2\text{ V}$, (1) $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2\text{ V}$
			—* ²	—* ²	0.2* ²		
Output voltage		V_{OL}	—	—	0.4	V	$I_{OL} = 8\text{ mA}$
		V_{OH}	2.4	—	—	V	$I_{OH} = -4\text{ mA}$

Note: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading.
2. This characteristics is guaranteed only for L-version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹		C_{in}	—	—	6	pF	$V_{in} = 0\text{ V}$
Input/output capacitance* ¹		$C_{I/O}$	—	—	8	pF	$V_{I/O} = 0\text{ V}$

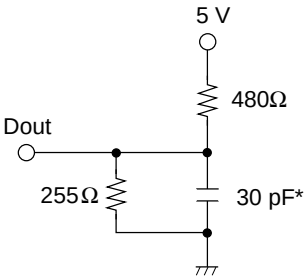
Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics (Ta = 0 to +70°C, VCC = 5 V ± 10%, unless otherwise noted.)

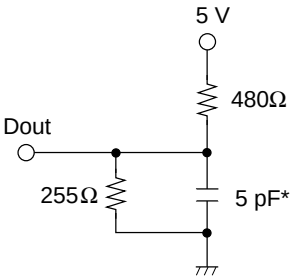
Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)

*Including scope and jig



Output load (B)

(for tCLZ, tOLZ, tLBLZ, tUBLZ, tCHZ, tOHZ, tLBHZ, tUBHZ, tWHZ, and tOW)

Read Cycle

Parameter	Symbol	HM621664HB -15 HM621664HB -20				Unit	Notes
		Min	Max	Min	Max		
Read cycle time	tRC	15	—	20	—	ns	
Address access time	tAA	—	15	—	20	ns	
Chip select access time	tACS	—	15	—	20	ns	
Output enable to output valid	tOE	—	8	—	10	ns	
Byte select to output valid	tLB, tUB	—	8	—	10	ns	
Output hold from address change	tOH	5	—	5	—	ns	
Chip select to output in low-Z	tCLZ	3	—	3	—	ns	1
Output enable to output in low-Z	tOLZ	1	—	1	—	ns	1
Byte select to output in low-Z	tLBLZ, tUBLZ	1	—	1	—	ns	1
Chip deselect to output in high-Z	tCHZ	—	7	—	7	ns	1
Output disable to output in high-Z	tOHZ	—	7	—	7	ns	1
Byte deselect to output in high-Z	tLBHZ, tUBHZ	—	7	—	7	ns	1

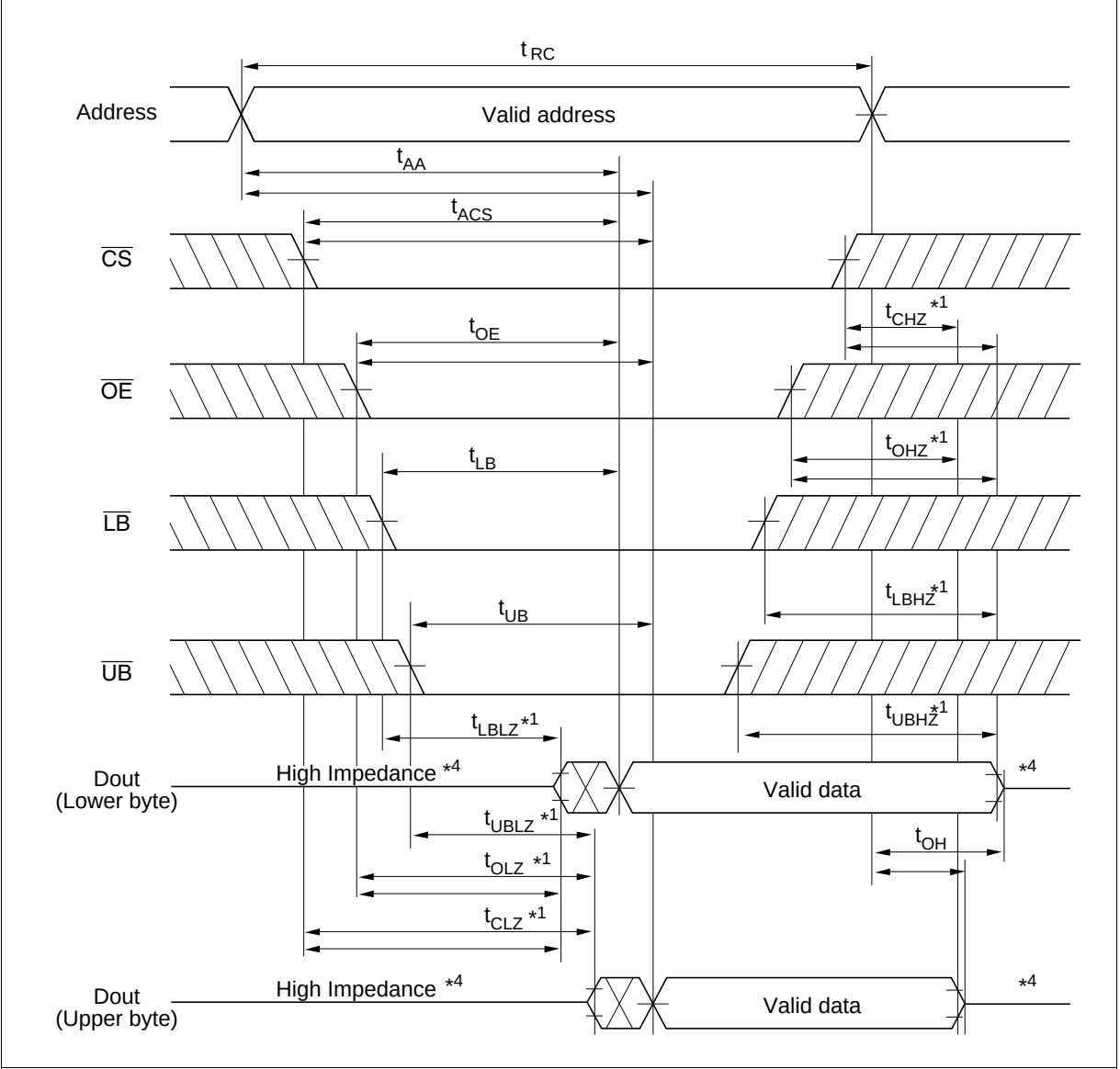
Write Cycle

Parameter	Symbol	HM621664HB -15 HM621664HB -20				Unit	Notes
		Min	Max	Min	Max		
Write cycle time	t_{WC}	15	—	20	—	ns	
Address valid to end of write	t_{AW}	12	—	15	—	ns	
Chip select to end of write	t_{CW}	10	—	12	—	ns	8
Write pulse width	t_{WP}	10	—	12	—	ns	7
Byte select to end of write	t_{LBW}, t_{UBW}	10	—	12	—	ns	9, 10
Address setup time	t_{AS}	0	—	0	—	ns	5
Write recovery time	t_{WR}	0	—	0	—	ns	6
Data to write time overlap	t_{DW}	8	—	10	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	7	—	7	ns	1
Write enable to output in high-Z	t_{WHZ}	—	7	—	7	ns	1

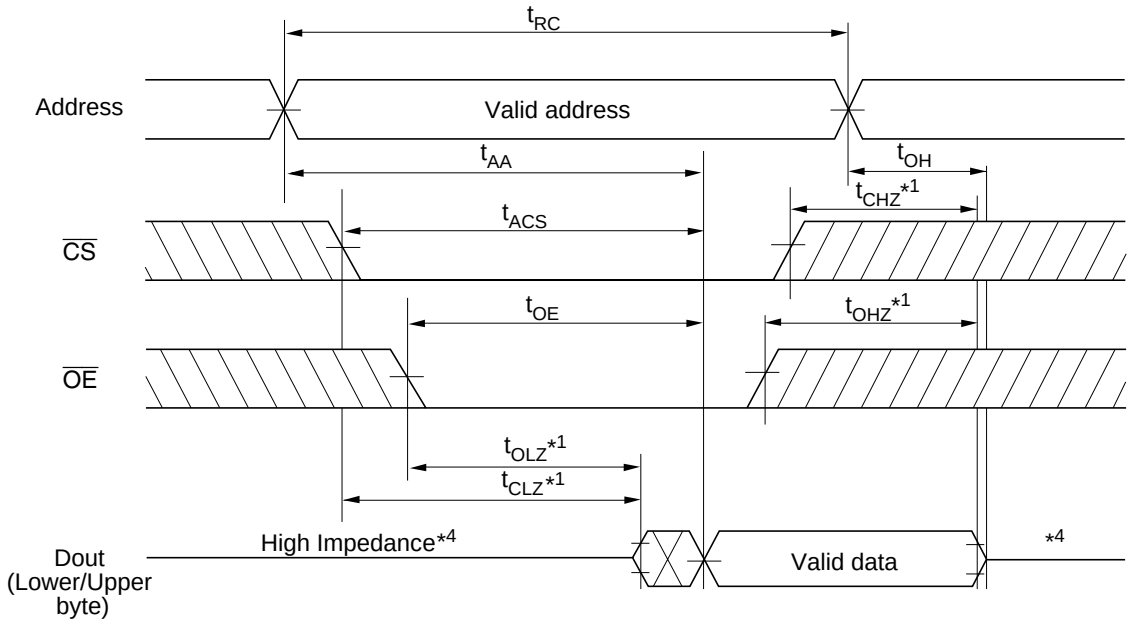
- Notes: 1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
2. If the $\overline{CS}$ or $\overline{LB}$ or $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.
3. $\overline{WE}$ and/or $\overline{CS}$ must be high during address transition time.
4. If $\overline{CS}$, $\overline{OE}$, $\overline{LB}$ and $\overline{UB}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
5. t_{AS} is measured from the latest address transition to the latest of $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ going low.
6. t_{WR} is measured from the earliest of $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ going high to the first address transition.
7. A write occurs during the overlap of low $\overline{CS}$, low $\overline{WE}$ and low $\overline{LB}$ or low $\overline{UB}$.
8. t_{CW} is measured from the later of $\overline{CS}$ going low to the end of write.
9. t_{LBW} is measured from the later of $\overline{LB}$ going low to the end of write.
10. t_{UBW} is measured from the later of $\overline{UB}$ going low to the end of write.

Timing Waveforms

Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)

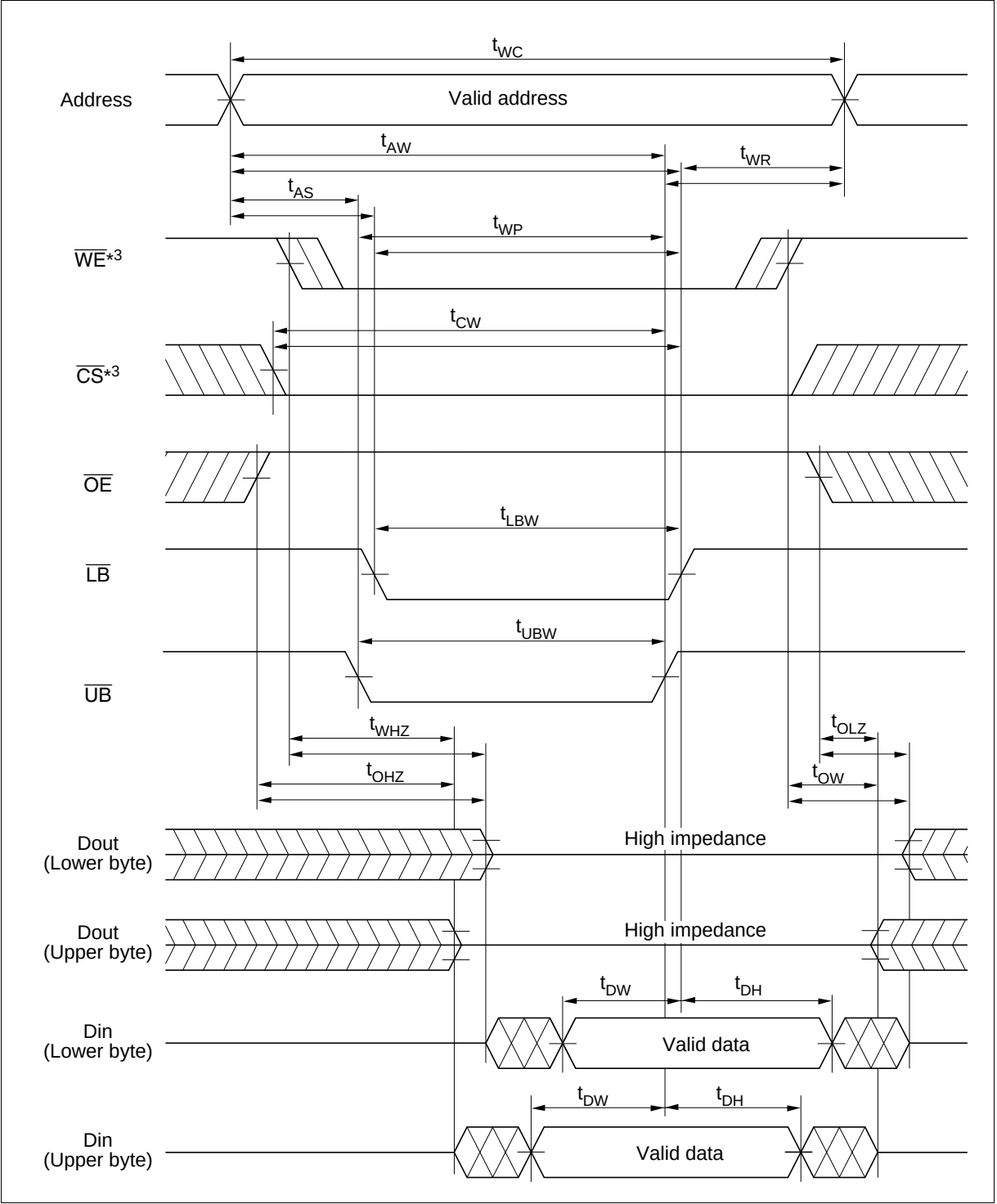


Read Timing Waveform (2) ($\overline{WE} = V_{IH}$, $\overline{LB} = V_{IL}$, $\overline{UB} = V_{IL}$)

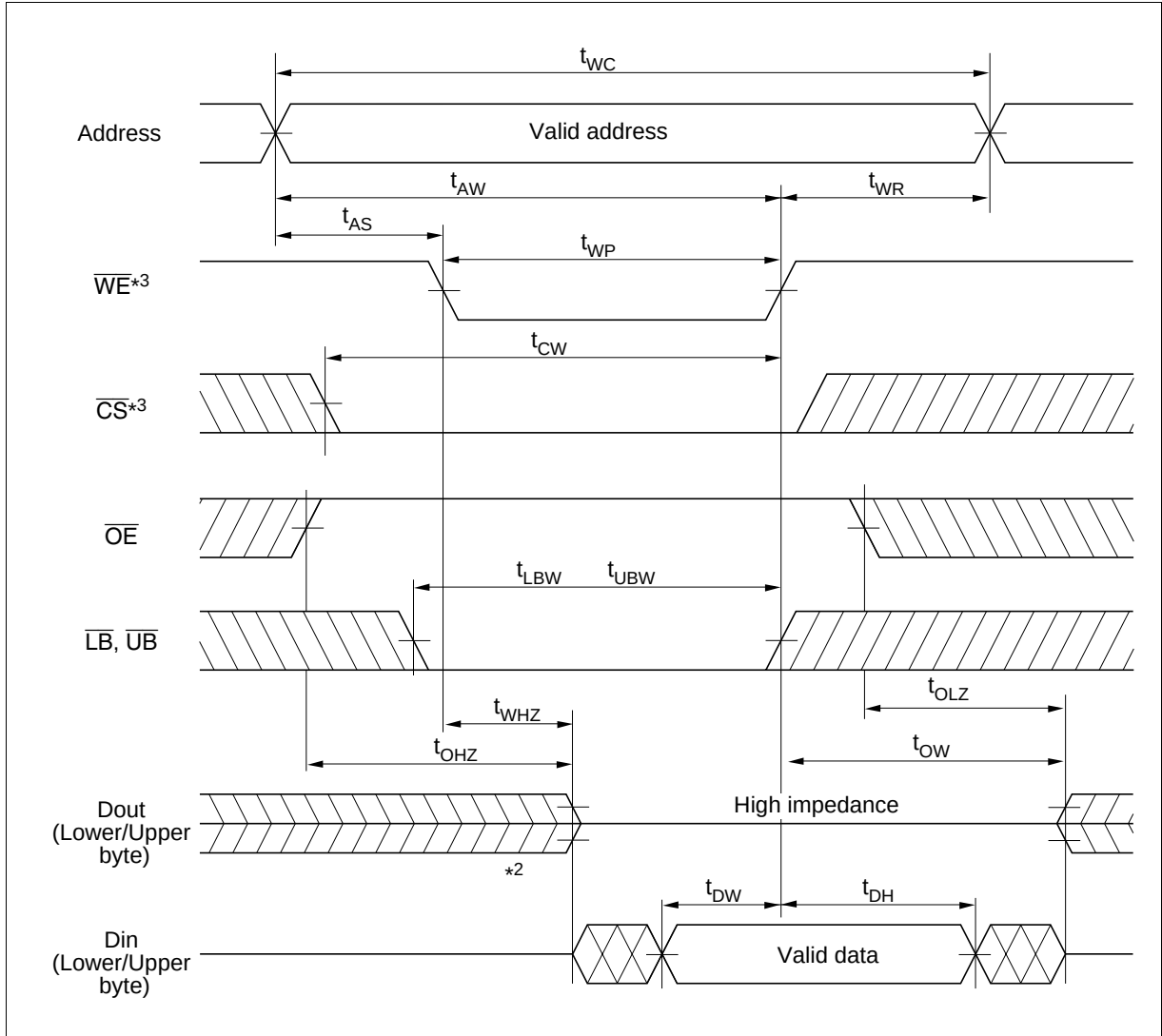


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Write Timing Waveform (1) ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled)

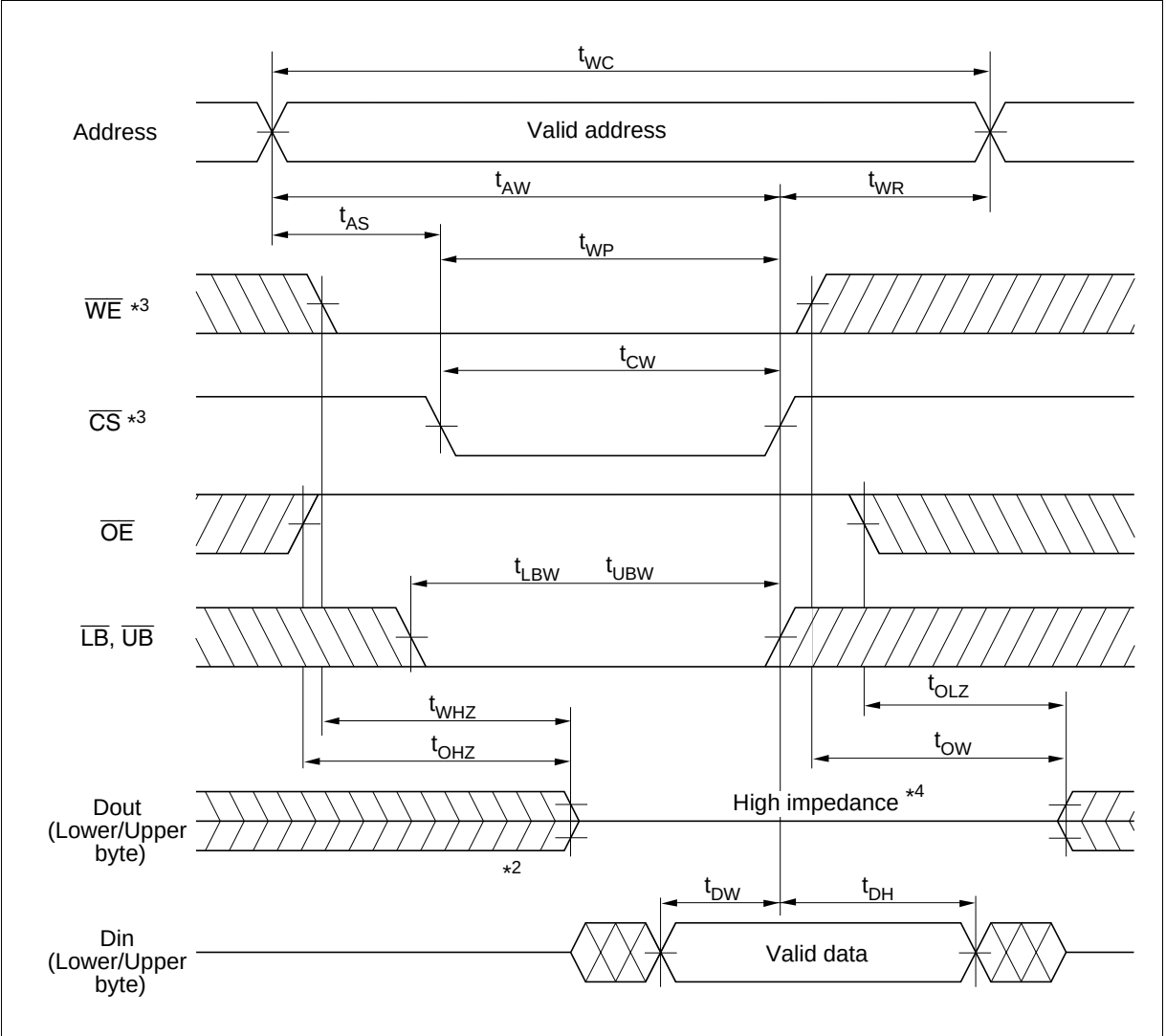


Write Timing Waveform (2) ($\overline{\text{WE}}$ Controlled)



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Write Timing Waveform (3) ($\overline{\text{CS}}$ Controlled)



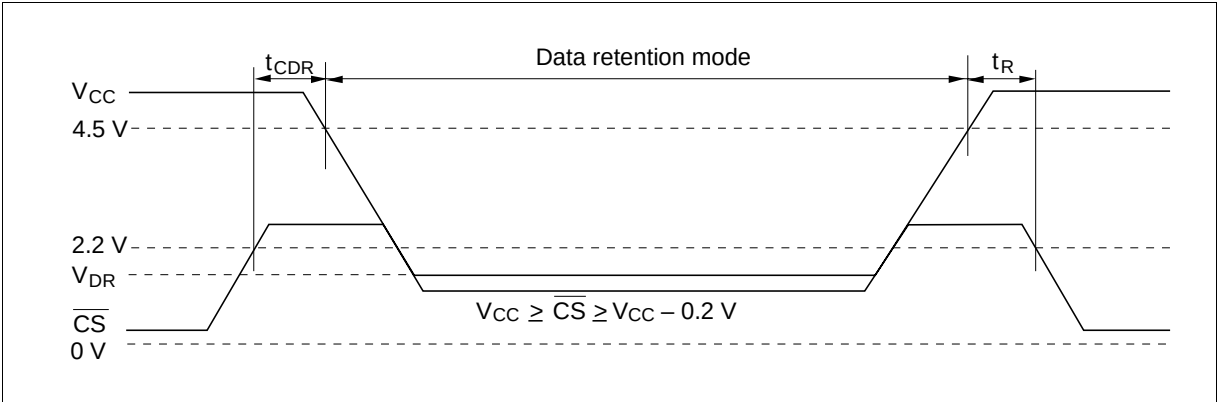
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
V _{CC} for data retention	V _{DR}	2.0	—	—	V	V _{CC} ≥ $\overline{\text{CS}}$ ≥ V _{CC} − 0.2 V, (1) 0 V ≤ Vin ≤ 0.2 V or (2) V _{CC} ≥ Vin ≥ V _{CC} − 0.2 V
Data retention current	I _{CCDR}	—	2	80	μA	V _{CC} = 3 V V _{CC} ≥ $\overline{\text{CS}}$ ≥ V _{CC} − 0.2 V, (1) 0 V ≤ Vin ≤ 0.2 V or (2) V _{CC} ≥ Vin ≥ V _{CC} − 0.2 V
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	5	—	—	ms	

Note: 1. Typical values are at V_{CC} = 3.0 V, Ta = 25°C, and not guaranteed.

Low V_{CC} Data Retention Timing Waveform

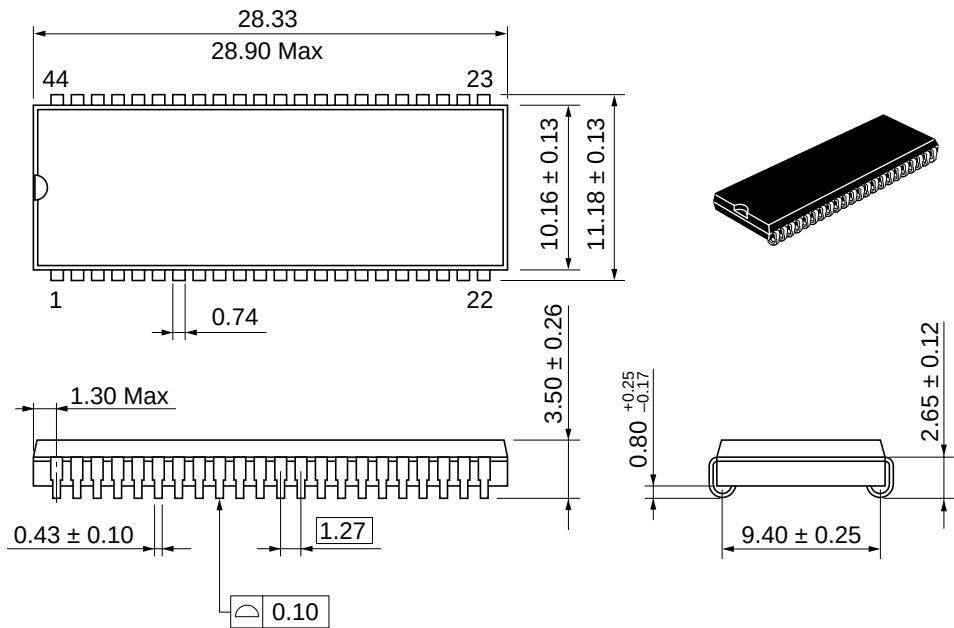


HM621664HB Series

Package Dimensions

HM621664HBJP/HBLJP Series (CP-44D)

Unit: mm



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jan. 23, 1995	Initial issue	K. Makuta	Y. Kinoshita
0.1	Jun. 28, 1996	Change of format Deletion of HM621664-12 Series Change of Bloc Diagram Function Table Addition of Mode Parameter Recommended DC Operating Condition Change of note 2. Addition of note 3. DC Characteristics Addition of note 2 AC Characteristics Change order of notes Change of Timing Waveform Addition of Read Timing Waveform (2)	Y. Saito	A. Ide
1.0	Sep. 11, 1996	DC Characteristics ICC (max) -15: 220 mA to 180 mA 170 mA to 150 mA		
