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# HN58S256A Series

32768-word  $\times$  8-bit Electrically Erasable and Programmable  
CMOS ROM

# HITACHI

ADE-203-692 (Z)

Preliminary

Rev. 0.0

Dec. 3, 1996

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## Description

The Hitachi HN58S256A is a electrically erasable and programmable EEPROM's organized as 32768-word  $\times$  8-bit employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 64-byte page programming function to make the write operations faster.

## Features

- Single 2.2 to 3.6 V supply
- On-chip latches: address, data,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{WE}}$
- Automatic byte write: 15 ms (max)
- Automatic page write (64 bytes): 15 ms (max)
- Fast access time: 150 ns (max)/200 ns (max)
- Low power dissipation: active: 10 mW/MHz, (typ)  
standby: 36  $\mu$ W (max)
- $\overline{\text{Data}}$  polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- $10^5$  erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Industrial versions (Temperature range:  $-40$  to  $85^\circ\text{C}$ ) are also available.

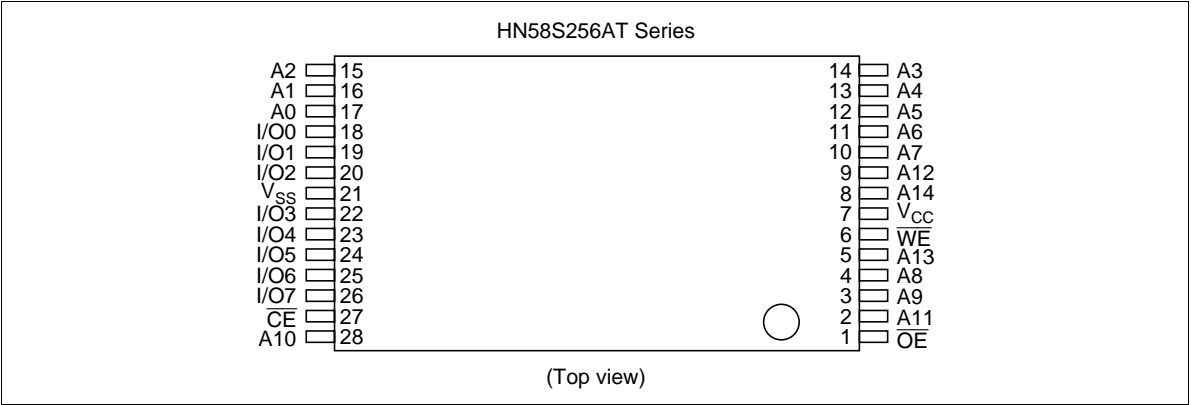
Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

# HN58S256A Series

## Ordering Information

Type No.	Access time	Package
HN58S256AT-15	150 ns	28-pin plastic TSOP (TFP-28DB)
HN58S256AT-20	200 ns	

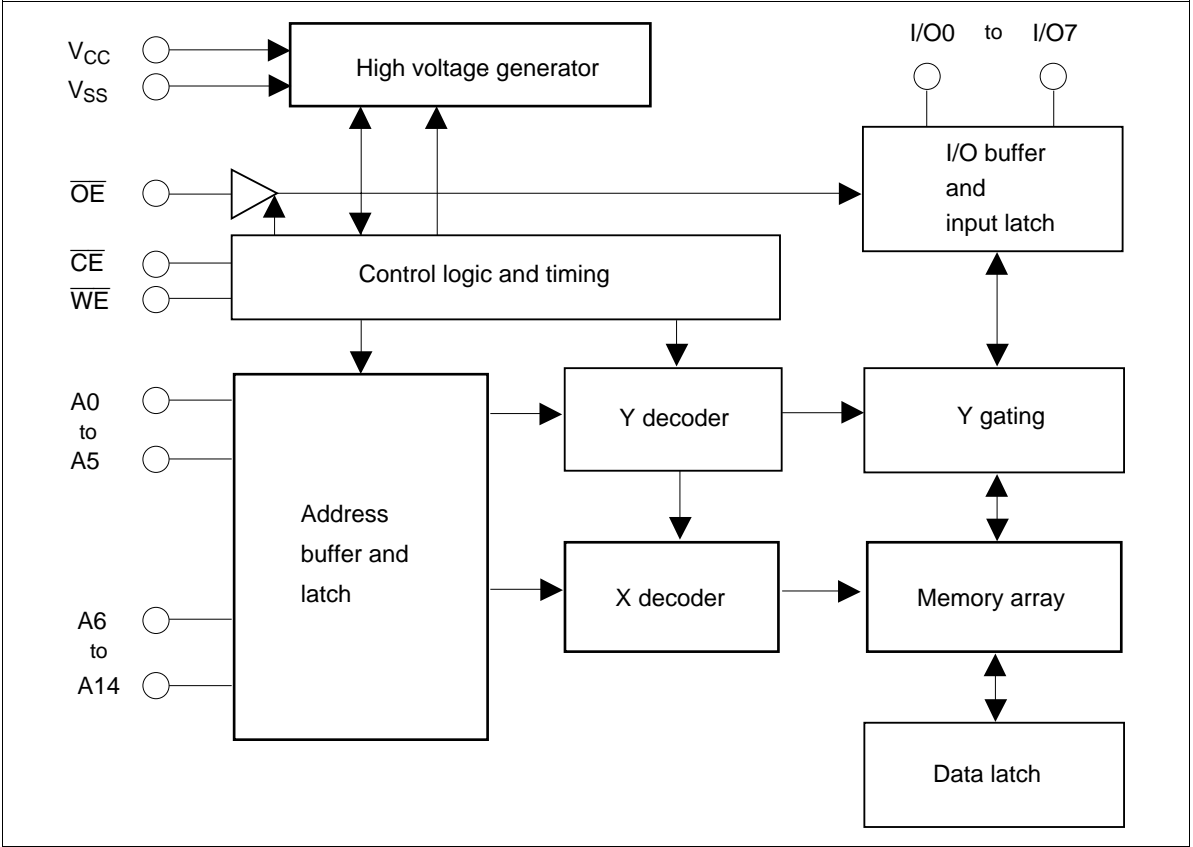
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A14	Address input
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

Block Diagram



Mode Selection

Pin mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	Dout
Standby	$V_{IH}$	$\times^{*2}$	$\times$	High-Z
Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	Din
Deselect	$V_{IL}$	$V_{IH}$	$V_{IH}$	High-Z
Write inhibit	$\times$	$\times$	$V_{IH}$	—
	$\times$	$V_{IL}$	$\times$	—
Data polling	$V_{IL}$	$V_{IL}$	$V_{IH}$	Data out (I/O7)

Notes: 1. Refer to the recommended DC operating condition.

2.  $\times$  = Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V <sub>CC</sub>	−0.6 to +4.6	V
Input voltage*1	V <sub>in</sub>	−0.5*2 to +4.6*4	V
Operating temperature range*3	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C

Notes: 1. With respect to V<sub>SS</sub>  
2. V<sub>in</sub> min = −3.0 V for pulse width ≤ 50 ns  
3. Including electrical characteristics and data retention  
4. Should not exceed V<sub>CC</sub> + 1.0 V.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.2	3.0	3.6	V
Input voltage	V <sub>IL</sub>	−0.3*1	—	0.4	V
	V <sub>IH</sub>	V <sub>CC</sub> × 0.7	—	V <sub>CC</sub> + 0.3*2	V
Operating temperature	Topr	0	—	70	°C

Notes: 1. V<sub>IL</sub> min: −1.0 V for pulse width ≤ 50 ns.  
2. V<sub>IH</sub> max: V<sub>CC</sub> + 1.0 V for pulse width ≤ 50 ns.

DC Characteristics (Ta = 0 to +70 °C, V<sub>CC</sub> = 2.2 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	—	2	μA	V <sub>CC</sub> = 3.6 V, V <sub>in</sub> = 0 to 3.6 V
Output leakage current	I <sub>LO</sub>	—	—	2	μA	V <sub>CC</sub> = 3.6 V, V <sub>out</sub> = 3.6/0.4 V, $\overline{CE} = V_{IH}$ , V <sub>in</sub> = 0 to 3.6 V
V <sub>CC</sub> current (standby)	I <sub>CC1</sub>	—	—	10	μA	$\overline{CE} = V_{CC}$
	I <sub>CC2</sub>	—	—	500	μA	$\overline{CE} = V_{IH}$
V <sub>CC</sub> current (active)	I <sub>CC3</sub>	—	—	8	mA	I <sub>out</sub> = 0 mA, Duty = 100%, Cycle = 1 μs at V <sub>CC</sub> = 3.6 V
		—	—	12	mA	I <sub>out</sub> = 0 mA, Duty = 100%, Cycle = 150 ns at V <sub>CC</sub> = 3.6 V
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 1.0 mA
Output high voltage	V <sub>OH</sub>	V <sub>CC</sub> × 0.8	—	—	V	I <sub>OH</sub> = −100 μA

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*1	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*1	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70 °C, Vcc = 2.2 to 3.6 V)

Test Conditions

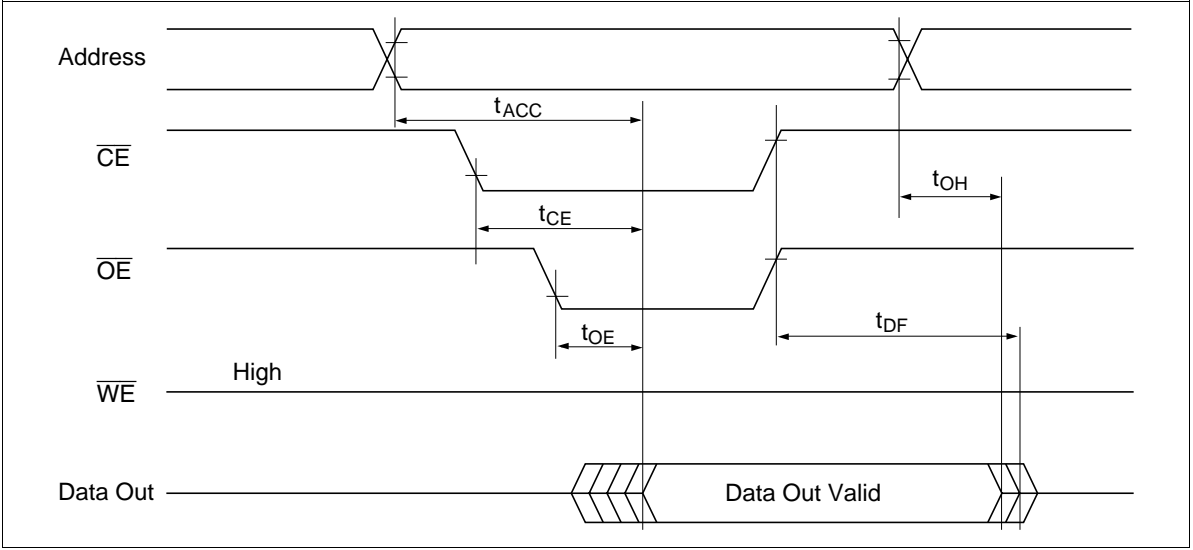
- Input pulse levels: 0.4 V to 1.9 V (Vcc ≤ 2.7V), 0.4V to 2.4 V (Vcc > 2.7 V)
- Input rise and fall time: ≤ 5 ns
- Input timing reference levels: 0.8, 1.8 V
- Output load: 1TTL Gate +100 pF
- Output reference levels: 1.1 V, 1.1 V (Vcc ≤ 2.7V),1.5 V, 1.5 V (Vcc > 2.7 V)

Read Cycle

		HN58S256A					
		-15		-20			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Address to output delay	t <sub>ACC</sub>	—	150	—	200	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{CE}$ to output delay	t <sub>CE</sub>	—	150	—	200	ns	$\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ to output delay	t <sub>OE</sub>	10	80	10	100	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
Address to output hold	t <sub>OH</sub>	0	—	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ ( $\overline{CE}$ ) high to output float* <sup>1</sup>	t <sub>DF</sub>	0	100	0	100	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$

Notes: 1. tDF is defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



## Write Cycle

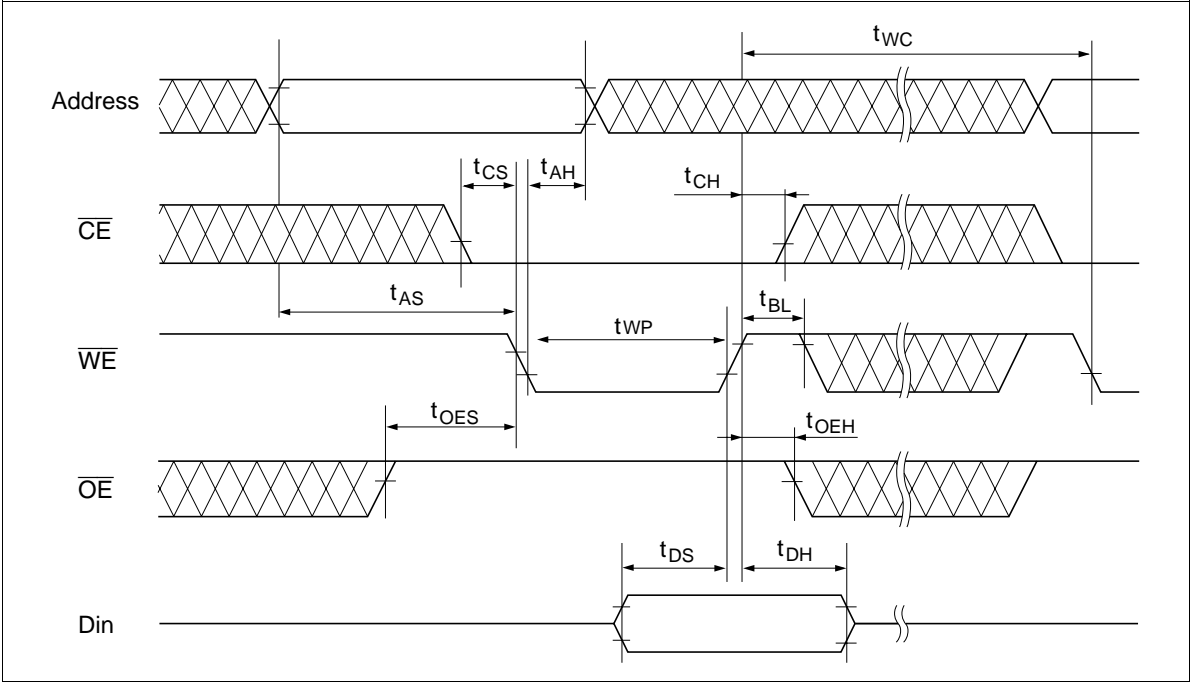
Parameter	Symbol	Min* <sup>1</sup>	Typ	Max	Unit	Test conditions
Address setup time	$t_{AS}$	0	—	—	ns	
Address hold time	$t_{AH}$	150	—	—	ns	
$\overline{CE}$ to write setup time ( $\overline{WE}$ controlled)	$t_{CS}$	0	—	—	ns	
$\overline{CE}$ hold time ( $\overline{WE}$ controlled)	$t_{CH}$	0	—	—	ns	
$\overline{WE}$ to write setup time ( $\overline{CE}$ controlled)	$t_{WS}$	0	—	—	ns	
$\overline{WE}$ hold time ( $\overline{CE}$ controlled)	$t_{WH}$	0	—	—	ns	
$\overline{OE}$ to write setup time	$t_{OES}$	0	—	—	ns	
$\overline{OE}$ hold time	$t_{OEH}$	0	—	—	ns	
Data setup time	$t_{DS}$	150	—	—	ns	
Data hold time	$t_{DH}$	0	—	—	ns	
$\overline{WE}$ pulse width ( $\overline{WE}$ controlled)	$t_{WP}$	200	—	—	ns	
$\overline{CE}$ pulse width ( $\overline{CE}$ controlled)	$t_{CW}$	200	—	—	ns	
Data latch time	$t_{DL}$	200	—	—	ns	
Byte load cycle	$t_{BLC}$	0.4	—	30	$\mu s$	
Byte load window	$t_{BL}$	100	—	—	$\mu s$	
Write cycle time	$t_{WC}$	—	—	15* <sup>2</sup>	ms	
Write start time	$t_{DW}$	0* <sup>3</sup>	—	—	ns	

Notes: 1. Use this device in longer cycle than this value.

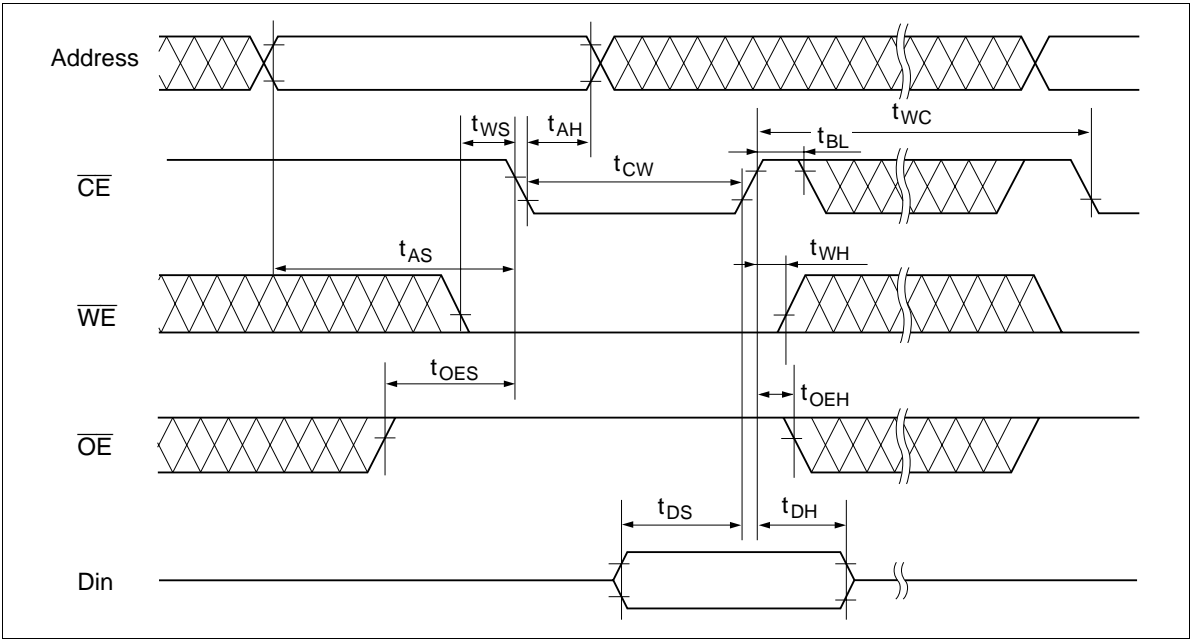
2.  $t_{WC}$  must be longer than this value unless polling techniques is used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after  $t_{DW}$  if polling techniques is used.

Byte Write Timing Waveform (1) ( $\overline{\text{WE}}$  Controlled)

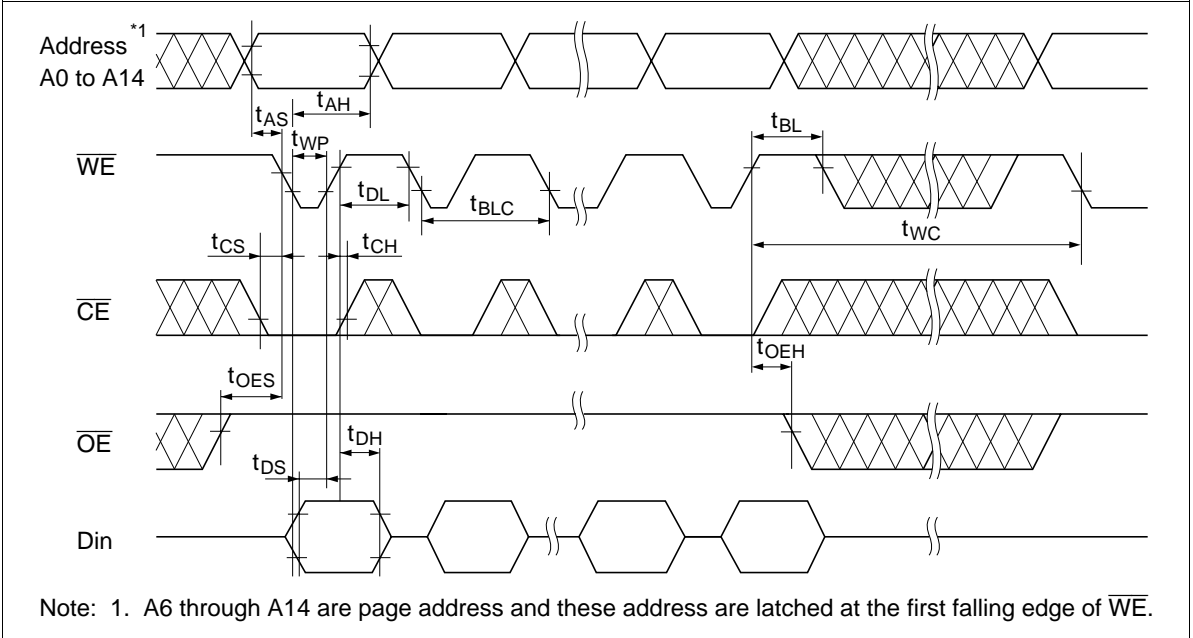


Byte Write Timing Waveform (2) ( $\overline{\text{CE}}$  Controlled)

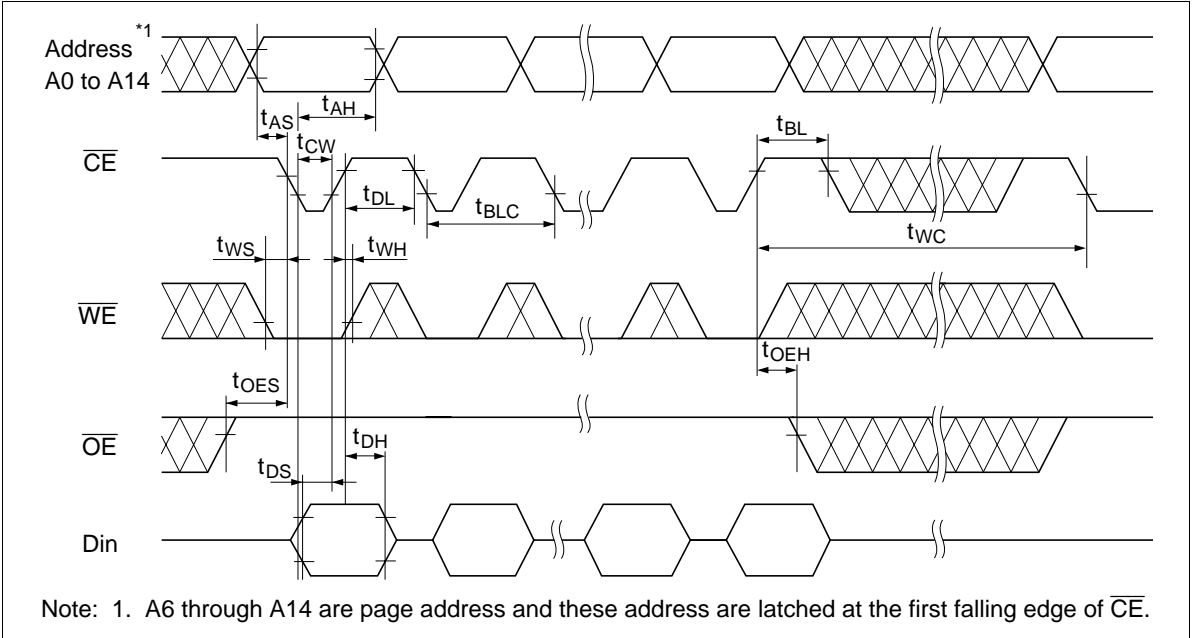




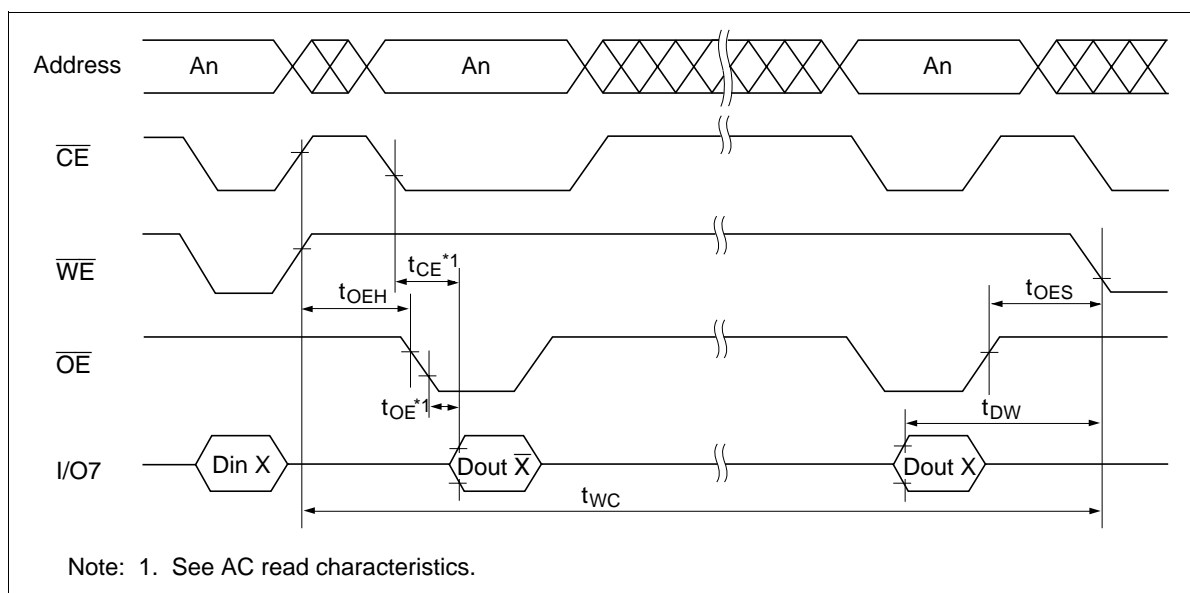
Page Write Timing Waveform (1) ( $\overline{\text{WE}}$  Controlled)



Page Write Timing Waveform (2) ( $\overline{\text{CE}}$  Controlled)



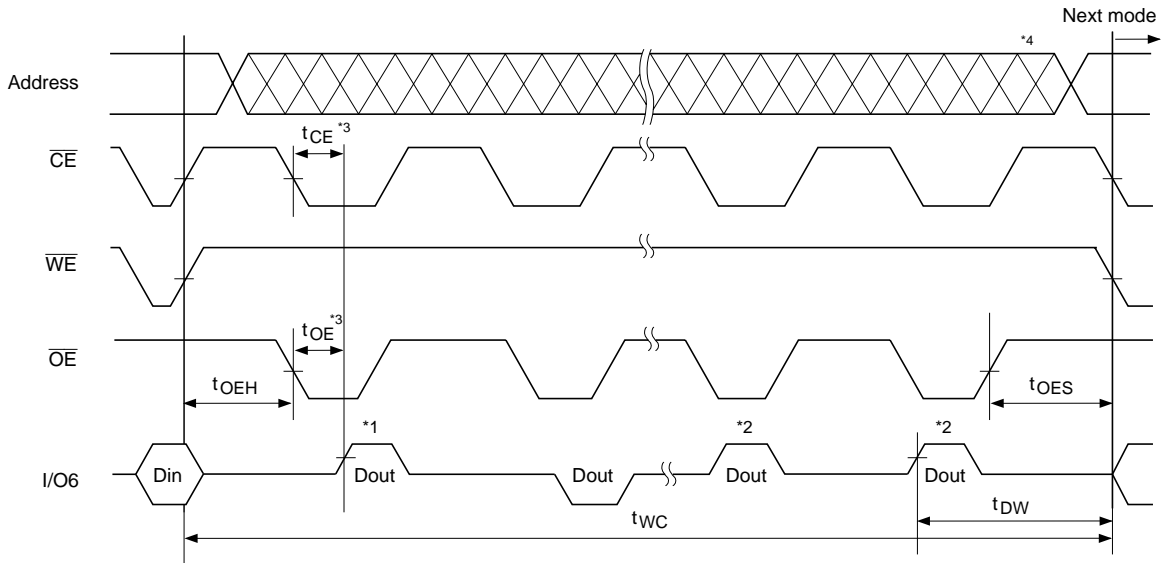
### Data Polling Timing Waveform



## Toggle bit

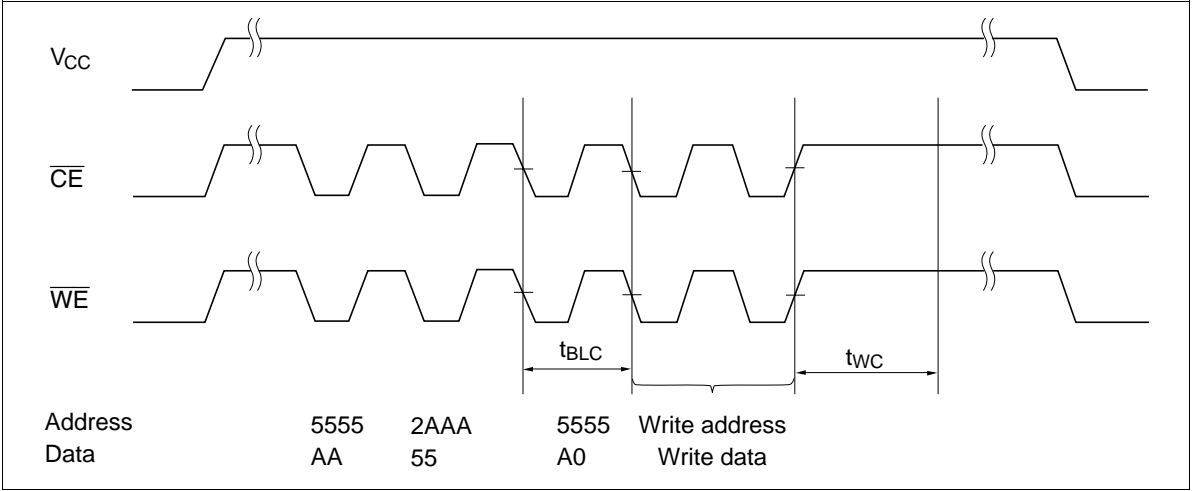
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from “1” to “0” (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

## Toggle bit Waveform

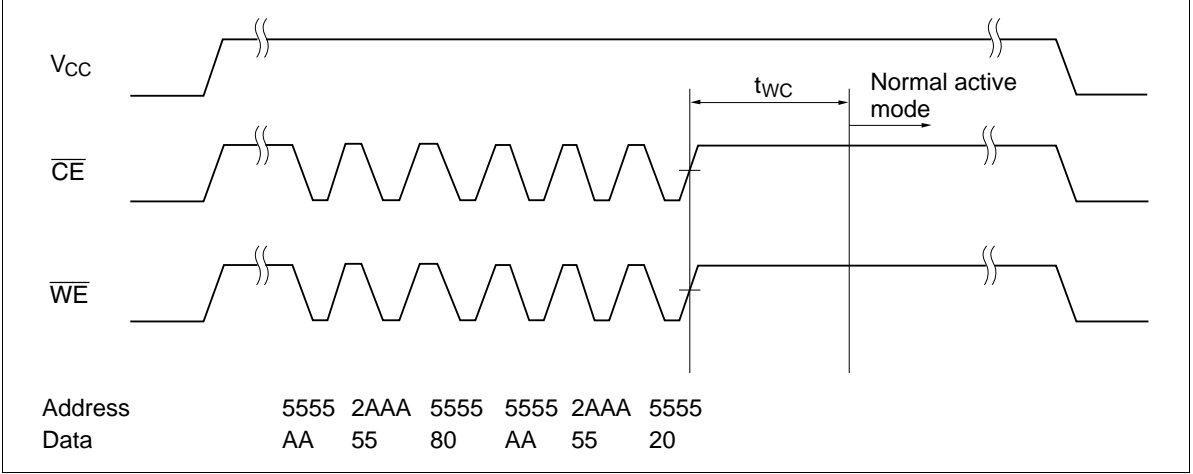


- Notes:
1. I/O6 beginning state is "1".
  2. I/O6 ending state will vary.
  3. See AC read characteristics.
  4. Any address location can be used, but the address must be fixed.

Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



## Functional Description

### Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30  $\mu$ s from the preceding falling edge of  $\overline{WE}$  or  $\overline{CE}$ . When  $\overline{CE}$  or  $\overline{WE}$  is high for 100  $\mu$ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

### Data Polling

Data polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

### $\overline{WE}$ , $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , and data is latched by the rising edge of  $\overline{WE}$  or  $\overline{CE}$ .

### Write/Erase Endurance and Data Retention Time

The endurance is  $10^5$  cycles in case of the page programming and  $10^4$  cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than  $10^4$  cycles.

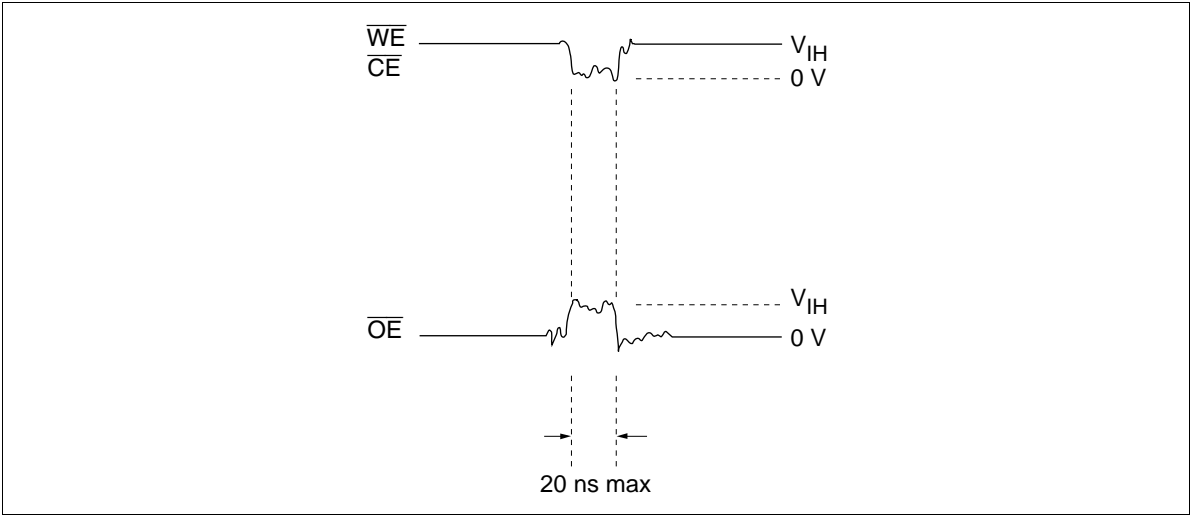
Data Protection

1. Data Protection against Noise on Control Pins ( $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{WE}}$ ) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

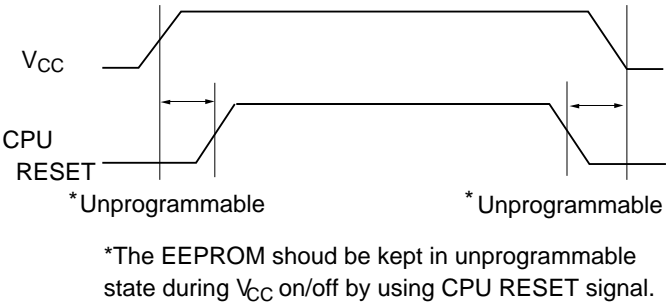
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.

Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V<sub>CC</sub> On/Off

When V<sub>CC</sub> is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.



(1) Protection by  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$

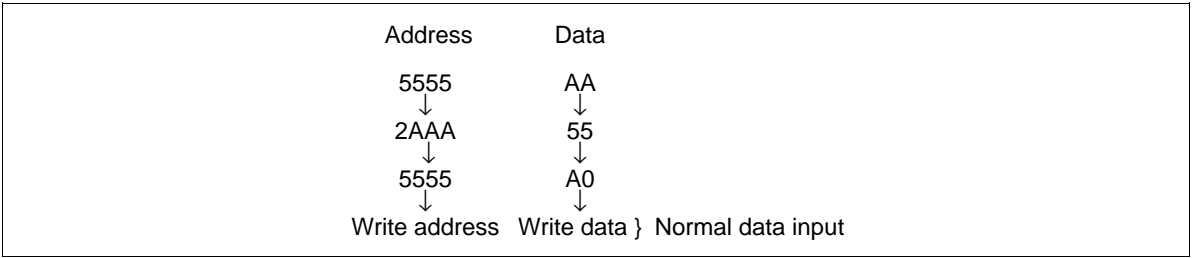
To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V <sub>CC</sub>	×	×
$\overline{OE}$	×	V <sub>SS</sub>	×
$\overline{WE}$	×	×	V <sub>CC</sub>

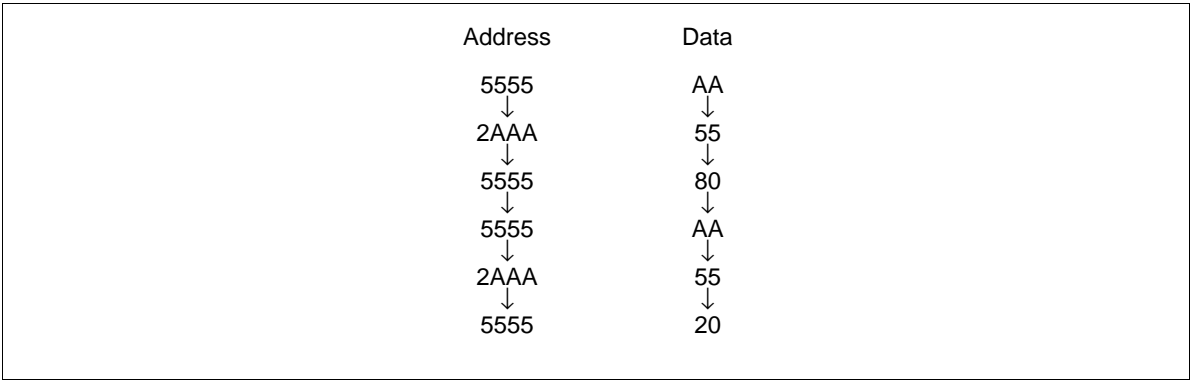
×: Don't care.  
V<sub>CC</sub>: Pull-up to V<sub>CC</sub> level.  
V<sub>SS</sub>: Pull-down to V<sub>SS</sub> level.

3. Software data protetion

To prevent unintentional programming caused by noise generated by external circuits. This device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.



Software data protection mode can be cancelled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the cancelling cycle, the data cannot be written.



The software data protection is not enabled at the shipment.

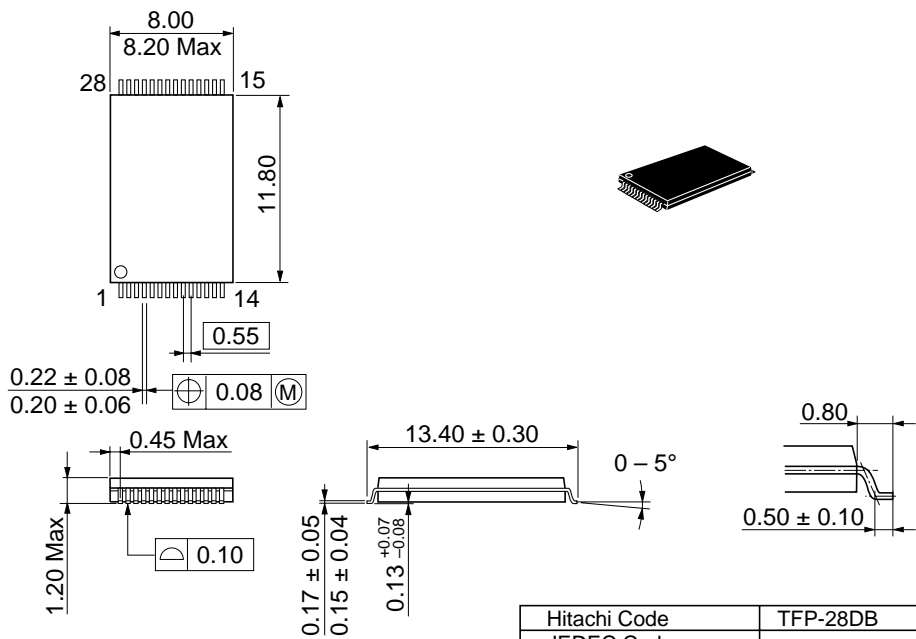
Note: There are some differences between Hitachi’s and other company’s for enable/disable sequence of software data protection. If there are any questions , please contact with Hitachi sales offices.



Package Dimensions

HN58S256AT Series (TFP-28DB)

Unit: mm



Hitachi Code	TFP-28DB
JEDEC Code	—
EIAJ Code	—
Weight	0.23 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Dce. 3, 1996	Initial issue		

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