HB56UW272EJN Series, HB56UW264EJN Series

2,097,152-word × 72-bit High Density Dynamic RAM Module
2,097,152-word × 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-717A (Z)
Rev.1.0
Jan. 27, 1997

Description

The HB56UW272EJN, HB56UW264EJN belong to 8 Byte DIMM (Dual In-line Memory Module) family, and have been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56UW272EJN is a 2M × 72 dynamic RAM module, mounted 9 pieces of 16-Mbit DRAM (HM51W17805) sealed in SOJ package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56UW264EJN is a 2M × 64 dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM51W17805) sealed in SOJ package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56UW272EJN, HB56UW264EJN offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56UW272EJN, HB56UW264EJN is 168-pin socket type package (dual lead out). Therefore, the HB56UW272EJN, HB56UW264EJN make high density mounting possible without surface mount technology. The HB56UW272EJN, HB56UW264EJN provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 168-pin socket type package (Dual lead out)
  - — Outline: 133.35 mm (Length) × 25.40 mm (Height) × 5.28 mm (Thickness)
  - — Lead pitch: 1.27 mm
- Single 3.3 V (±0.3 V) supply
- High speed
  - — Access time: t_{RAC} = 50/60/70ns (max)
    t_{CAC} = 13/15/18ns (max)
- Low power dissipation
  - — Active mode: 3.56/3.24/2.92 W (max) (HB56UW272EJN Series)
    3.17/2.88/2.59 W (max) (HB56UW264EJN Series)
  - — Standby mode (TTL): 64.8 mW (max) (HB56UW272EJN Series)
    (TTL): 57.6 mW (max) (HB56UW264EJN Series)
    (CMOS): 4.86 mW (max) (L-version) (HB56UW272EJN Series)
    (CMOS): 4.32 mW (max) (L-version) (HB56UW264EJN Series)

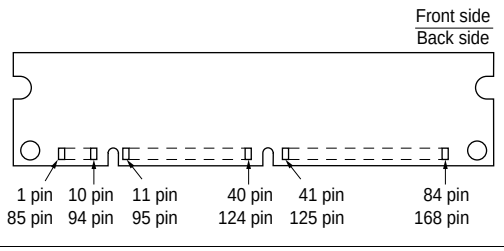
Hitachi semiconductor

- JEDEC standard outline unbuffered 8-byte DIMM
- EDO page mode capability
- Refresh period
  - 2048 refresh cycles: 32 ms
    128 ms (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
  - Self refresh (L-version)

Ordering Information

Type No.	Access time	Package	Contact pad
HB56UW272EJN-5	50 ns	168-pin dual lead out socket type	Gold
HB56UW272EJN-6	60 ns		
HB56UW272EJN-7	70 ns		
HB56UW272EJN-5L	50 ns		
HB56UW272EJN-6L	60 ns		
HB56UW272EJN-7L	70 ns		
HB56UW264EJN-5	50 ns		
HB56UW264EJN-6	60 ns		
HB56UW264EJN-7	70 ns		
HB56UW264EJN-5L	50 ns		
HB56UW264EJN-6L	60 ns		
HB56UW264EJN-7L	70 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	NC
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS2}$	88	DQ34	130	$\overline{CAS6}$
5	DQ3	47	$\overline{CAS3}$	89	DQ35	131	$\overline{CAS7}$
6	V_{CC}	48	$\overline{WE2}$	90	V_{CC}	132	NC
7	DQ4	49	V_{CC}	91	DQ36	133	V_{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2 (NC)*3	94	DQ39	136	CB6 (NC)*7
11	DQ8	53	CB3 (NC)*4	95	DQ40	137	CB7 (NC)*8
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{CC}	101	DQ45	143	V_{CC}
18	V_{CC}	60	DQ20	102	V_{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0 (NC)*1	63	NC	105	CB4 (NC)*5	147	NC
22	CB1 (NC)*2	64	V_{SS}	106	CB5 (NC)*6	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	$\overline{WE0}$	69	DQ24	111	NC	153	DQ56
28	$\overline{CAS0}$	70	DQ25	112	$\overline{CAS4}$	154	DQ57
29	$\overline{CAS1}$	71	DQ26	113	$\overline{CAS5}$	155	DQ58
30	$\overline{RAS0}$	72	DQ27	114	NC	156	DQ59
31	$\overline{OE0}$	73	V_{CC}	115	NC	157	V_{CC}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62

Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V_{CC}	82	SDA	124	V_{CC}	166	SA1
41	V_{CC}	83	SCL	125	NC	167	SA2
42	NC	84	V_{CC}	126	NC	168	V_{CC}

Notes:
1. CB0: HB56UW272EJN, NC: HB56UW264EJN
2. CB1: HB56UW272EJN, NC: HB56UW264EJN
3. CB2: HB56UW272EJN, NC: HB56UW264EJN
4. CB3: HB56UW272EJN, NC: HB56UW264EJN
5. CB4: HB56UW272EJN, NC: HB56UW264EJN
6. CB5: HB56UW272EJN, NC: HB56UW264EJN
7. CB6: HB56UW272EJN, NC: HB56UW264EJN
8. CB7: HB56UW272EJN, NC: HB56UW264EJN

Pin Description

Pin name	Function
A0 to A10	Address input — Row address: A0 to A10 — Column address: A0 to A9 — Refresh address: A0 to A10
DQ0 to DQ63	Data-in/data-out
$\overline{RAS0}$, $\overline{RAS2}$	Row address strobe
$\overline{CAS0}$ to $\overline{CAS7}$	Column address strobe
$\overline{WE0}$, $\overline{WE2}$	Read/Write enable
$\overline{OE0}$, $\overline{OE2}$	Output enable
SDA	Serial data for PD
SCL	Serial clock for PD
SA0 to SA2	Serial address for PD
CB0 to CB7*[1]	Check bit
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

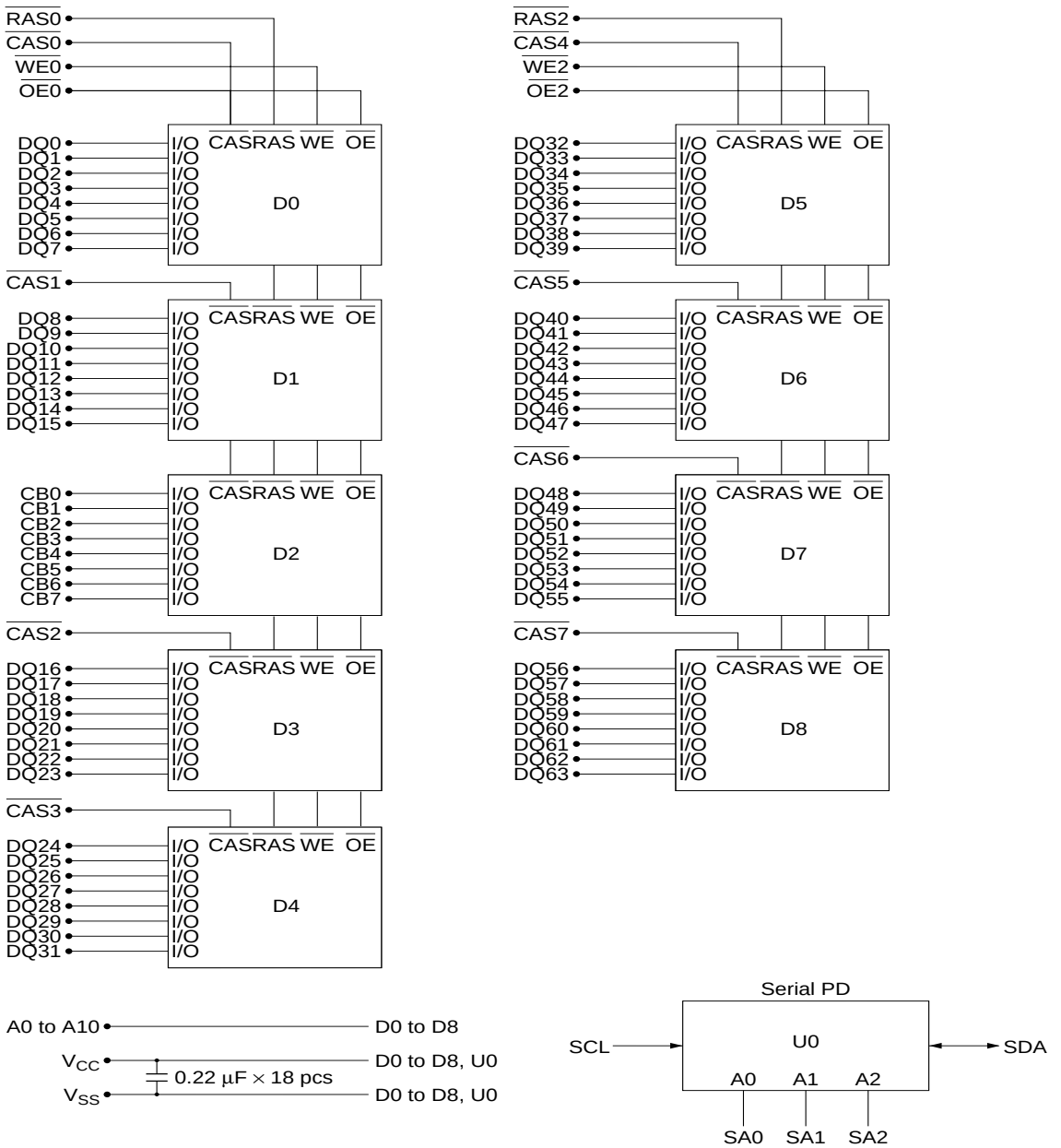
Note: 1. This function is supported only HB56UW272EJN Series.

Serial PD Matrix*[1]

Byte number	Function described		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comments
0	Number serial PD bytes		0	0	0	0	1	1	0	1	13
1	Serial memory		0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		0	0	0	0	0	0	1	0	EDO
3	Number of rows		0	0	0	0	1	0	1	1	11
4	Number of columns		0	0	0	0	1	0	1	0	10
5	Number of banks		0	0	0	0	0	0	0	1	1
6	Data width										
	HB56UW272EJN		0	1	0	0	1	0	0	0	72
	HB56UW264EJN		0	1	0	0	0	0	0	0	64
7	Data width (continued)		0	0	0	0	0	0	0	0	0 (+)
8	Voltage interface		0	0	0	0	0	0	0	1	3.3 Volt
9	$\overline{RAS}$ access time	50 ns	0	0	1	1	0	0	1	0	
		60 ns	0	0	1	1	1	1	0	0	
		70 ns	0	1	0	0	0	1	1	0	
10	$\overline{CAS}$ access time	13 ns	0	0	0	0	1	1	0	1	
		15 ns	0	0	0	0	1	1	1	1	
		18 ns	0	0	0	1	0	0	1	0	
11	Error detection/corraction										
	HB56UW272EJN		0	0	0	0	0	0	1	0	ECC
	HB56UW264EJN		0	0	0	0	0	0	0	0	None-parity
12	Refresh period		0	0	0	0	0	0	0	0	Normal (15.625 µs)
	Refresh period (L-version)		1	0	0	0	0	1	0	0	Self refresh (62.5 µs)

Note: 1. Serial-PD data are not protected.
1: High level (Serial data)
0: Low level (Serial data)

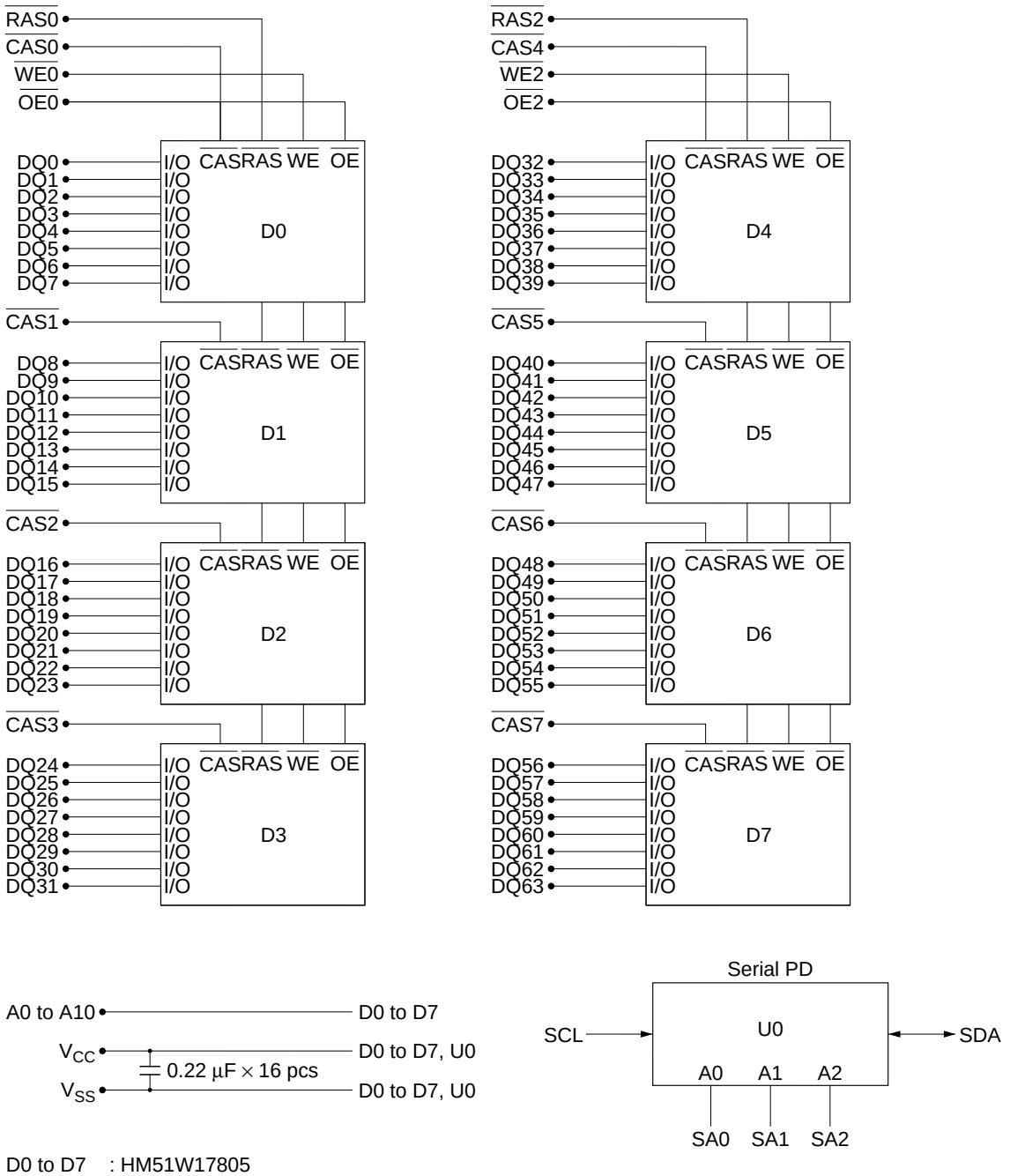
Block Diagram (HB56UW272EJN)



* D0 to D8 : HM51W17805
U0 : 24C02

Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collecter output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inactive "High" state.

Block Diagram (HB56UW264EJN)



* D0 to D7 : HM51W17805
U0 : 24C02

Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collecter output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inactive "High" state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation (HB56UW272EJN)	Pt	9	W
Power dissipation (HB56UW264EJN)	Pt	8	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V) (HB56UW272EJN)

		50 ns		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	990	—	900	—	810	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	18	—	18	—	18	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	9	—	9	—	9	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	1.35	—	1.35	—	1.35	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	990	—	900	—	810	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	45	—	45	—	45	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	990	—	900	—	810	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	900	—	810	—	765	mA	t_{HPC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	3.6	—	3.6	—	3.6	mA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 62.5 µs t_{RAS} ≤ 0.3 µs	4
Self refresh mode current (L-version)	I_{CC11}	—	2.25	—	2.25	—	2.25	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V Dout = High-Z	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. $\overline{CAS}$ = L (≤ 0.2 V) while $\overline{RAS}$ = L (≤ 0.2 V).

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V) (HB56UW264EJN)

		50 ns		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	880	—	800	—	720	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	1.2	—	1.2	—	1.2	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	880	—	800	—	720	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	880	—	800	—	720	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	800	—	720	—	680	mA	t_{HPC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	3.2	—	3.2	—	3.2	mA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 62.5 µs t_{RAS} ≤ 0.3 µs	4
Self refresh mode current (L-version)	I_{CC11}	—	2	—	2	—	2	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V Dout = High-Z	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. $\overline{CAS}$ = L (≤ 0.2 V) while $\overline{RAS}$ = L (≤ 0.2 V).

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V) (HB56UW272EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{I!}$	—	65	pF	1
Input capacitance ($\overline{RAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	55	pF	1
Input capacitance ($\overline{CAS}$)	C_{I3}	—	34	pF	1
I/O capacitance (DQ, CB)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V) (HB56UW264EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{I!}$	—	60	pF	1
Input capacitance ($\overline{RAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	48	pF	1
Input capacitance ($\overline{CAS}$)	C_{I3}	—	27	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70˚C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V) *[1], *[2], *[18], *[19]

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	84	—	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	—	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10000	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	14	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	12	30	12	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	10	—	13	—	13	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	35	—	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	13	—	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	7
Refresh period (2,048 cycles)	t_{REF}	—	32	—	32	—	32	ms	
Refresh period (2,048 cycles) (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	25	—	30	—	35	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	18	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time from $\overline{RAS}$	t_{RCHR}	50	—	60	—	70	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	15	—	18	—	23	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	22
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	13, 22
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	13	—	15	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{RAS}$	t_{OFR}	—	13	—	15	—	15	ns	22
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	13	—	15	—	15	ns	
$\overline{WE}$ to Din delay time	t_{WED}	13	—	15	—	18	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	13	—	15	—	18	—	ns	
$\overline{RAS}$ next $\overline{CAS}$ delay time	t_{RNCD}	50	—	60	—	70	—	ns	

Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	8	—	10	—	13	—	ns	
Write command pulse width	t_{WP}	8	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8	—	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8	—	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	8	—	10	—	13	—	ns	15

Read-Modify-Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	111	—	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	67	—	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	49	—	57	—	ns	14
$\overline{OE}$ hold time $\overline{WE}$	t_{OEH}	13	—	15	—	18	—	ns	

Refresh Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	8	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	5	—	ns	

EDO Page Mode Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	20	—	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	30	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	30	—	35	—	40	—	ns	
Output data hole time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time refferred $\overline{OE}$	t_{COL}	8	—	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	30	—	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read-modify-write cycle time	t_{HPRWC}	57	—	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	45	—	54	—	62	—	ns	14

Self Refresh Mode (L-version)

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{RAS}$ pulse width (Self refresh)	t_{RASS}	100	—	100	—	100	—	µs	
$\overline{RAS}$ precharge time (Self refresh)	t_{RPS}	90	—	110	—	130	—	ns	
$\overline{CAS}$ hold time (Self refresh)	t_{CHS}	–50	—	–50	—	–50	—	ns	

Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RAD}$ (max) + t_{AA} (max)- t_{CAC} (max), then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics onry; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min) or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the DQ pin will remain open circuit (high impedance); $t_{OEH} < t_{OEH}$, invalid data will be out at each DQ.
19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
22. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.

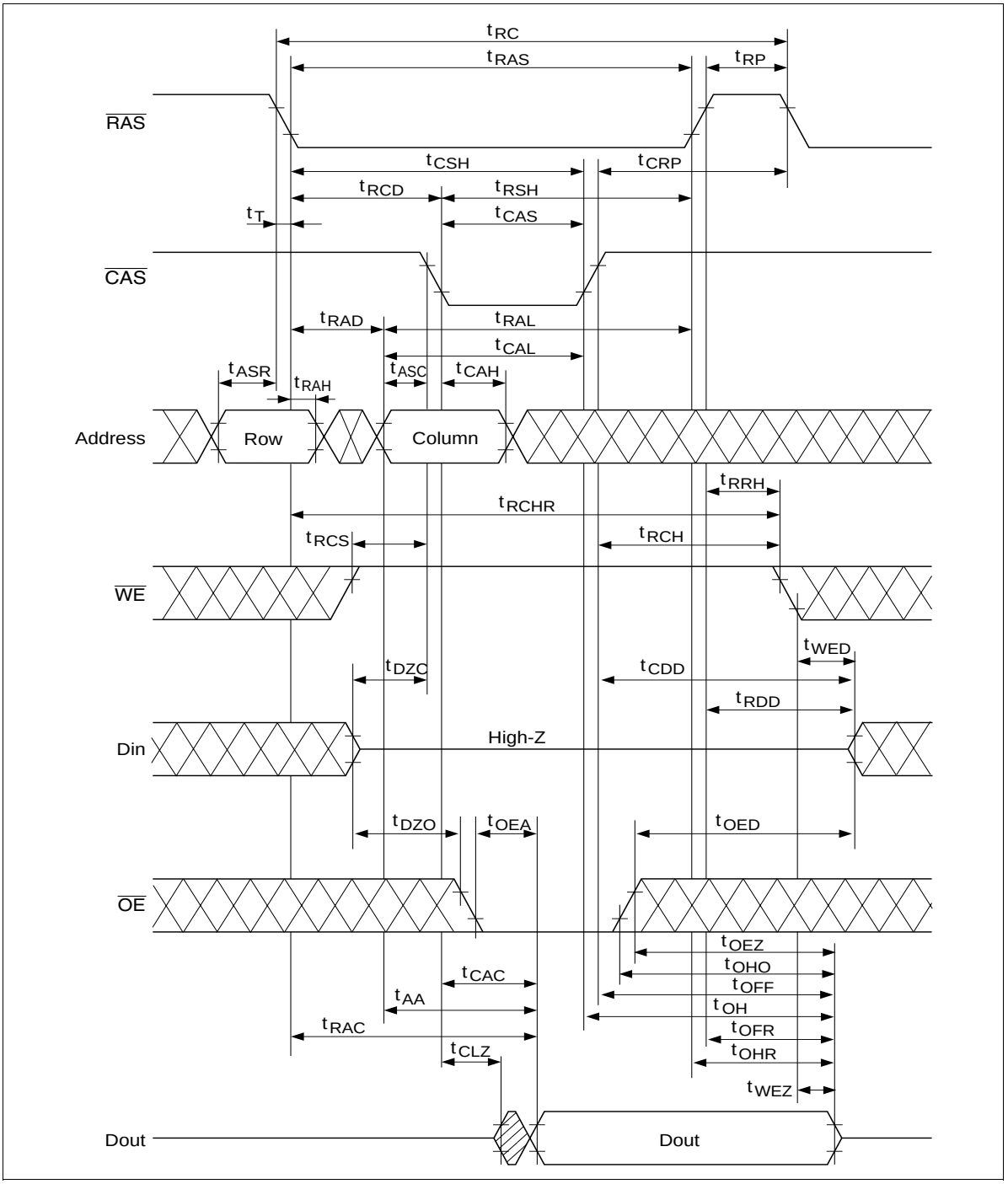
23. Please do not use t_{RASS} timing, 10 µs ≤ t_{RASS} ≤ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If t_{RASS} ≥ 100 µs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
24. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
25. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 2048 of distributed CBR refresh with 15.6 µs interval should be executed within 32 ms immediately after exiting from and before entering into the self refresh mode.
26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
27. XXX: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

    ///////: Invalid Dout

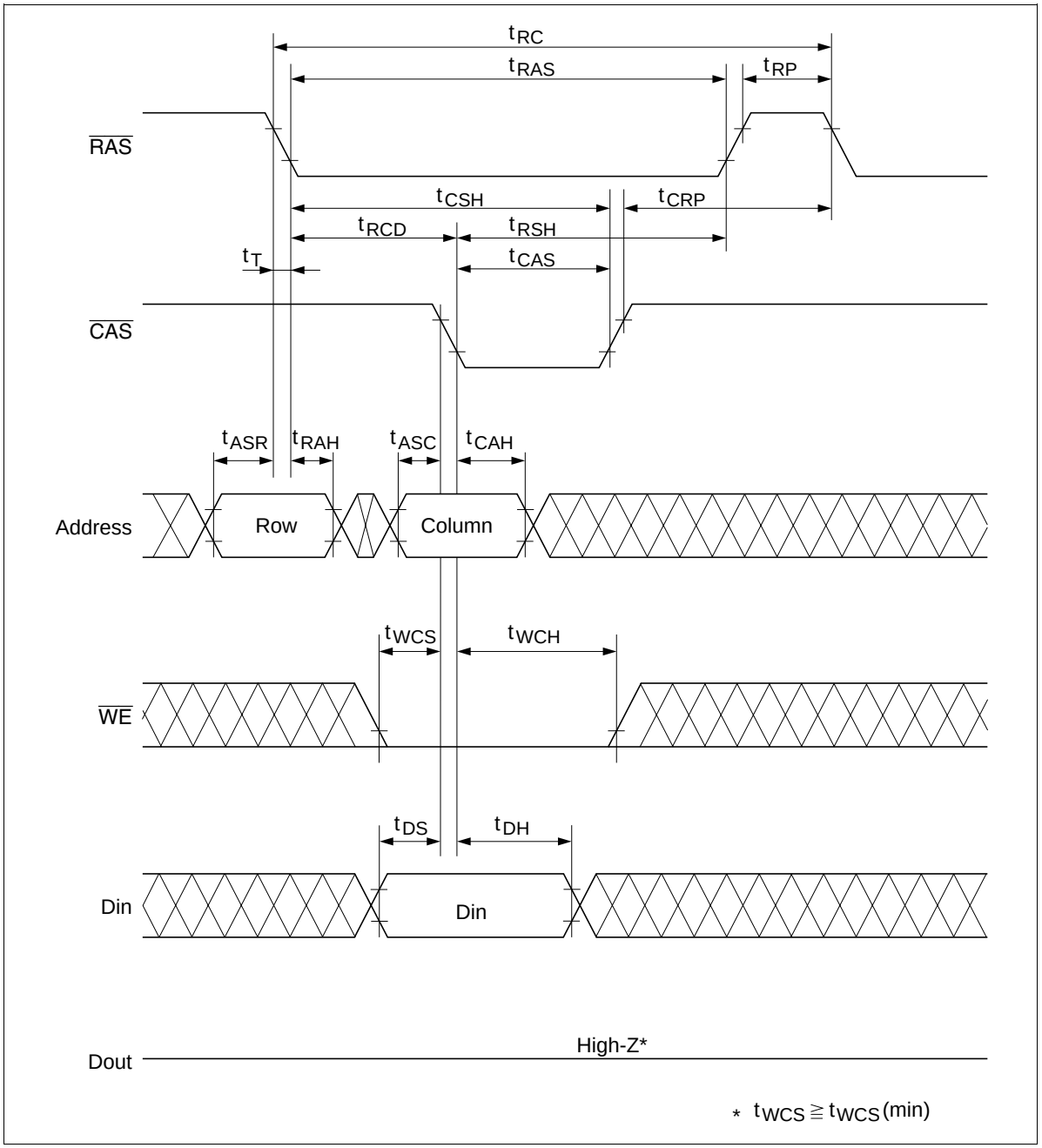
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[27]

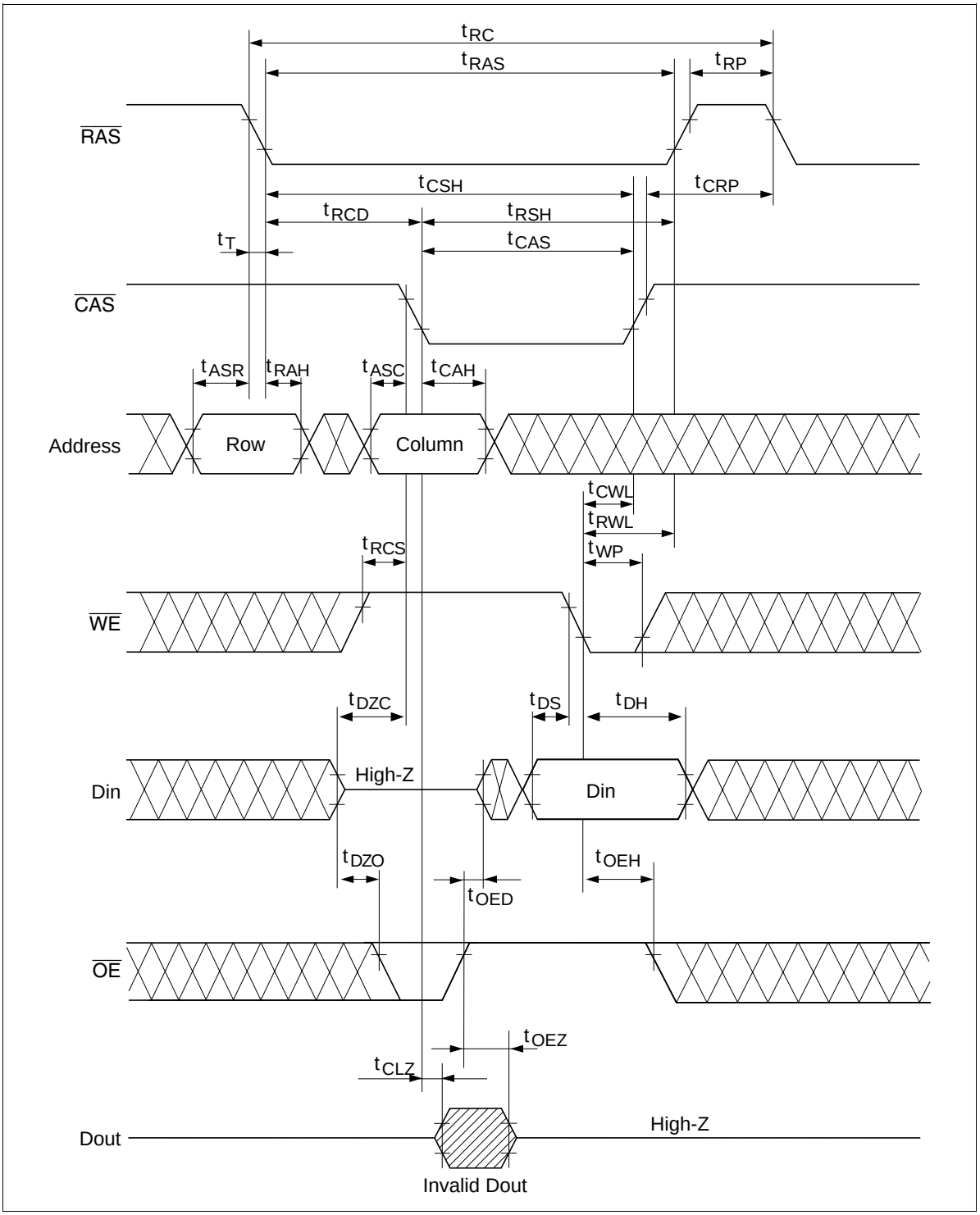
Read Cycle



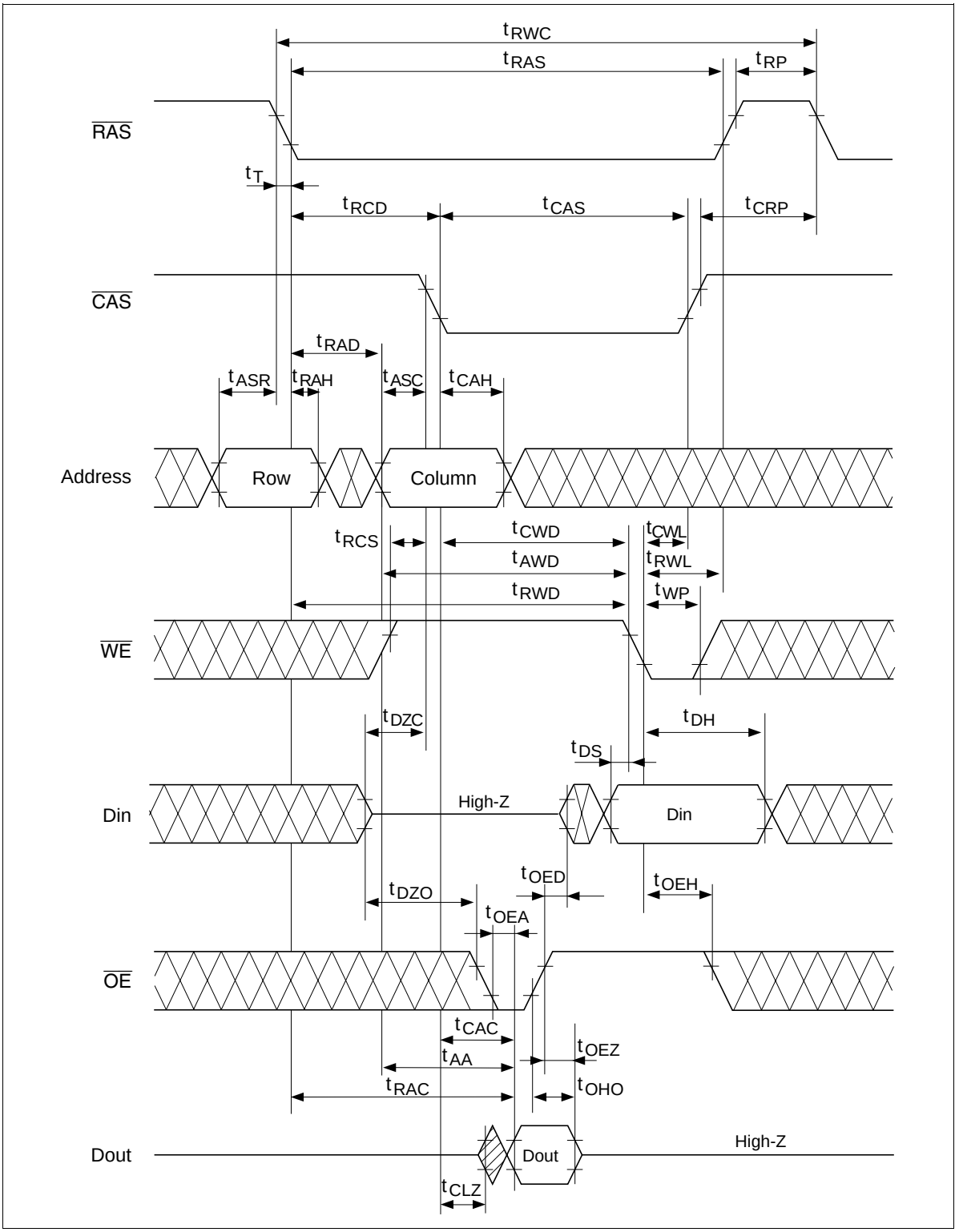
Early Write Cycle



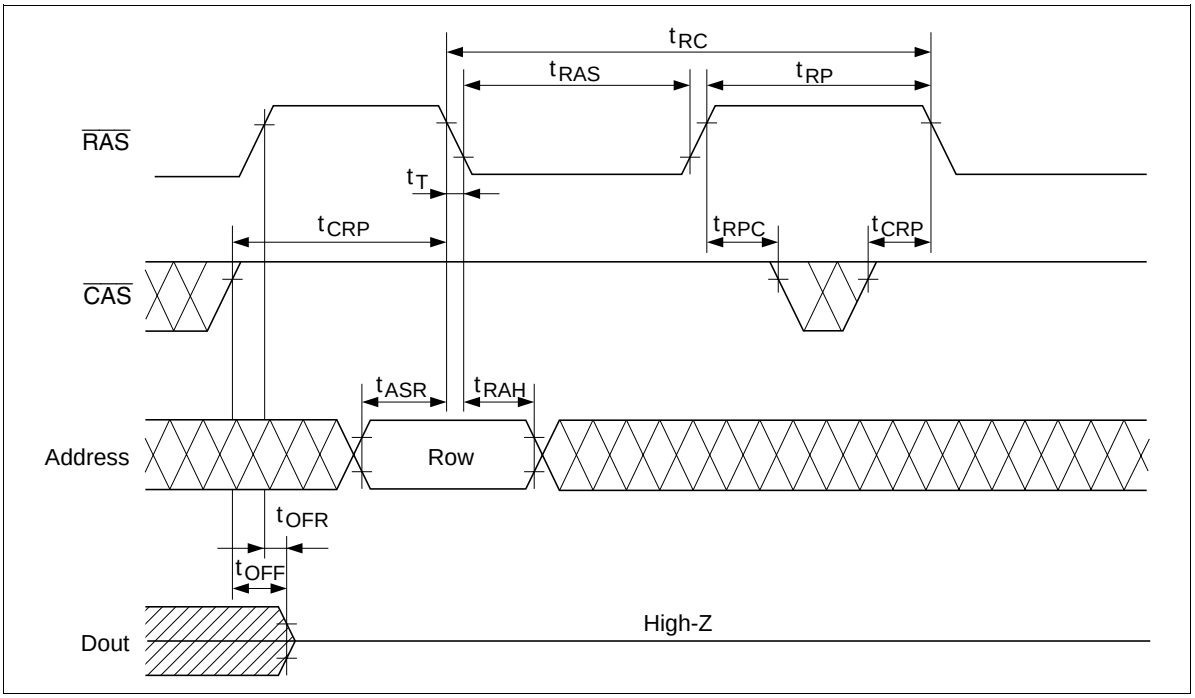
Delayed Write Cycle*[18]



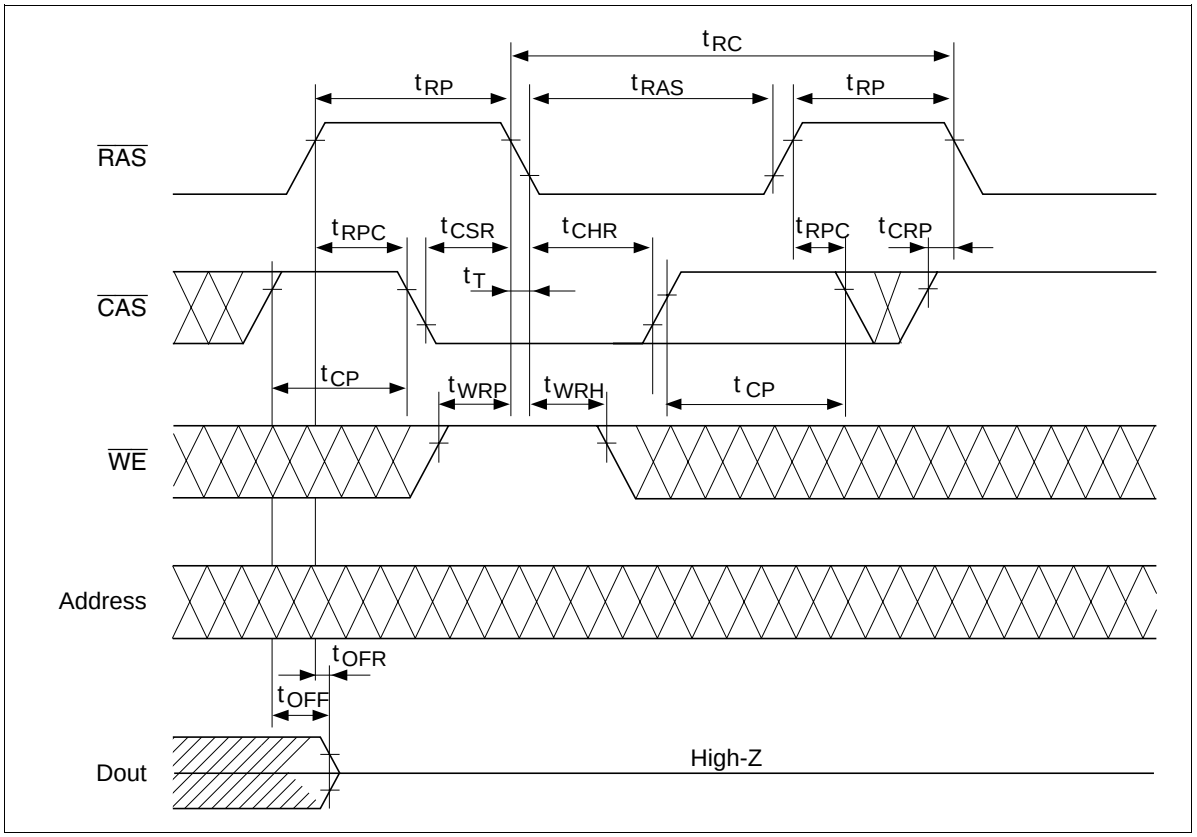
Read-Modify-Write Cycle*[18]



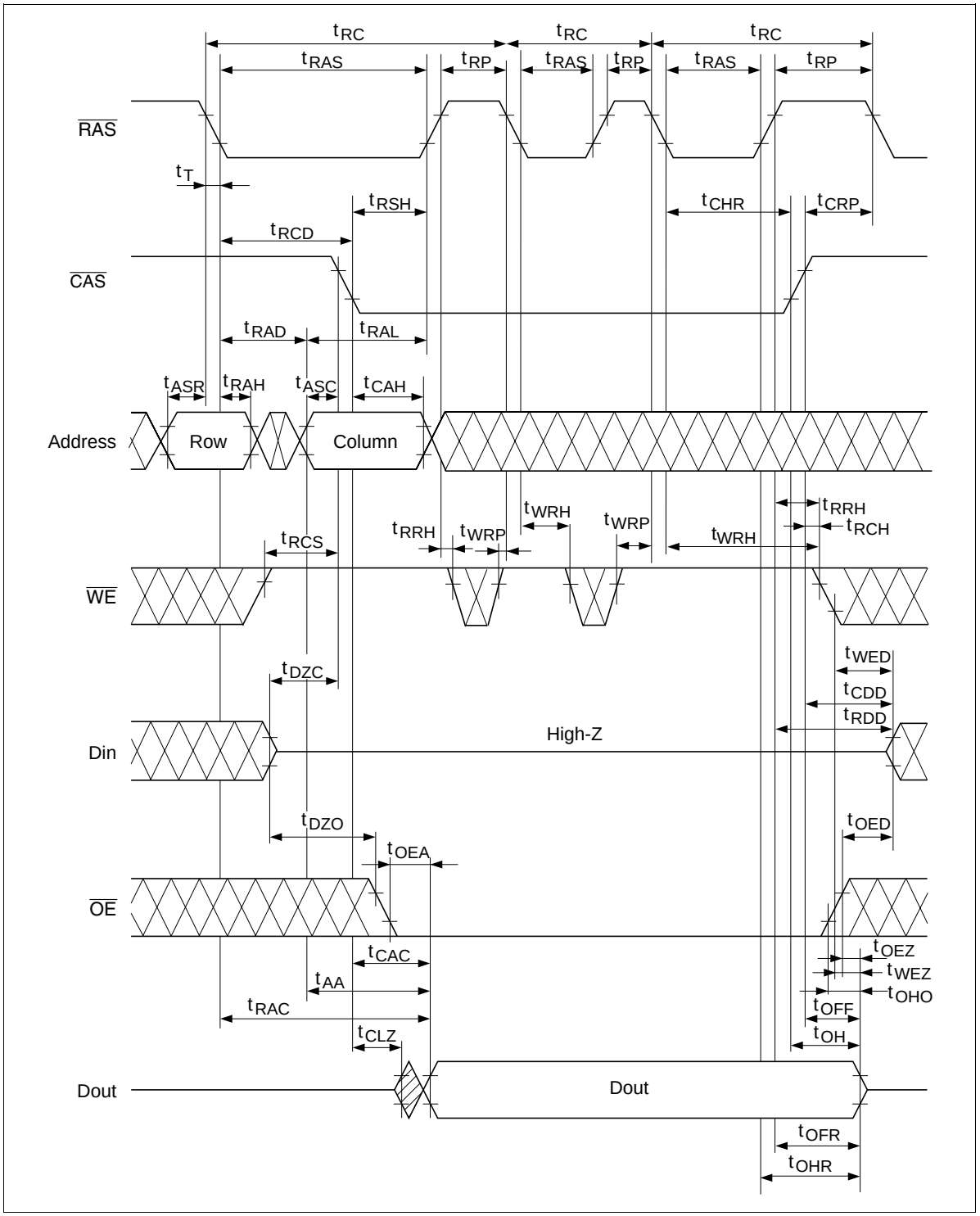
$\overline{\text{RAS}}$-Only Refresh Cycle



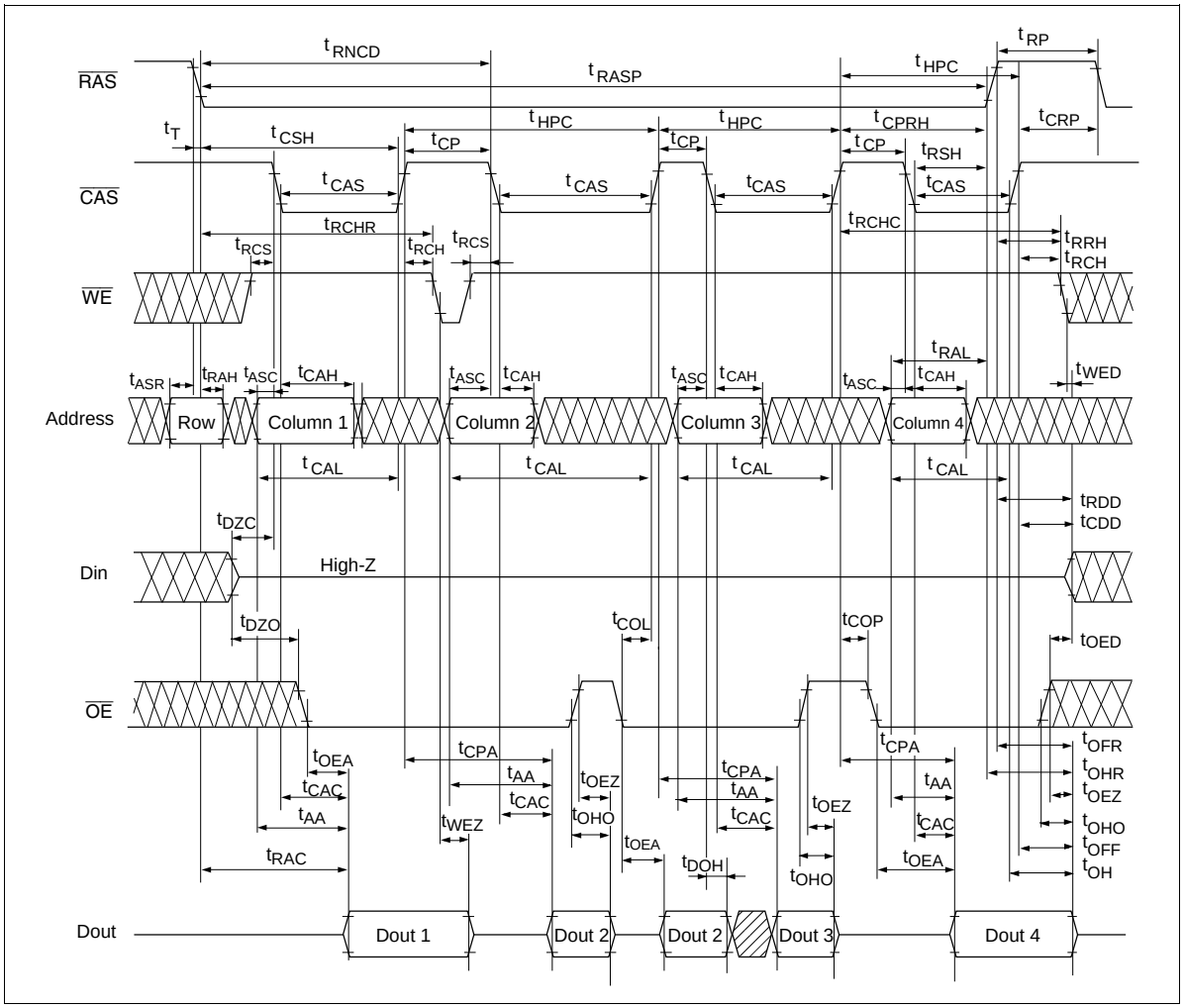
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



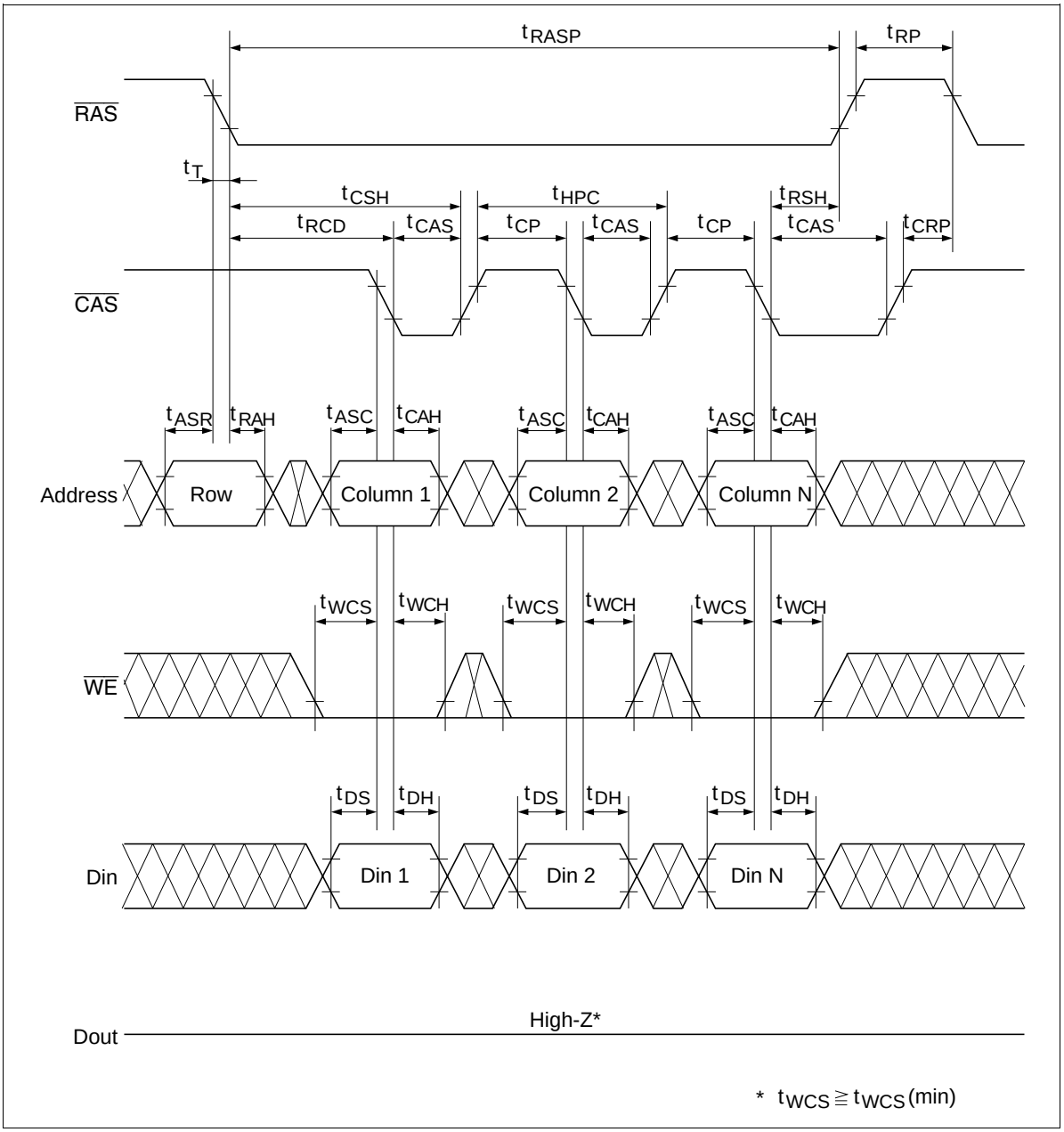
Hidden Refresh Cycle



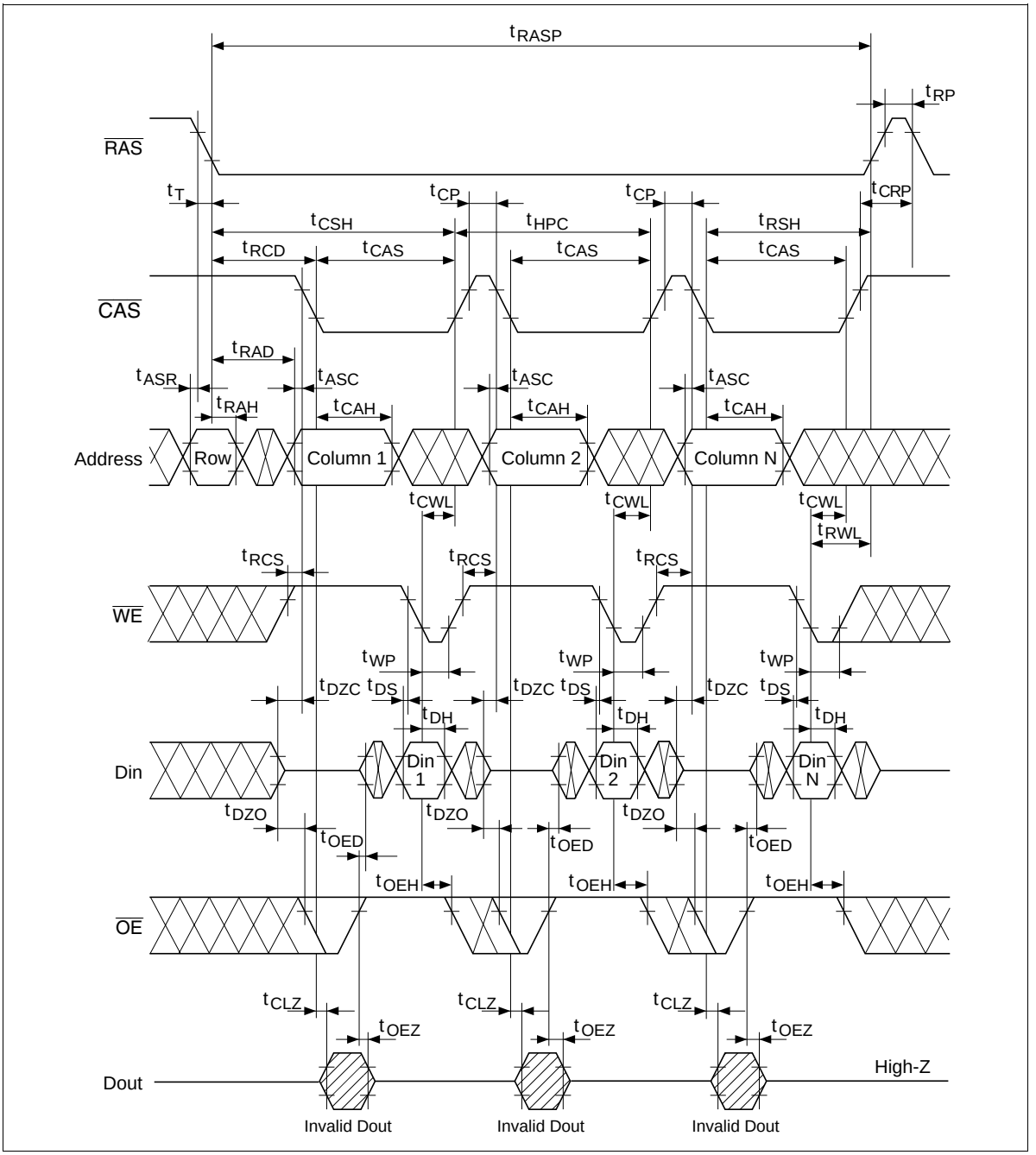
EDO Page Mode Read Cycle



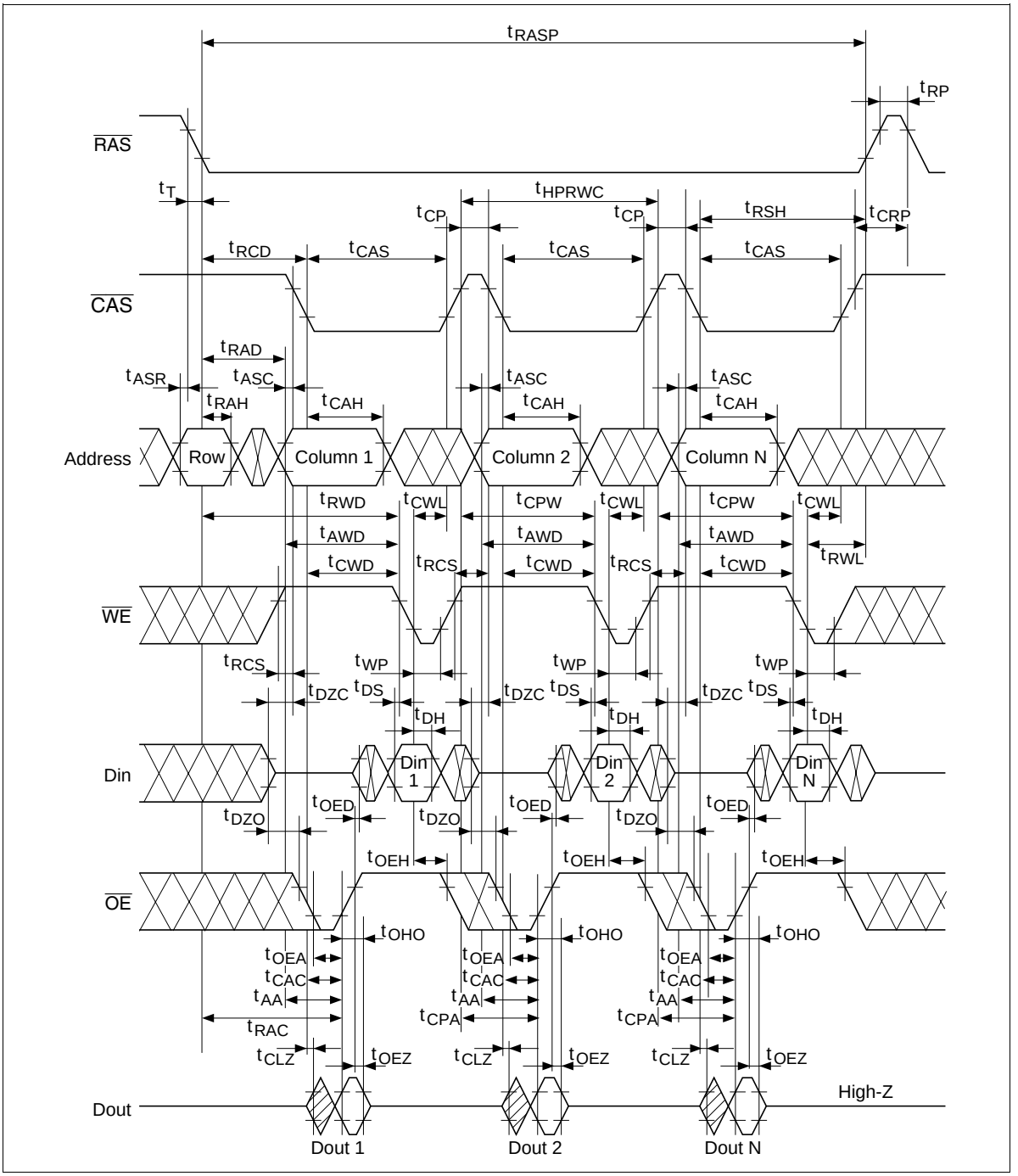
EDO Page Mode Early Write Cycle



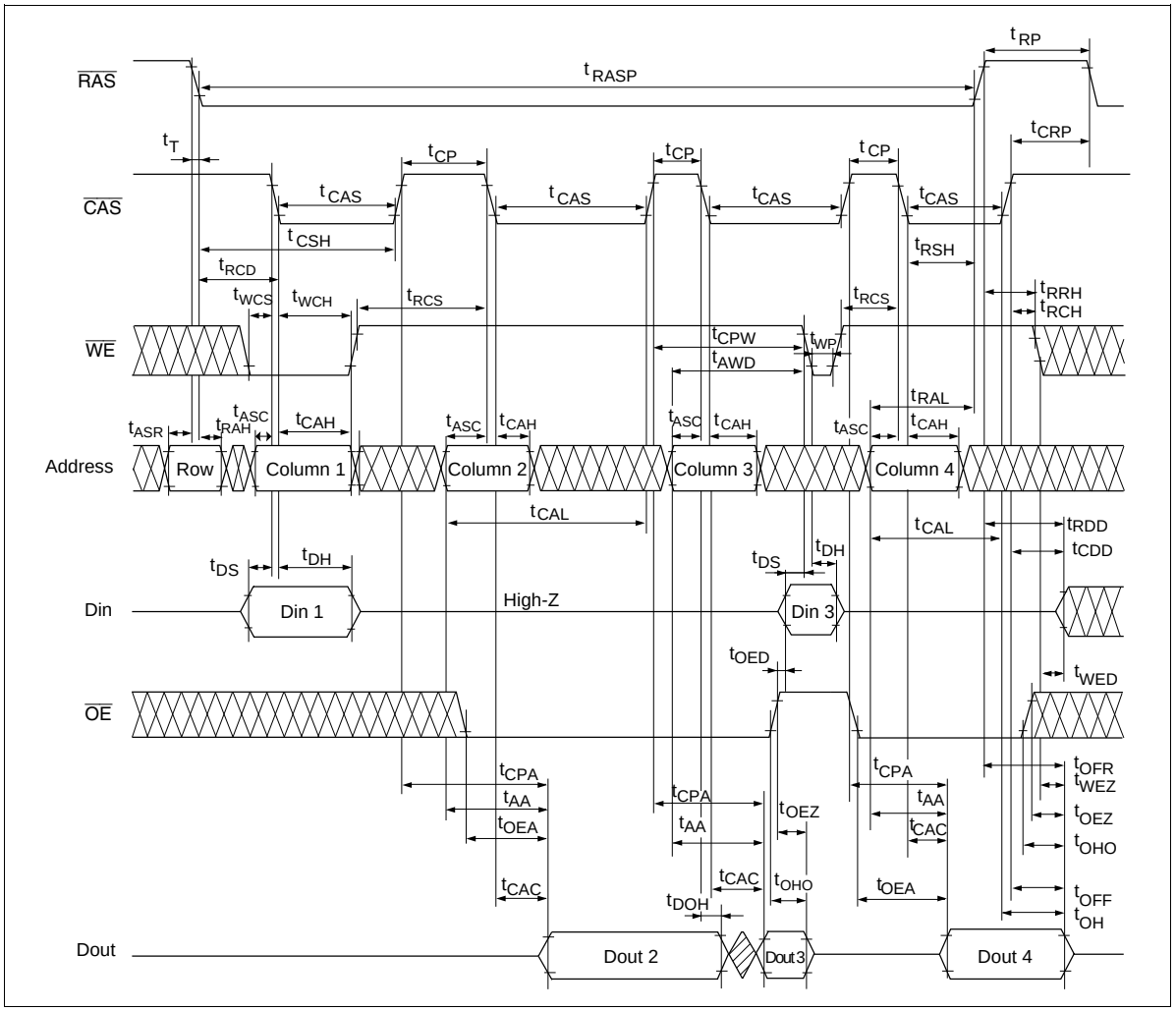
EDO Page Mode Delayed Write Cycle*[18]



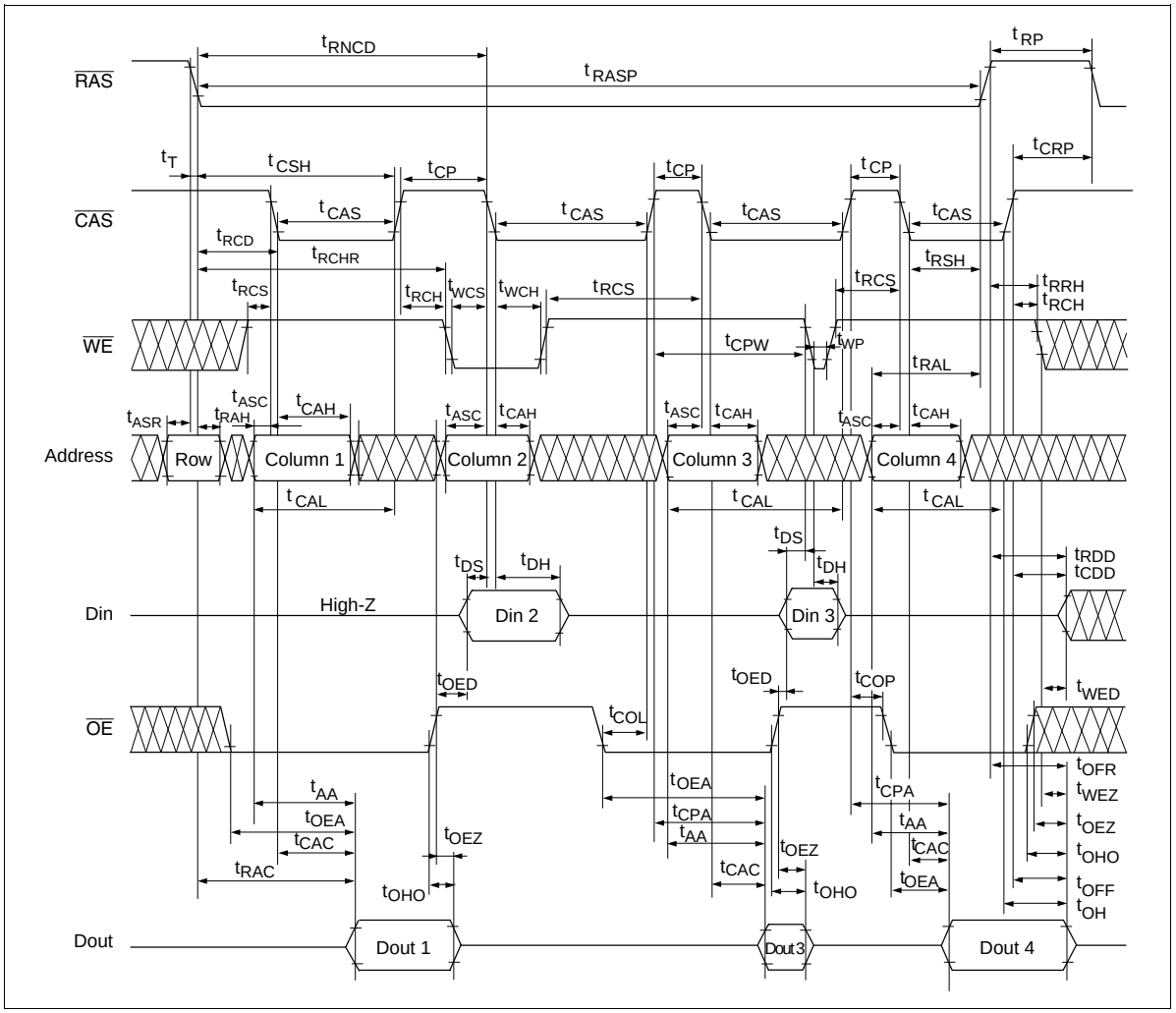
EDO Page Mode Read-Modify-Write Cycle*[18]



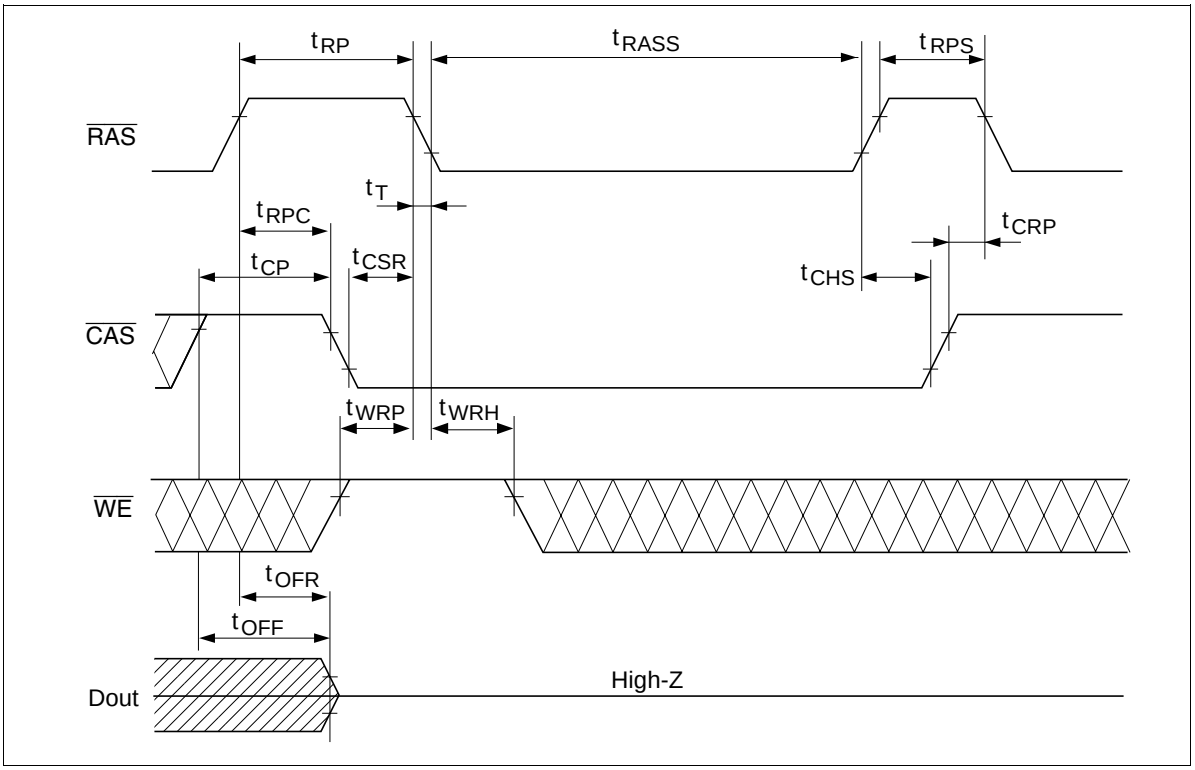
EDO Page Mode Mix Cycle (1)



EDO Page Mode Mix Cycle (2)

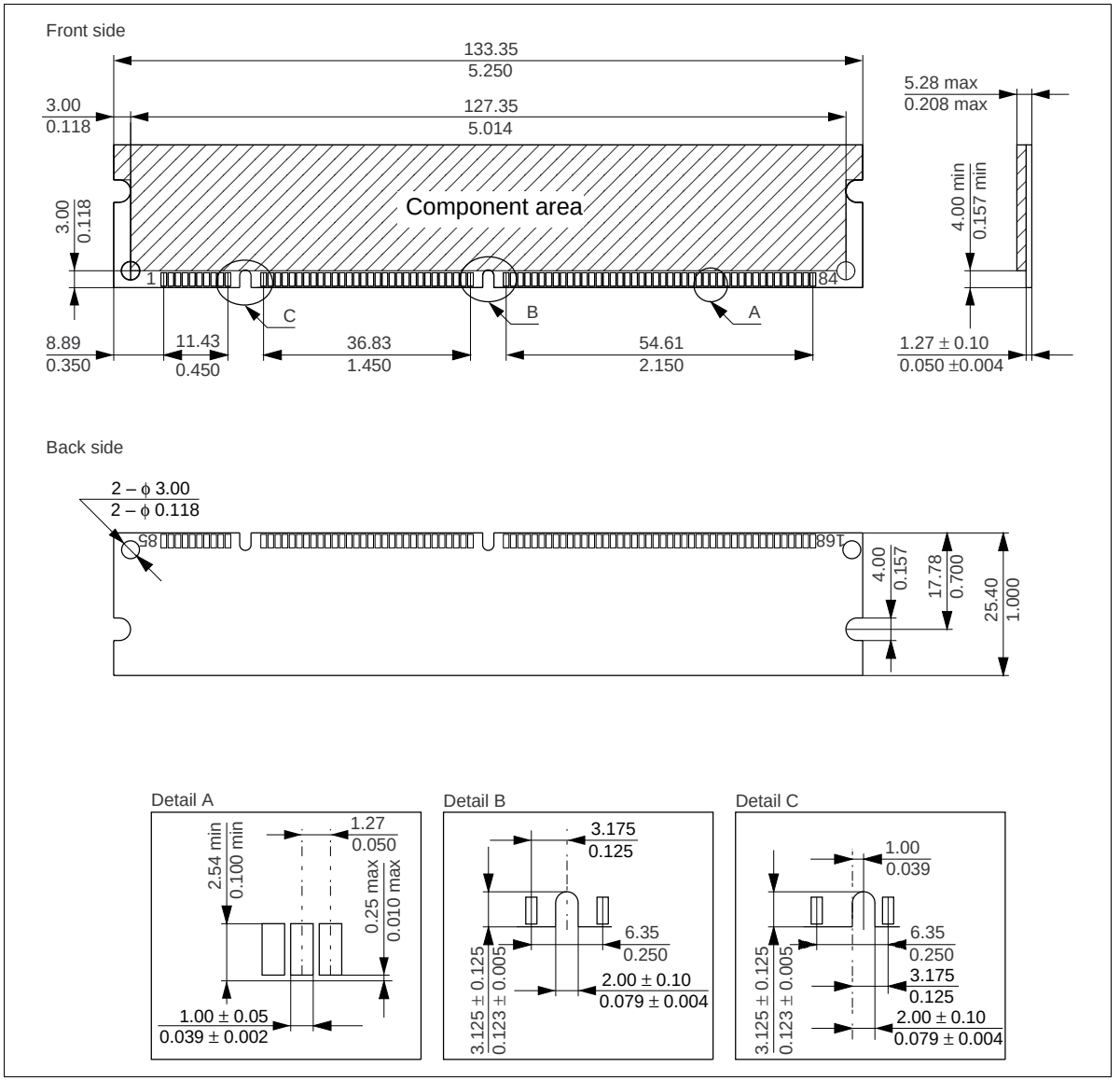


Self Refresh Cycle (L-version)* [23, 24, 25, 26]



Physical Outline

Unit: mm/inch



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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

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1.0	Jan. 27, 1997	Initial issue		