
HB56U464EJ-6B/7B

4,194,304-word $\times$ 64-bit High Density Dynamic RAM Module
168-pin JEDEC Standard Outline Buffered 8 BYTE DIMM

HITACHI

ADE-203-590(Z)

Preliminary

Rev. 0.0

May. 14, 1996

Description

The HB56U464EJ belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications.

The HB56U464EJ is a $4M \times 64$ dynamic RAM module, mounted 16 pieces of 16-Mbit DRAM (HM5116405BS) sealed in SOJ package, 1 piece of 16-bit BiCMOS line driver (74ABT16244) sealed in TSSOP package and 1 piece of 20-bit BiCMOS line driver (74ABT16827) sealed in TSSOP package.

The HB56U464EJ offers Extended Data Out (EDO) Page Mode as a high speed access mode.

An outline of the HB56U464EJ is 168-pin socket type package (dual lead out).

Therefore, the HB56U464EJ makes high density mounting possible without surface mount technology. The HB56U464EJ provides common data inputs and outputs.

Decoupling capacitors are mounted beneath each SOJ on the module board.

Features

- 168-pin socket type package (Dual lead out)
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time: $t_{RAC} = 60/70$ ns (max)
 - Access time: $t_{CAC} = 20/23$ ns (max)
- Low power dissipation
 - Active mode: 7.06/6.22 W (max)
 - Standby mode (TTL): 504 mW (max)
 - Standby mode (CMOS): 420 mW (max)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

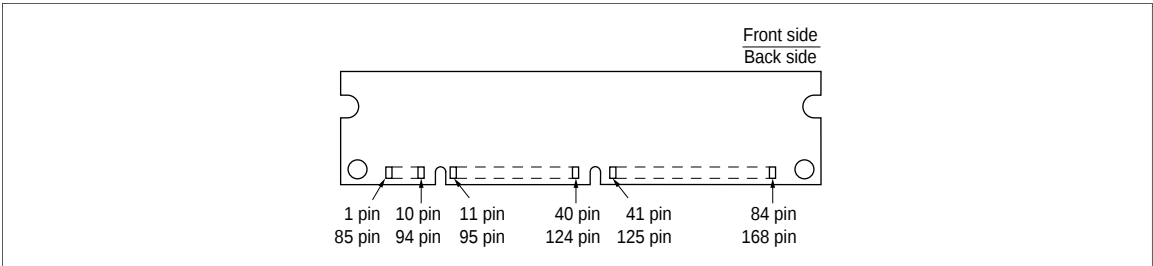
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- Buffered input except RAS and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- EDO page mode capability
- 4,096 refresh cycles: 64 ms
 - RAS-only refresh
 - CAS-before-RAS refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56U464EJ-6B	60 ns	168-pin dual lead out socket type	Gold
HB56U464EJ-7B	70 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	12	V _{SS}	23	V _{SS}	34	A2
2	DQ0	13	DQ9	24	NC	35	A4
3	DQ1	14	DQ10	25	NC	36	A6
4	DQ2	15	DQ11	26	V _{CC}	37	A8
5	DQ3	16	DQ12	27	$\overline{\text{WE0}}$	38	A10
6	V _{CC}	17	DQ13	28	$\overline{\text{CE0}}$	39	NC
7	DQ4	18	V _{CC}	29	$\overline{\text{CE2}}$	40	V _{CC}
8	DQ5	19	DQ14	30	$\overline{\text{RE0}}$	41	NC
9	DQ6	20	DQ15	31	$\overline{\text{OE0}}$	42	NC
10	DQ7	21	DQ16	32	V _{SS}	43	V _{SS}
11	NC	22	NC	33	A0	44	$\overline{\text{OE2}}$

Pin Arrangement (cont)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
45	$\overline{\text{RE2}}$	76	DQ34	107	V _{SS}	138	V _{SS}
46	$\overline{\text{CE4}}$	77	NC	108	NC	139	DQ56
47	$\overline{\text{CE6}}$	78	V _{SS}	109	NC	140	DQ57
48	$\overline{\text{WE2}}$	79	PD1	110	V _{CC}	141	DQ58
49	V _{CC}	80	PD3	111	NC	142	DQ59
50	NC	81	PD5	112	$\overline{\text{CE1}}$	143	V _{CC}
51	NC	82	PD7	113	$\overline{\text{CE3}}$	144	DQ60
52	DQ18	83	ID0 (V _{SS})	114	NC	145	NC
53	DQ19	84	V _{CC}	115	NC	146	NC
54	V _{SS}	85	V _{SS}	116	V _{SS}	147	NC
55	DQ20	86	DQ36	117	A1	148	NC
56	DQ21	87	DQ37	118	A3	149	DQ61
57	DQ22	88	DQ38	119	A5	150	NC
58	DQ23	89	DQ39	120	A7	151	DQ63
59	V _{CC}	90	V _{CC}	121	A9	152	V _{SS}
60	DQ24	91	DQ40	122	A11	153	DQ64
61	NC	92	DQ41	123	NC	154	DQ65
62	NC	93	DQ42	124	V _{CC}	155	DQ66
63	NC	94	DQ43	125	NC	156	DQ67
64	NC	95	NC	126	B0	157	V _{CC}
65	DQ25	96	V _{SS}	127	V _{SS}	158	DQ68
66	NC	97	DQ45	128	NC	159	DQ69
67	DQ27	98	DQ46	129	NC	160	DQ70
68	V _{SS}	99	DQ47	130	$\overline{\text{CE5}}$	161	NC
69	DQ28	100	DQ48	131	$\overline{\text{CE7}}$	162	V _{SS}
70	DQ29	101	DQ49	132	$\overline{\text{PDE}}$	163	PD2
71	DQ30	102	V _{CC}	133	V _{CC}	164	PD4
72	DQ31	103	DQ50	134	NC	165	PD6
73	V _{CC}	104	DQ51	135	NC	166	PD8
74	DQ32	105	DQ52	136	DQ54	167	ID1 (V _{SS})
75	DQ33	106	NC	137	DQ55	168	V _{CC}

Pin Description

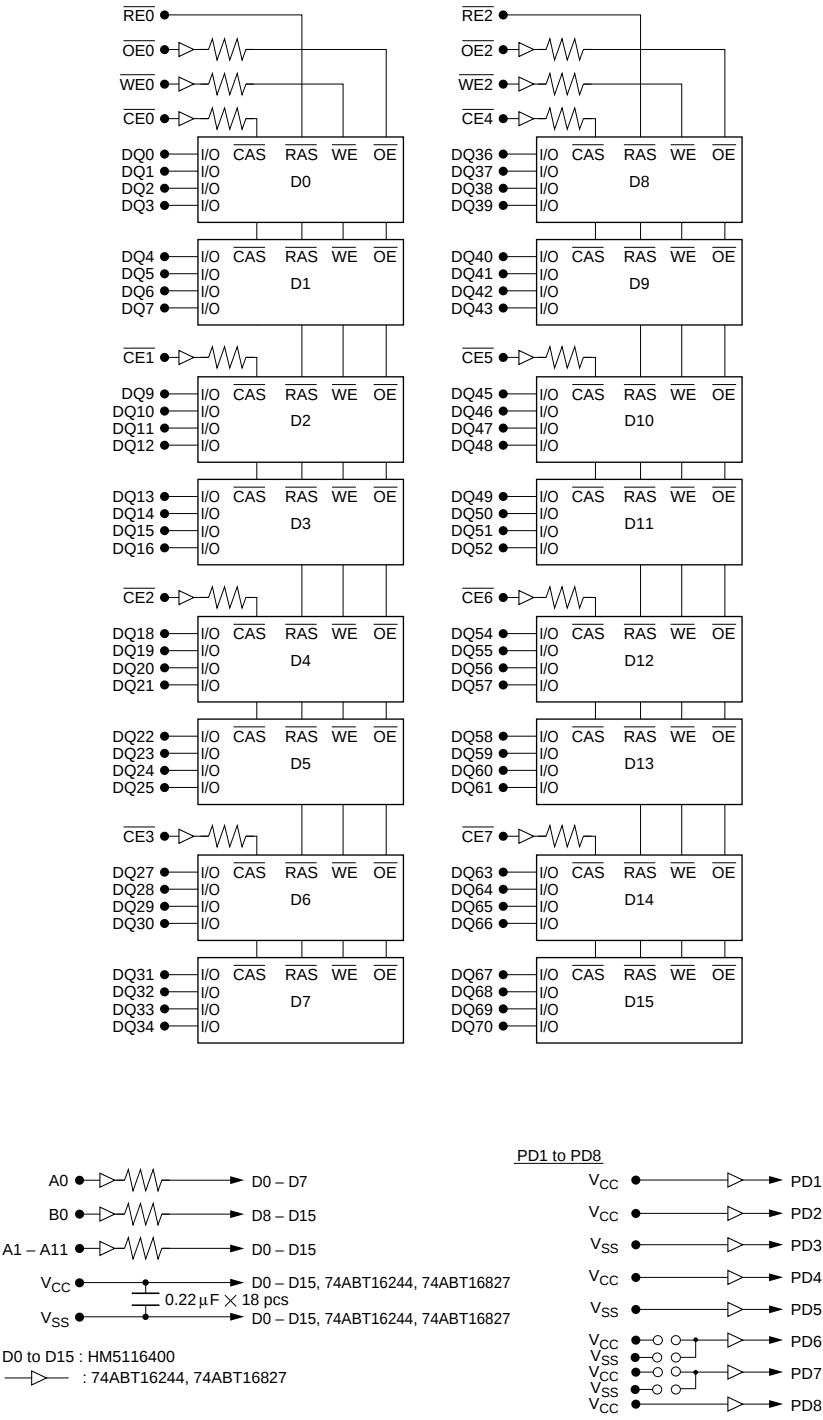
Pin Name	Function
A0 to A11, B0	Address Input : A0 to A11, B0 Row Address : A0 to A11, B0 Column Address : A0 to A9, B0 Refresh Address : A0 to A11, B0
DQ0 to DQ7, DQ9 to DQ16, DQ18 to DQ25, DQ27 to DQ34, DQ36 to DQ43, DQ45 to DQ52, DQ54 to DQ61, DQ63 to DQ70	Data-in/Data-out
RE0, RE2	Row Address Strobe
CE0 to CE7	Column Address Strobe
WE0, WE2	Read/Write Enable
OE0, OE2	Output Enable
V _{cc}	Power Supply
V _{ss}	Ground
PD1 to PD8	Presence Detect
ID0, ID1	ID bit
PDE	Presence Detect Enable
NC	No Connection

Presence Detect Pin Assignment

Pin Name	Pin No.	PDE = Low		PDE = High
		60 ns	70 ns	All
PD1	79	1	1	High-Z
PD2	163	1	1	High-Z
PD3	80	0	0	High-Z
PD4	164	1	1	High-Z
PD5	81	1	1	High-Z
PD6	165	1	0	High-Z
PD7	82	1	1	High-Z
PD8	166	1	1	High-Z

1: High Level (Driver Output)
0: Low Level (Driver Output)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _T	-1.0 to +7.0	V

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Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	17	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−0.5	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS} .

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	60 ns		70 ns		Unit	Test condition	Note
		Min	Max	Min	Max			
Operating current	I_{CC1}	—	1344	—	1184	mA	$t_{RC} = \min$	1, 2
Standby current	I_{CC2}	—	96	—	96	mA	TTL interface $\overline{RAS}, \overline{CAS} = V_{IH}$ Dout = High-Z	
		—	80	—	80	mA	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
$\overline{RAS}$ -only refresh current	I_{CC3}	—	1344	—	1184	mA	$t_{RC} = \min$	2
Standby current	I_{CC5}	—	144	—	144	mA	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ Dout = enable	1
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I_{CC6}	—	1344	—	1184	mA	$t_{RC} = \min$	
EDO page mode current	I_{CC7}	—	1664	—	1504	mA	$t_{HPC} = \min$	1, 3
Input leakage current	I_{LI}	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 5.5\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 5.5\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	71	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{CAS} = V_{IH}$ to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)^{*1, *2, *18, *19}

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	104	—	124	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	13	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	10	10000	13	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	ns	
Column address hold time	t _{CAH}	10	—	13	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	40	20	47	ns	3
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	ns	4
$\overline{\text{RAS}}$ hold time	t _{RSH}	20	—	23	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	48	—	58	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	—	10	—	ns	
$\overline{\text{OE}}$ to Din delay time	t _{OED}	20	—	23	—	ns	5
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	t _{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	2	50	2	50	ns	7
Refresh period (4,096 cycles)	t _{REF}	—	64	—	64	ms	

Read Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	20	—	23	ns	9, 10, 17
Access time from address	t_{AA}	—	35	—	40	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	20	—	23	ns	9
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	20	—	20	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	20	—	23	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	ns	
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	ns	
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	20	—	20	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	20	—	23	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	ns	

Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15	—	18	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	15	—	18	—	ns	15

Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Read-modify-write cycle time	t _{RWC}	149	—	175	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	87	—	100	—	ns	14
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	37	—	43	—	ns	14
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	52	—	60	—	ns	14
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t _{OEH}	15	—	18	—	ns	

Refresh Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{\text{CAS}}$ setup time (CBR refresh cycle)	t _{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh cycle)	t _{CHR}	10	—	10	—	ns	
$\overline{\text{WE}}$ setup time (CBR refresh cycle)	t _{WRP}	5	—	5	—	ns	
$\overline{\text{WE}}$ hold time (CBR refresh cycle)	t _{WRH}	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	t _{RPC}	0	—	0	—	ns	

EDO Page Mode Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode cycle time	t _{HPC}	25	—	30	—	ns	20
EDO page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	40	—	45	ns	9, 17
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	40	—	45	—	ns	
Output data hold time from $\overline{\text{CAS}}$ low	t _{DOH}	3	—	3	—	ns	9, 17
$\overline{\text{CAS}}$ hold time referenced $\overline{\text{OE}}$	t _{COL}	10	—	13	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ setup time	t _{COP}	5	—	5	—	ns	
Read command hold time from $\overline{\text{CAS}}$ precharge	t _{RCHC}	35	—	40	—	ns	

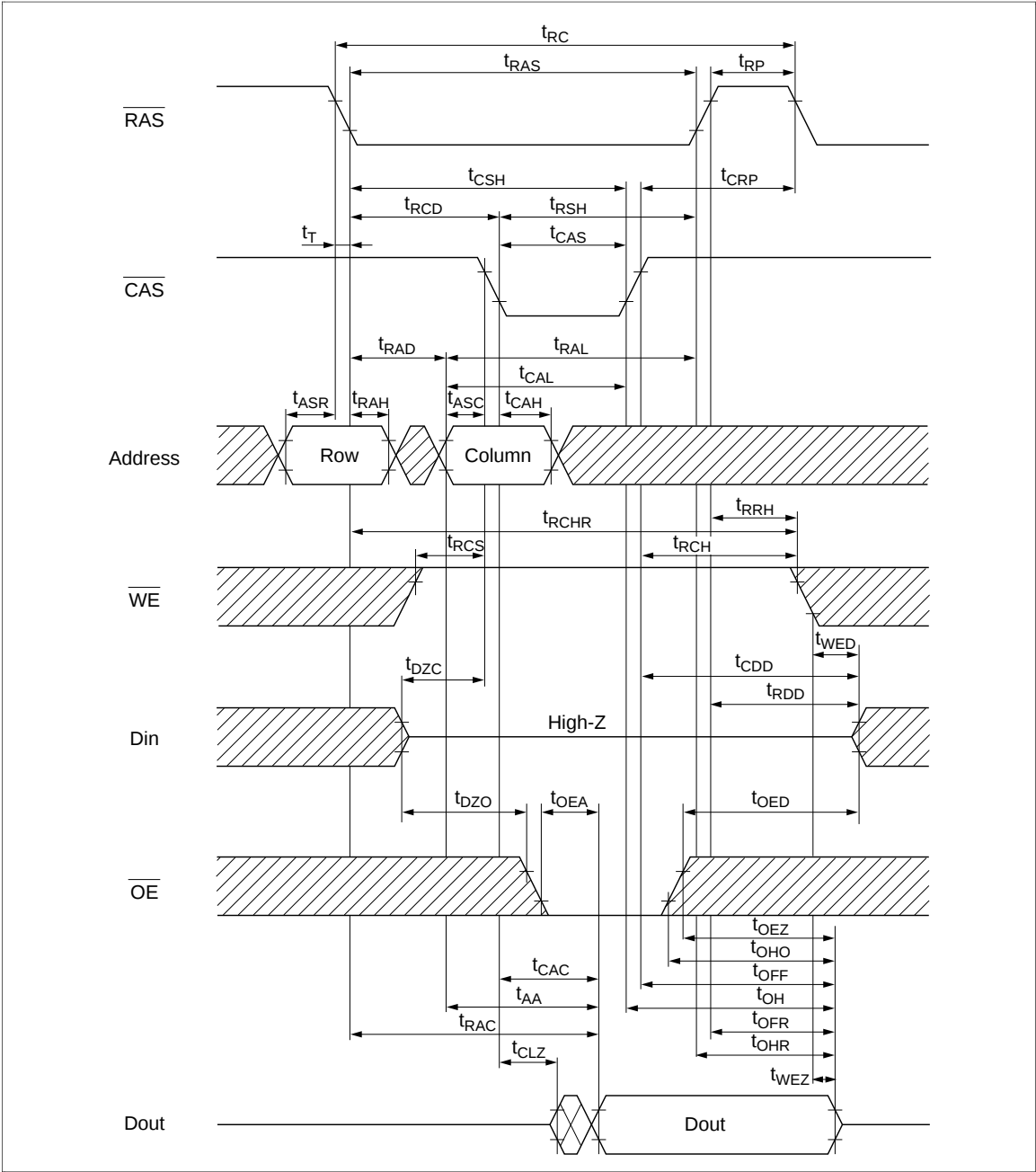
EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	t _{PRWC}	79	—	90	—	ns	
$\overline{\text{WE}}$ delay time from $\overline{\text{CAS}}$ precharge	t _{CPW}	54	—	62	—	ns	14

- Notes:
1. AC measurements assume $t_T = 2 \text{ ns}$.
 2. An initial pause of $200 \mu\text{s}$ is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh).
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1TTL loads and 100 pF.
 10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 11. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. $t_{\text{OFF}} (\text{max})$ and $t_{\text{OEZ}} (\text{max})$ is define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$, and $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ or $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}} (\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycle and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 17. Access time is determined by the longest among t_{AA} or t_{CAC} or t_{CPA} .
 18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device. After $\overline{\text{RAS}}$ is reset, if $t_{\text{OEH}} \geq t_{\text{CWL}}$, the DQ pin will remain open circuit (high impedance); $t_{\text{OEH}} \leq t_{\text{CWL}}$, invalid data will be out at each DQ.
 19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 20. $t_{\text{HPC}} (\text{min})$ can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2t_T$) becomes greater than the specified $t_{\text{HPC}} (\text{min})$ value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
 21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}}/V_{\text{SS}}$ line noise, which causes to degrade $V_{\text{IH}} \text{ min}/V_{\text{IL}} \text{ max}$ level.

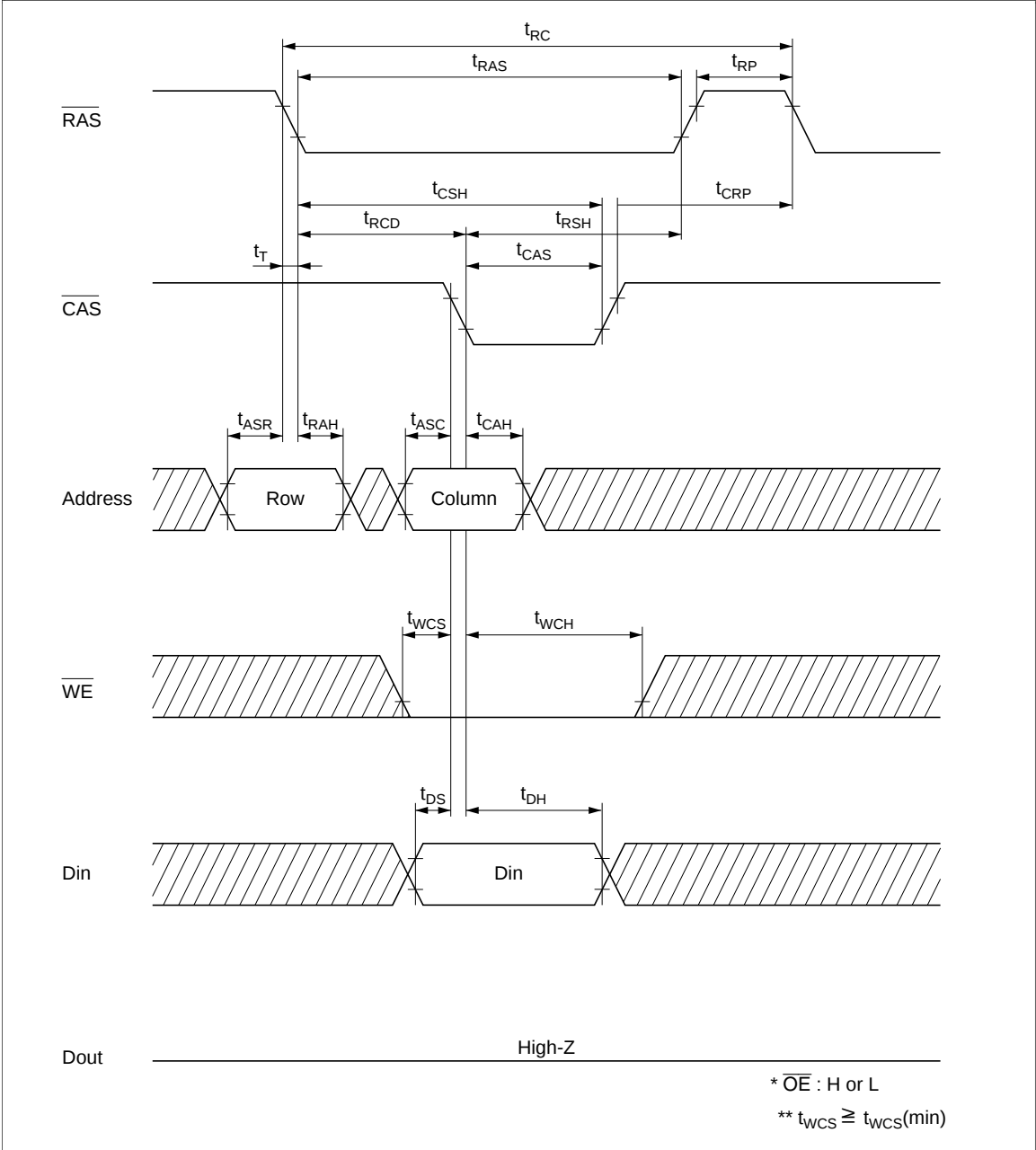
Timing Waveforms*22

Read Cycle

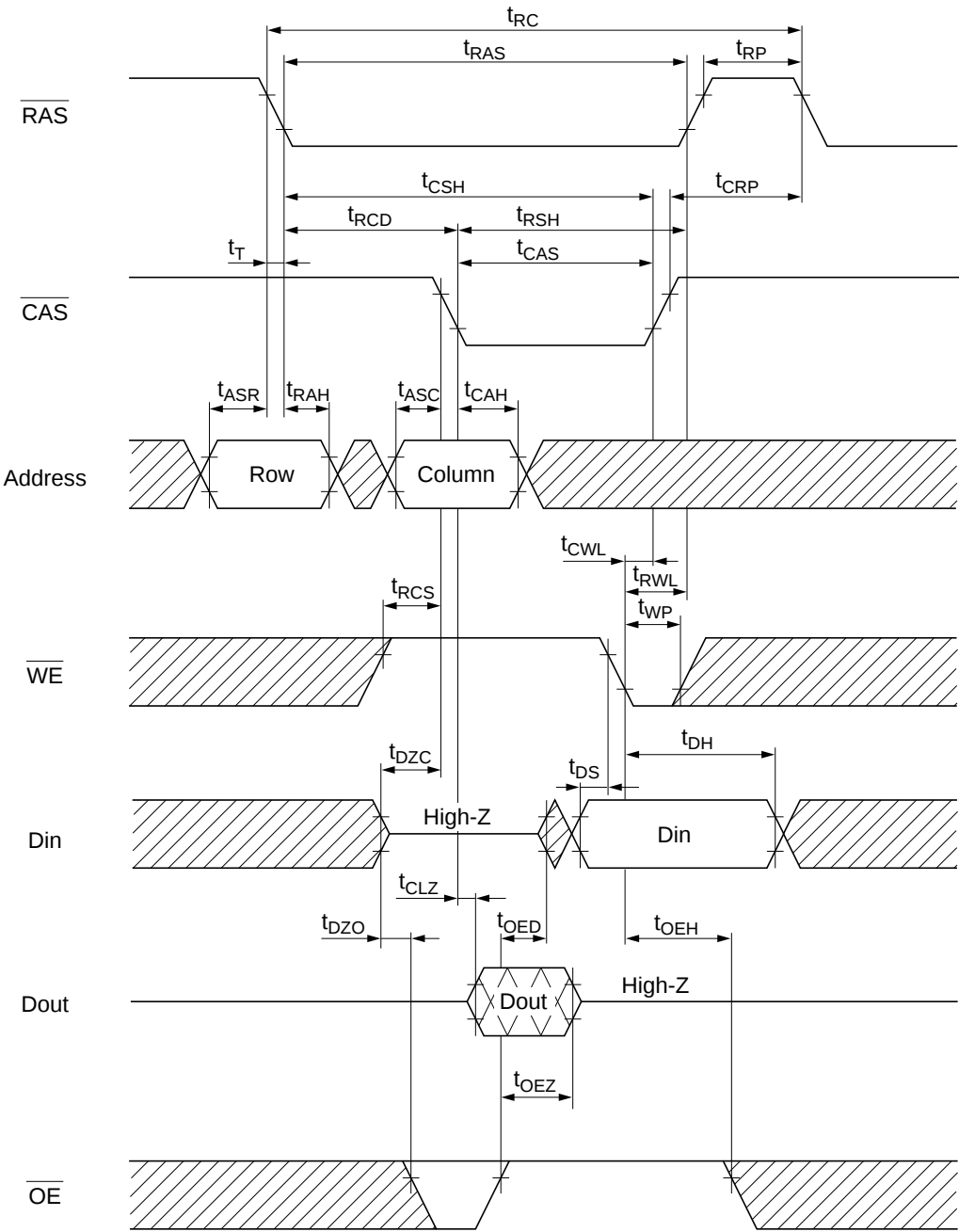


Note : 22.  : H or L (H: $V_{\text{IH}}(\text{min}) \leq V_{\text{in}} \leq V_{\text{IH}}(\text{max})$, L: $V_{\text{IL}}(\text{min}) \leq V_{\text{in}} \leq V_{\text{IL}}(\text{max})$)
 : Invalid Dout

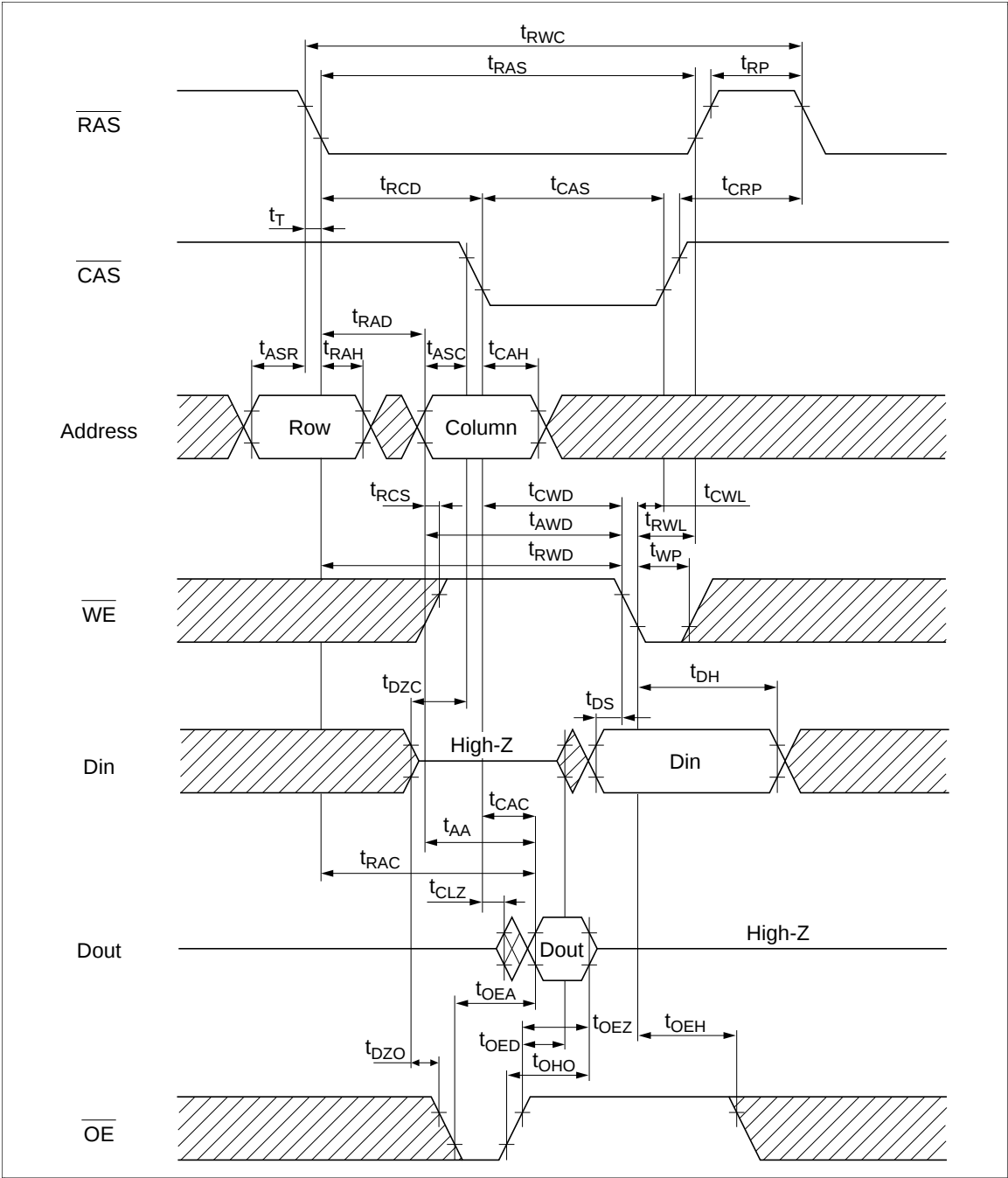
Early Write Cycle



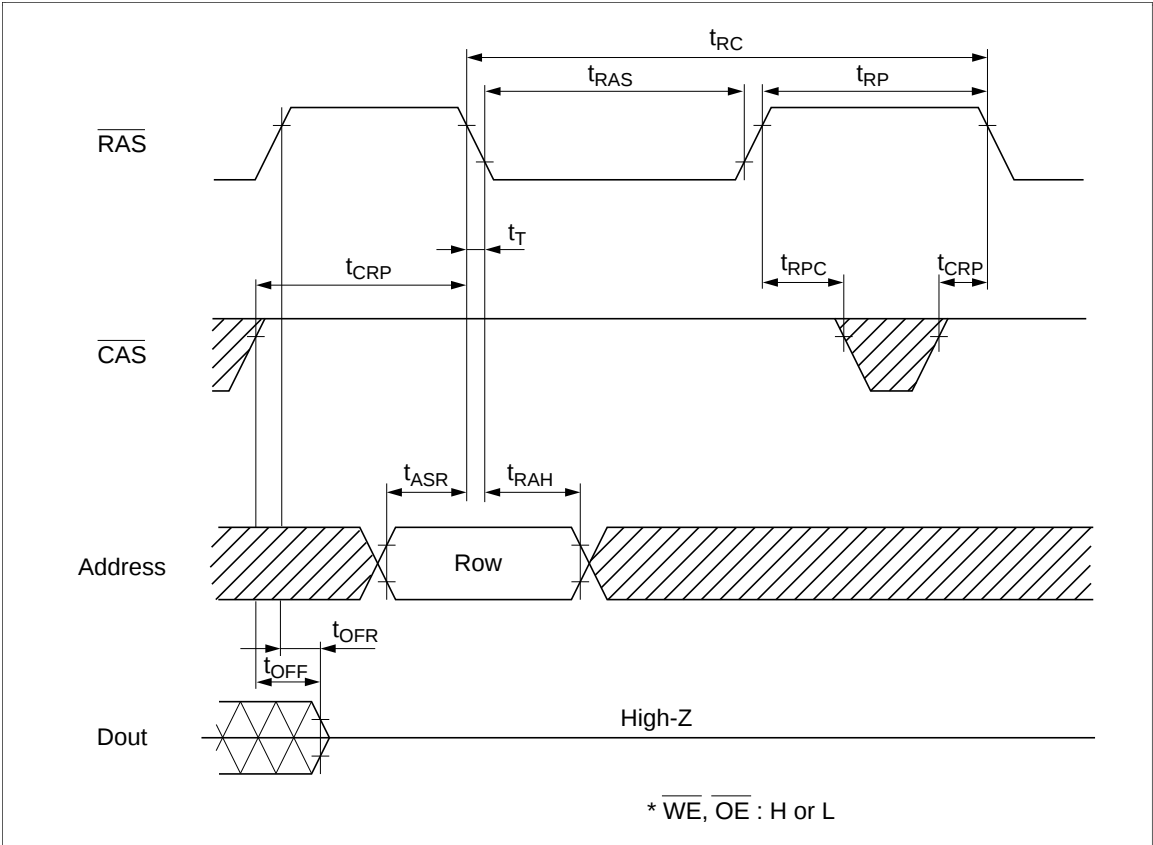
Delayed Write Cycle



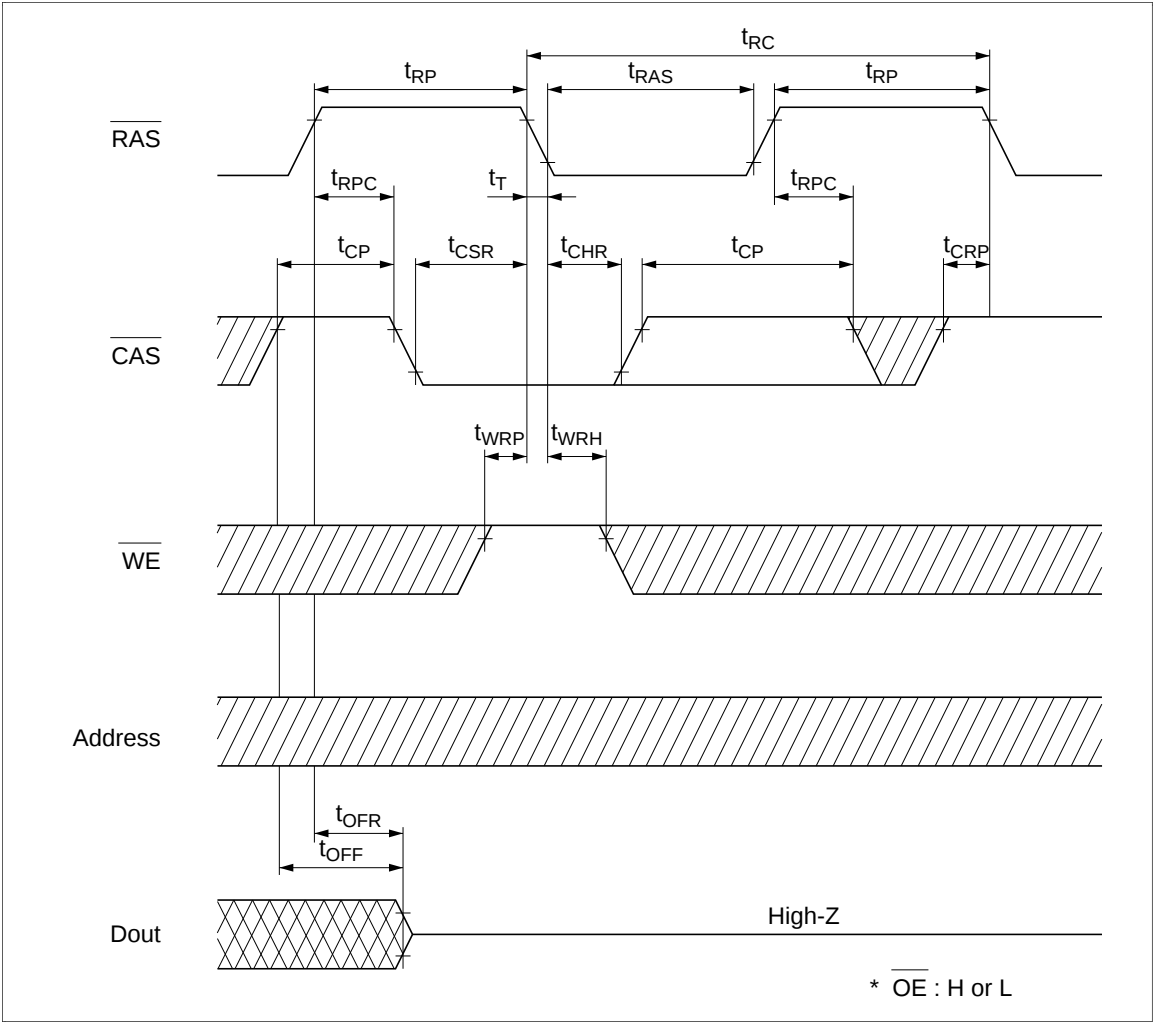
Read-Modify-Write Cycle



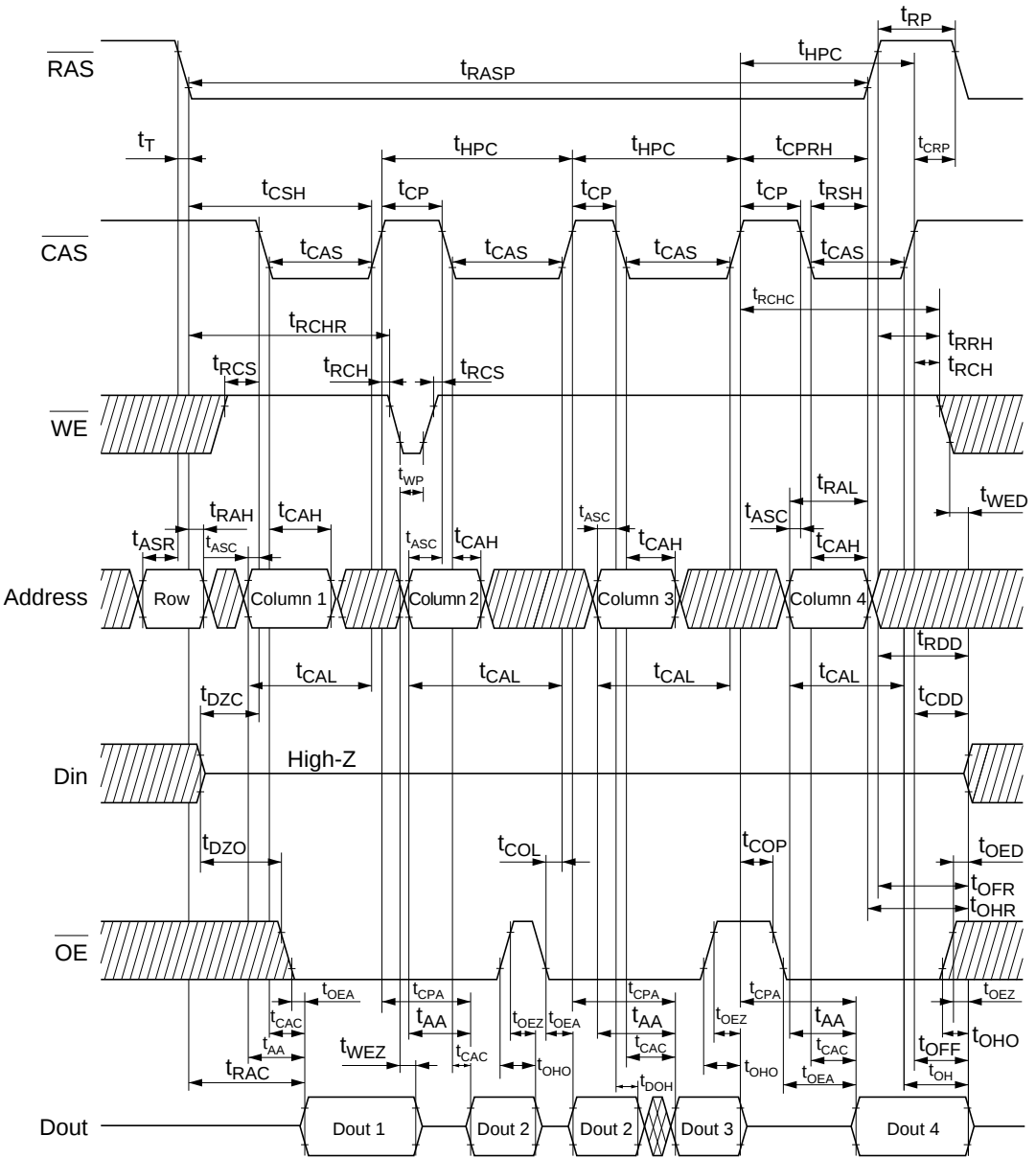
RAS-Only Refresh Cycle



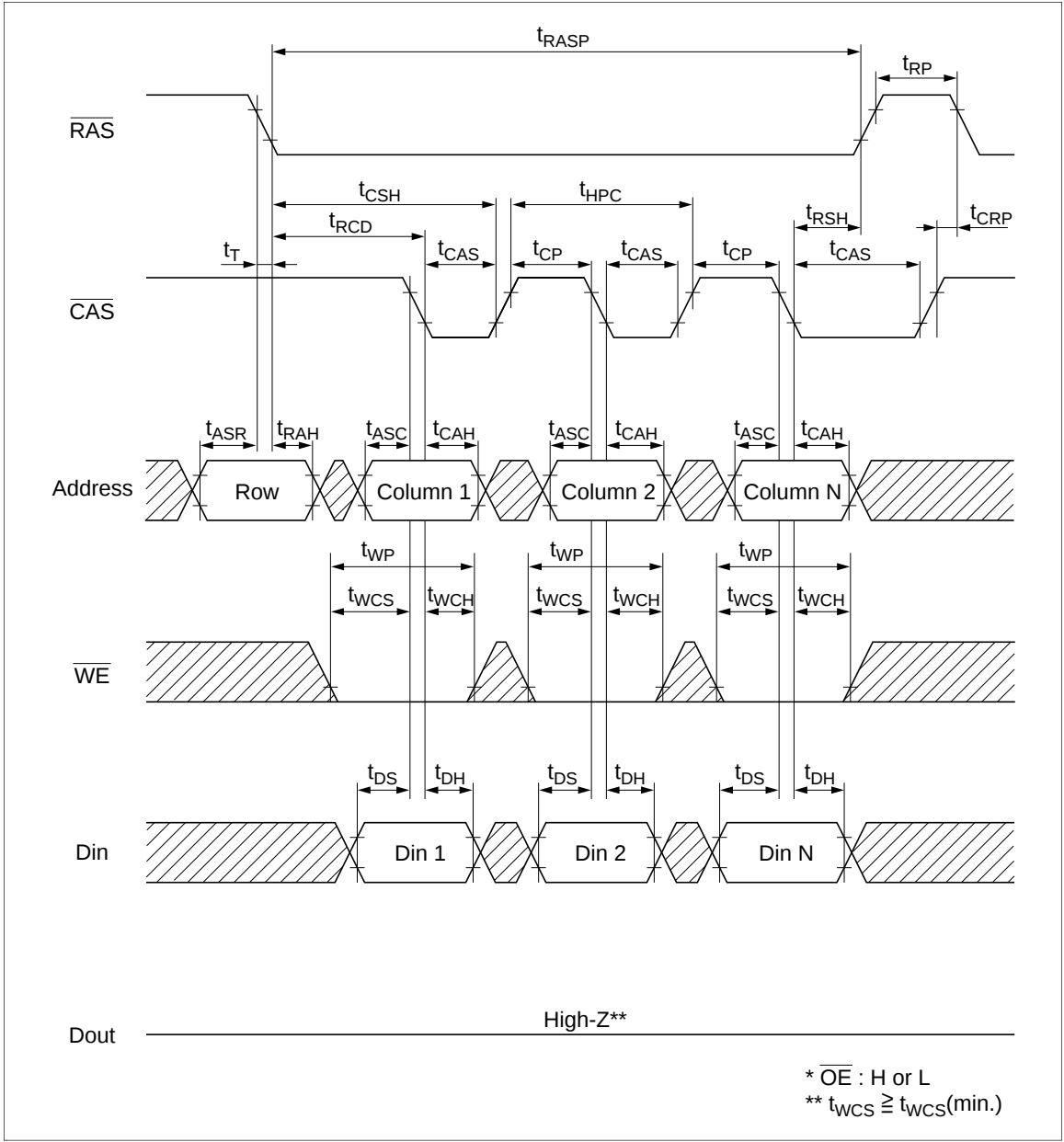
CAS-Before-RAS Refresh Cycle



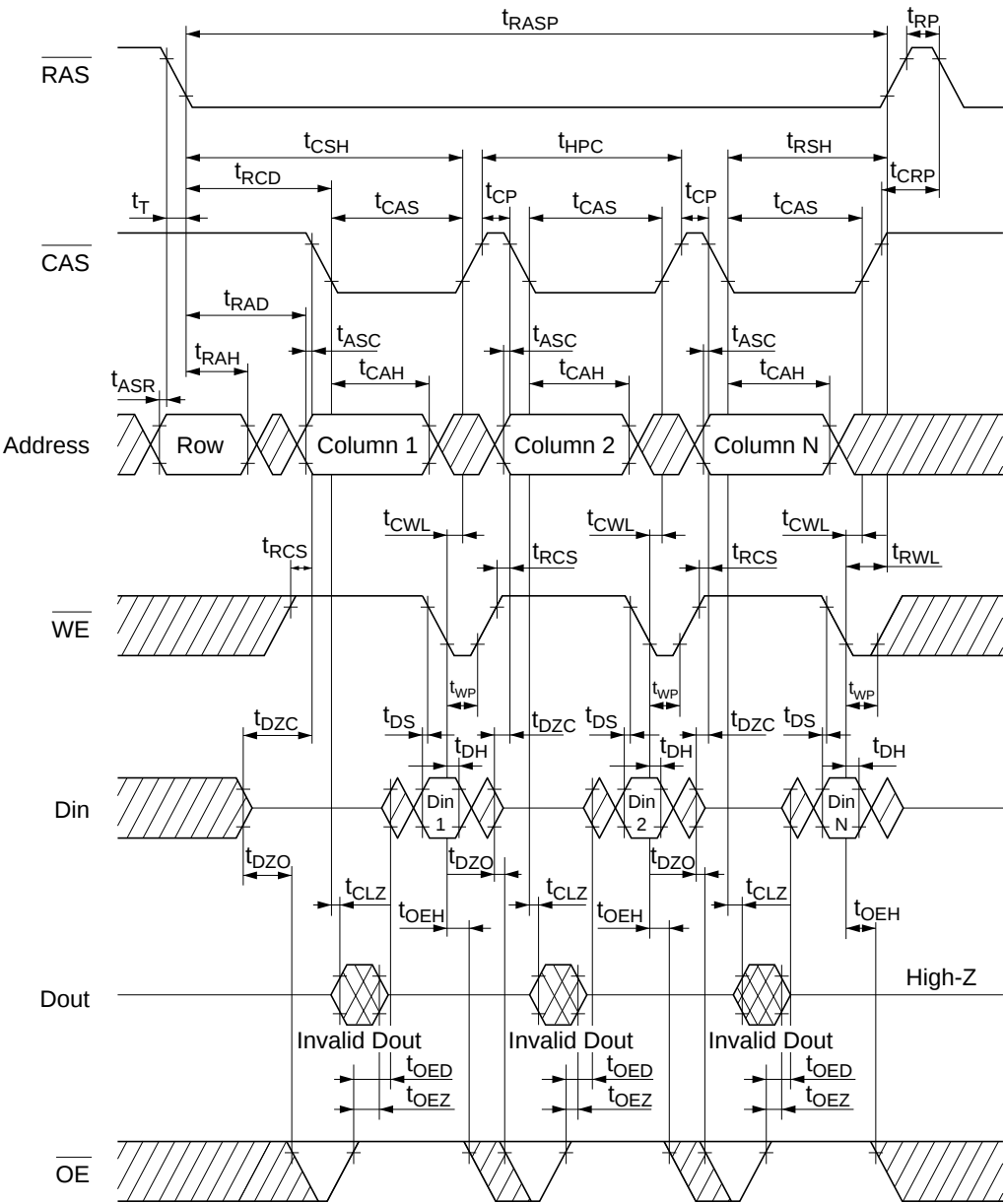
EDO Page Mode Read Cycle



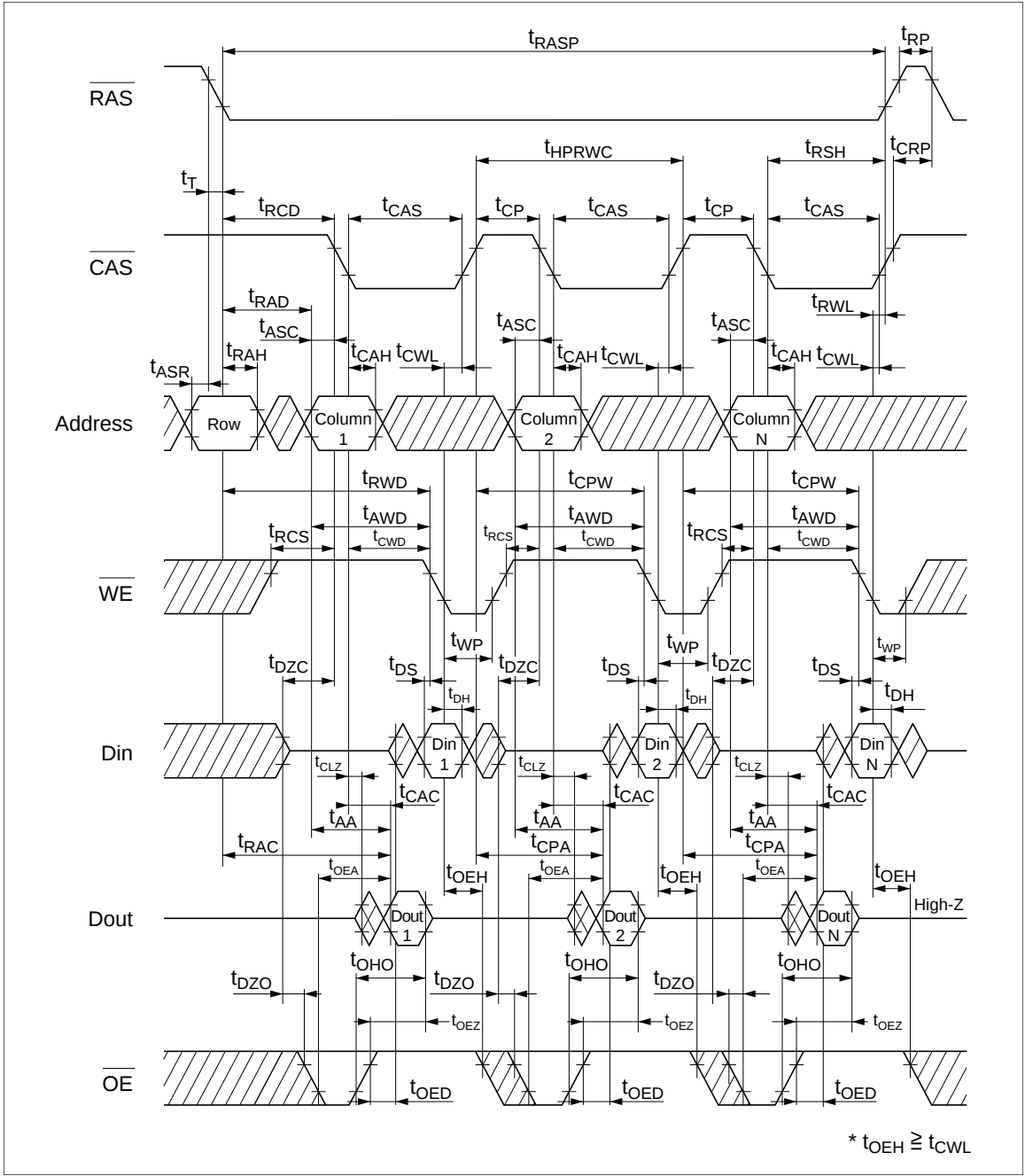
EDO Page Mode Early Write Cycle



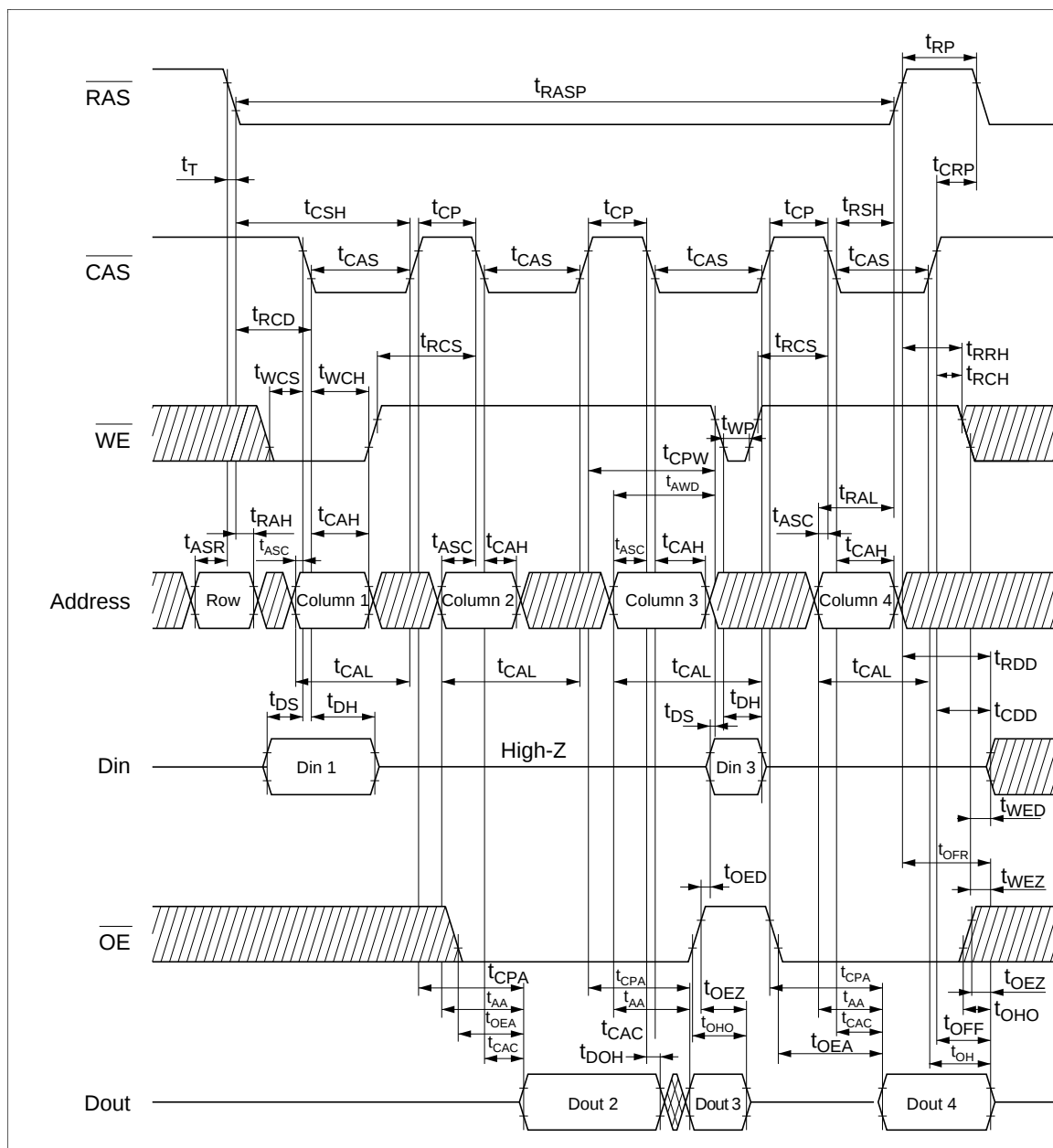
EDO Page Mode Delayed Write Cycle



EDO Page Mode Read-Modify-Write Cycle

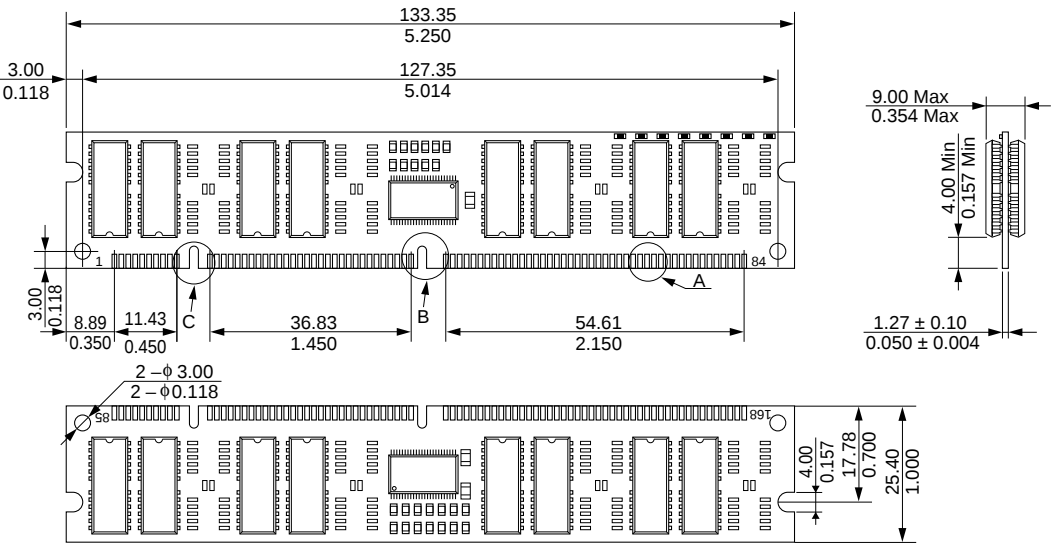


EDO Page Mode Mix Cycle (1)

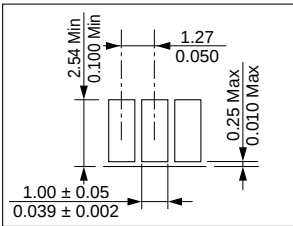


Physical Outline

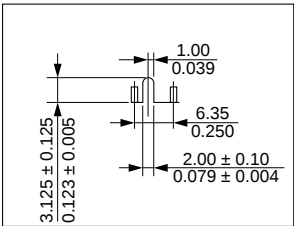
Unit: mm/inch



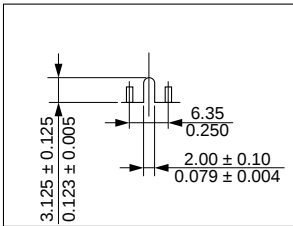
Detail A



Detail B



Detail C



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