HB56SW872ESNJ Series, HB56SW864ESNJ Series

8,388,608-word × 72-bit High Density Dynamic RAM Module
8,388,608-word × 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-764A (Z)
Rev. 1.0
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Description

The HB56SW872ESNJ, HB56SW864ESNJ belong to 8 Byte DIMM (Dual In-line Memory Module) family, and have been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56SW872ESNJ is a 8M × 72 dynamic RAM module, mounted 36 pieces of 16-Mbit DRAM (HM51W17405) sealed in TCP package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56SW864ESNJ is a 8M × 64 dynamic RAM module, mounted 32 pieces of 16-Mbit DRAM (HM51W17405) sealed in TCP package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56SW872ESNJ, HB56SW864ESNJ offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56SW872ESNJ, HB56SW864ESNJ is 168-pin socket type package (dual lead out). Therefore, the HB56SW872ESNJ, HB56SW864ESNJ make high density mounting possible without surface mount technology. The HB56SW872ESNJ, HB56SW864ESNJ provide common data inputs and outputs. Decoupling capacitors are mounted beneath each TCP on the module board.

Features

- 168-pin socket type package (Dual lead out)
  - — Lead pitch: 1.27 mm
- Single 3.3 V (+0.3 V/ –0.15 V) supply
- JEDEC standard outline unbufferd 8 byte DIMM
- High speed
  - — Access time: t_{RAC} = 60/70 ns (max)
    t_{CAC} = 15/18 ns (max)
- Low power dissipation
  - — Active mode: 6.16/5.51 W (max) (HB56SW872ESNJ)
    5.47/4.90 W (max) (HB56SW864ESNJ)

Hitachi semiconductor

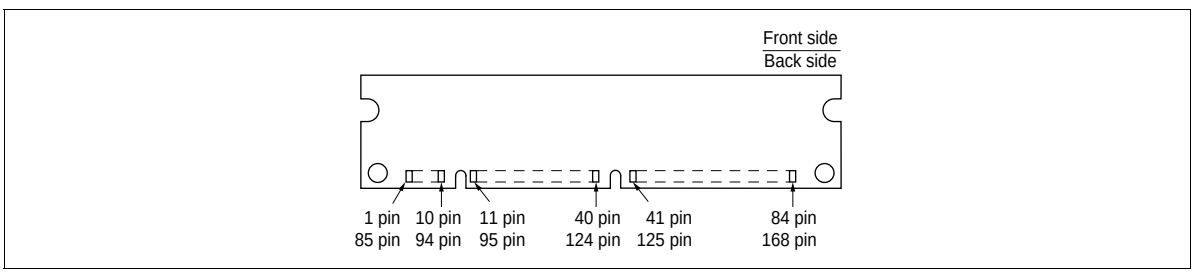
— Standby mode (TTL): 259 mW (max) (HB56SW872ESNJ)
(TTL): 230 mW (max) (HB56SW864ESNJ)
(CMOS): 130 mW (max) (HB56SW872ESNJ)
(CMOS): 115 mW (max) (HB56SW864ESNJ)

- EDO page mode capability
- 2,048 refresh cycle: 32 ms
- 2 variations of refresh
  — $\overline{\text{RAS}}$-only refresh
  — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

Ordering Information

Type No.	Access time	Package	Contact pad
HB56SW872ESNJ-6	60 ns	168-pin dual lead out socket type	Gold
HB56SW872ESNJ-7	70 ns		
HB56SW864ESNJ-6	60 ns		
HB56SW864ESNJ-7	70 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	36	A6	71	DQ26	106	CB5 (NC)*[6]
2	DQ0	37	A8	72	DQ27	107	V_{SS}
3	DQ1	38	A10	73	V_{CC}	108	NC
4	DQ2	39	NC	74	DQ28	109	NC
5	DQ3	40	V_{CC}	75	DQ29	110	V_{CC}
6	V_{CC}	41	V_{CC}	76	DQ30	111	NC
7	DQ4	42	NC	77	DQ31	112	$\overline{CAS4}$
8	DQ5	43	V_{SS}	78	V_{SS}	113	$\overline{CAS5}$
9	DQ6	44	$\overline{OE2}$	79	NC	114	$\overline{RAS1}$
10	DQ7	45	$\overline{RAS2}$	80	NC	115	NC
11	DQ8	46	$\overline{CAS2}$	81	NC	116	V_{SS}
12	V_{SS}	47	$\overline{CAS3}$	82	SDA	117	A1
13	DQ9	48	$\overline{WE2}$	83	SCL	118	A3
14	DQ10	49	V_{CC}	84	V_{CC}	119	A5
15	DQ11	50	NC	85	V_{SS}	120	A7
16	DQ12	51	NC	86	DQ32	121	A9
17	DQ13	52	CB2 (NC)*[3]	87	DQ33	122	NC
18	V_{CC}	53	CB3 (NC)*[4]	88	DQ34	123	NC
19	DQ14	54	V_{SS}	89	DQ35	124	V_{CC}
20	DQ15	55	DQ16	90	V_{CC}	125	NC
21	CB0 (NC)*[1]	56	DQ17	91	DQ36	126	NC
22	CB1 (NC)*[2]	57	DQ18	92	DQ37	127	V_{SS}
23	V_{SS}	58	DQ19	93	DQ38	128	NC
24	NC	59	V_{CC}	94	DQ39	129	$\overline{RAS3}$
25	NC	60	DQ20	95	DQ40	130	$\overline{CAS6}$
26	V_{CC}	61	NC	96	V_{SS}	131	$\overline{CAS7}$
27	$\overline{WE0}$	62	NC	97	DQ41	132	NC
28	$\overline{CAS0}$	63	NC	98	DQ42	133	V_{CC}
29	$\overline{CAS1}$	64	V_{SS}	99	DQ43	134	NC
30	$\overline{RAS0}$	65	DQ21	100	DQ44	135	NC
31	$\overline{OE0}$	66	DQ22	101	DQ45	136	CB6 (NC)*[7]
32	V_{SS}	67	DQ23	102	V_{CC}	137	CB7 (NC)*[8]
33	A0	68	V_{SS}	103	DQ46	138	V_{SS}
34	A2	69	DQ24	104	DQ47	139	DQ48
35	A4	70	DQ25	105 (NC)*[5]	CB4	140	DQ49

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
141	DQ50	148	V_{SS}	155	DQ58	162	V_{SS}
142	DQ51	149	DQ53	156	DQ59	163	NC
143	V_{CC}	150	DQ54	157	V_{CC}	164	NC
144	DQ52	151	DQ55	158	DQ60	165	SA0
145	NC	152	V_{SS}	159	DQ61	166	SA1
146	NC	153	DQ56	160	DQ62	167	SA2
147	NC	154	DQ57	161	DQ63	168	V_{CC}

Notes:
1. CB0: HB56SW872ESNJ, NC: HB56SW864ESNJ
2. CB1: HB56SW872ESNJ, NC: HB56SW864ESNJ
3. CB2: HB56SW872ESNJ, NC: HB56SW864ESNJ
4. CB3: HB56SW872ESNJ, NC: HB56SW864ESNJ
5. CB4: HB56SW872ESNJ, NC: HB56SW864ESNJ
6. CB5: HB56SW872ESNJ, NC: HB56SW864ESNJ
7. CB6: HB56SW872ESNJ, NC: HB56SW864ESNJ
8. CB7: HB56SW872ESNJ, NC: HB56SW864ESNJ

Pin Description

Pin name	Function
A0 to A10	Address input — Row address: A0 to A10 — Column address: A0 to A10 — Refresh address: A0 to A10
DQ0 to DQ63	Data-in/data-out
$\overline{RAS0}$ to $\overline{RAS3}$	Row address strobe
$\overline{CAS0}$ to $\overline{CAS7}$	Column address strobe
$\overline{WE0}$, $\overline{WE2}$	Read/Write enable
$\overline{OE0}$, $\overline{OE2}$	Output enable
SDA	Serial data out (Bit0 to 7)
SCL	Clock for presence detect
SA0 to SA2	Serial address input
CB0 to CB7*[1]	Check bit
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

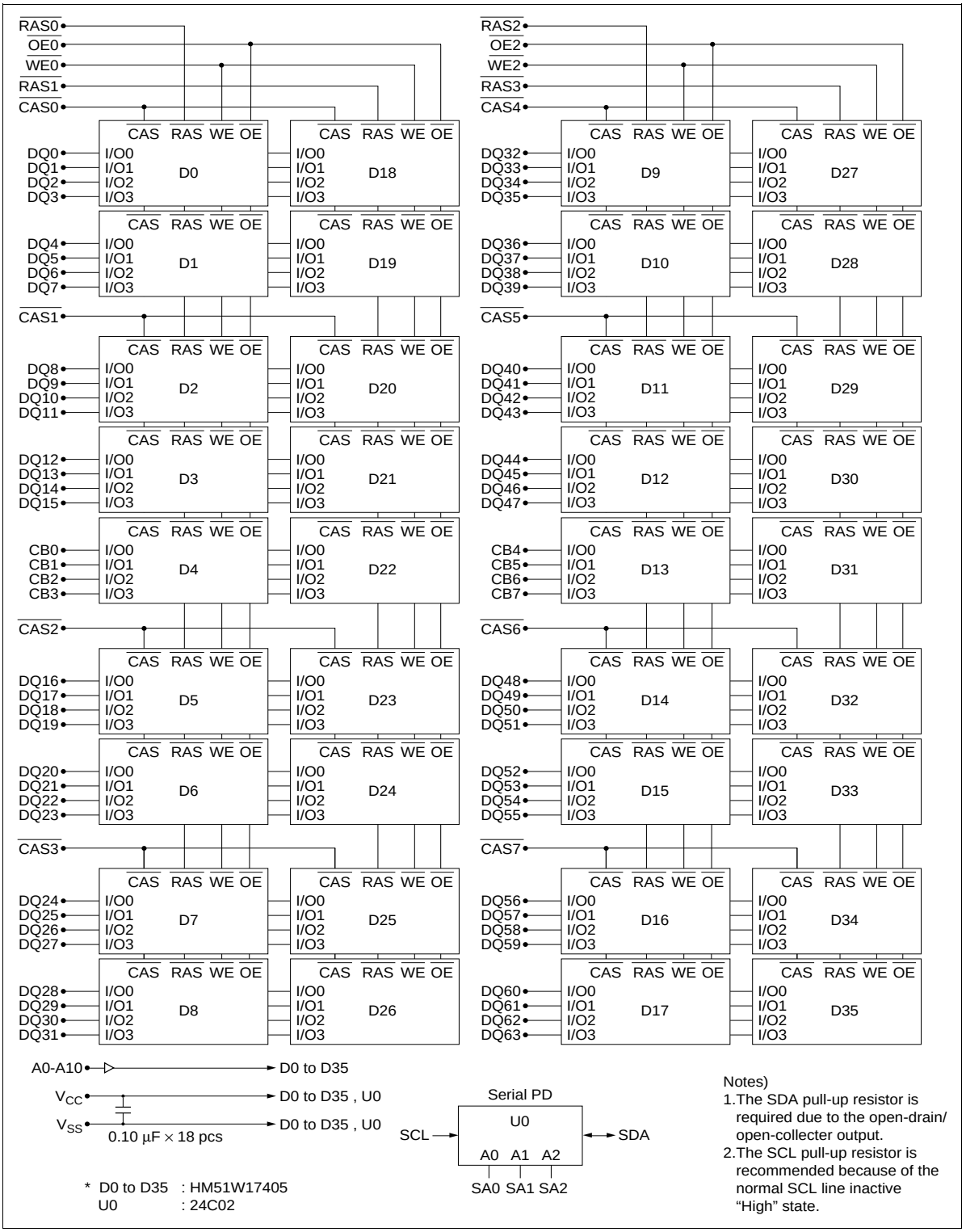
Note: 1. This function is supported only HB56SW872ESNJ.

Serial PD Matrix*[1]

Byte number	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment
0	Number serial PD bytes	0	0	0	0	1	1	0	1	13
1	Serial memory	0	0	0	0	1	0	0	0	256 Bytes
2	Fundamental memory type	0	0	0	0	0	0	1	0	EDO
3	Number of rows	0	0	0	0	1	0	1	1	11
4	Number of columns	0	0	0	0	1	0	1	1	11
5	Number of banks	0	0	0	0	0	0	1	0	2
6	Data width (HB56SW872ESNJ)	0	1	0	0	1	0	0	0	72
	Data width (HB56SW864ESNJ)	0	1	0	0	0	0	0	0	64
7	Data width (continued)	0	0	0	0	0	0	0	0	0 (+)
8	Voltage interface	0	0	0	0	0	0	0	1	3.3 Volt
9	$\overline{RAS}$ access time 60 ns	0	0	1	1	1	1	0	0	
	$\overline{RAS}$ access time 70 ns	0	1	0	0	0	1	1	0	
10	$\overline{CAS}$ access time 15 ns	0	0	0	0	1	1	1	1	
	$\overline{CAS}$ access time 18 ns	0	0	0	1	0	0	1	0	
11	Error detection/corraction (HB56SW872ESNJ)	0	0	0	0	0	0	1	0	ECC
	Error detection/corraction (HB56SW864ESNJ)	0	0	0	0	0	0	0	0	Non-parity
12	Refresh period	0	0	0	0	0	0	0	0	Normal (15.625 μs)

Note: 1. Serial-PD Datas are not protected.
0: Serial Data, “driven to Low”, 1: Serial Data, “driven to High”

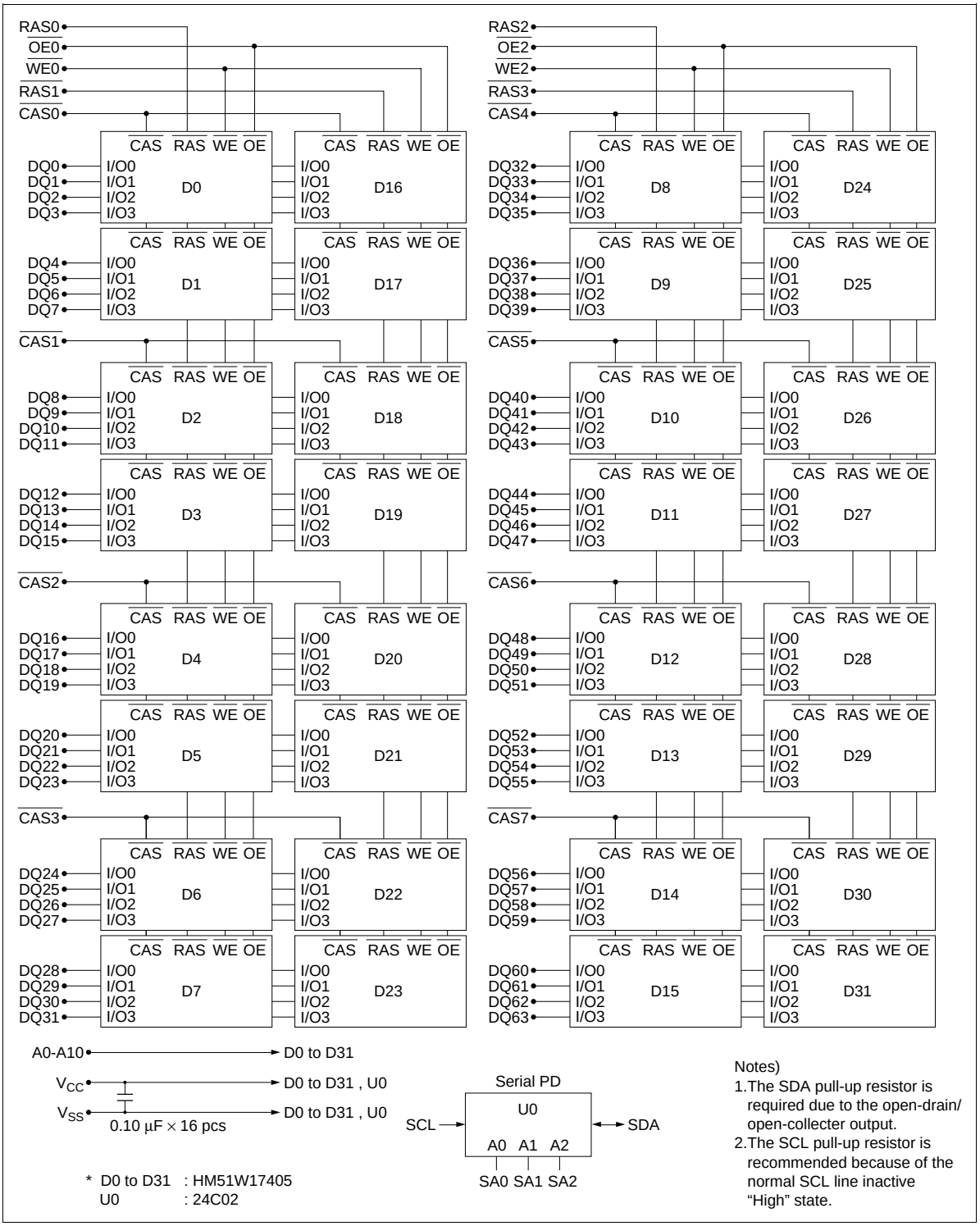
Block Diagram (HB56SW872ESNJ)



* D0 to D35 : HM51W17405
U0 : 24C02

Notes)
1. The SDA pull-up resistor is required due to the open-drain/ open-collecter output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inactive "High" state.

Block Diagram (HB56SW864ESNJ)



* D0 to D31 : HM51W17405
U0 : 24C02

Notes)
1. The SDA pull-up resistor is required due to the open-drain/ open-collecter output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inactive "High" state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}.	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation (HB56SW872ESNJ)	Pt	18	W
Power dissipation (HB56SW864ESNJ)	Pt	16	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.15	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V +0.3 V/ –0.15 V, V_{SS} = 0 V) (HB56SW872ESNJ)

		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	1710	—	1530	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	72	—	72	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	36	—	36	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} –0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	1710	—	1530	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	180	—	180	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1710	—	1530	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	1530	—	1440	mA	t_{HPC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V +0.3 V/ –0.15 V, V_{SS} = 0 V) (HB56SW864ESNJ)

		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	1520	—	1360	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	64	—	64	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	32	—	32	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} –0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	1520	—	1360	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	160	—	160	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1520	—	1360	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	1360	—	1280	mA	t_{HPC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V +0.3 V/ –0.15 V) (HB56SW872ESNJ)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	200	pF	1
Input capacitance ($\overline{CAS}$)	C_{I2}	—	62	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	83	pF	1
Input capacitance ($\overline{WE}$, $\overline{OE}$)	C_{I4}	—	146	pF	1
Output capacitance (DQ)	$C_{I/O}$	—	27	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V +0.3 V/ –0.15 V) (HB56SW864ESNJ)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	180	pF	1
Input capacitance ($\overline{CAS}$)	C_{I2}	—	48	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	76	pF	1
Input capacitance ($\overline{WE}$, $\overline{OE}$)	C_{I4}	—	132	pF	1
Output capacitance (DQ)	$C_{I/O}$	—	27	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V +0.3 V/ –0.15 V, V_{SS} = 0 V) *1, *2, *18, *19

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	45	14	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	12	30	12	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	13	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7
Refresh period (2,048 cycles)	t_{REF}	—	32	—	32	ms	

Read Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	15	—	18	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{RAS}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	22
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13, 22
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{RAS}$	t_{OFR}	—	15	—	15	ns	22
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	15	—	15	ns	
$\overline{WE}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	15	—	18	—	ns	
$\overline{RAS}$ next $\overline{CAS}$ delay time	t_{RNCD}	60	—	70	—	ns	

Write Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	10	—	13	—	ns	15

Read-Modify-Write Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	49	—	57	—	ns	14
$\overline{OE}$ hold time $\overline{WE}$	t_{OEH}	15	—	18	—	ns	

Refresh Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	

EDO Page Mode Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	ns	
Output data hole time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time refferred $\overline{OE}$	t_{COL}	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read-modify-write cycle time	t_{HPRWC}	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	54	—	62	—	ns	14

Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RAD}$ (max) + t_{AA} (max)- t_{CAC} (max), then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

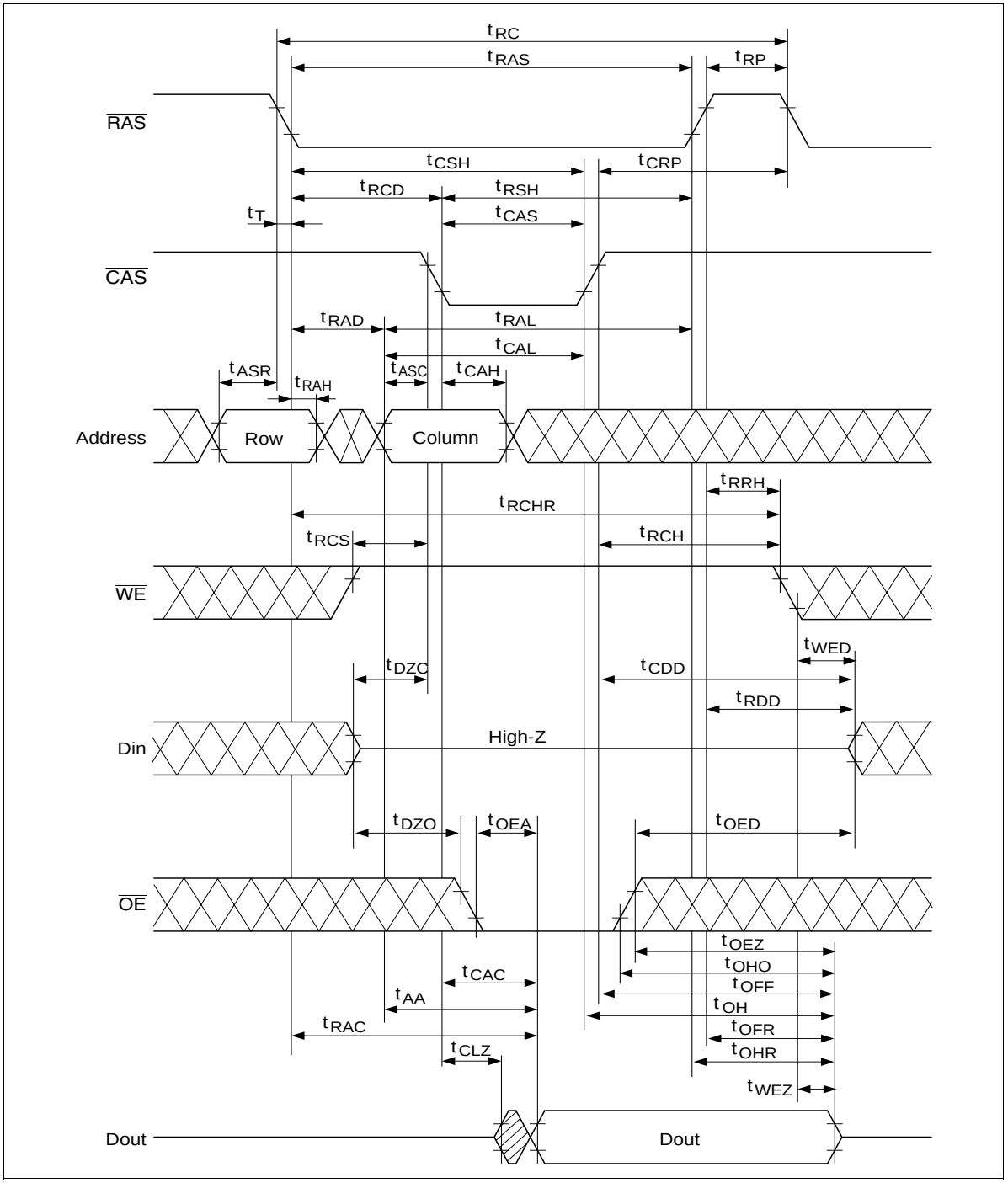
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics onry; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min) or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the DQ pin will remain open circuit (high impedance); $t_{OEH} < t_{OEH}$, invalid data will be out at each DQ.
19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
22. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.
23. XXX: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

    ///////: Invalid Dout

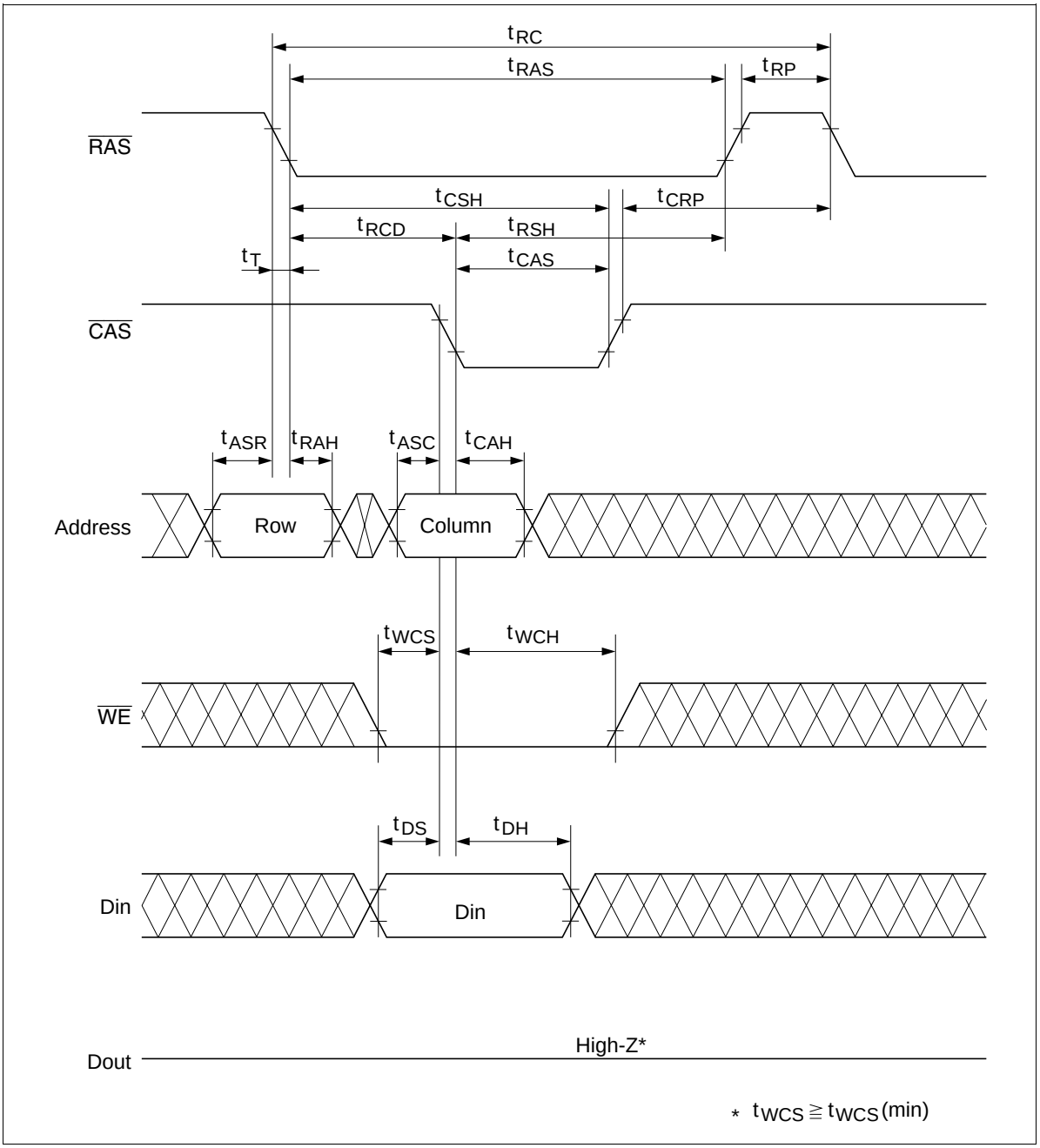
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[23]

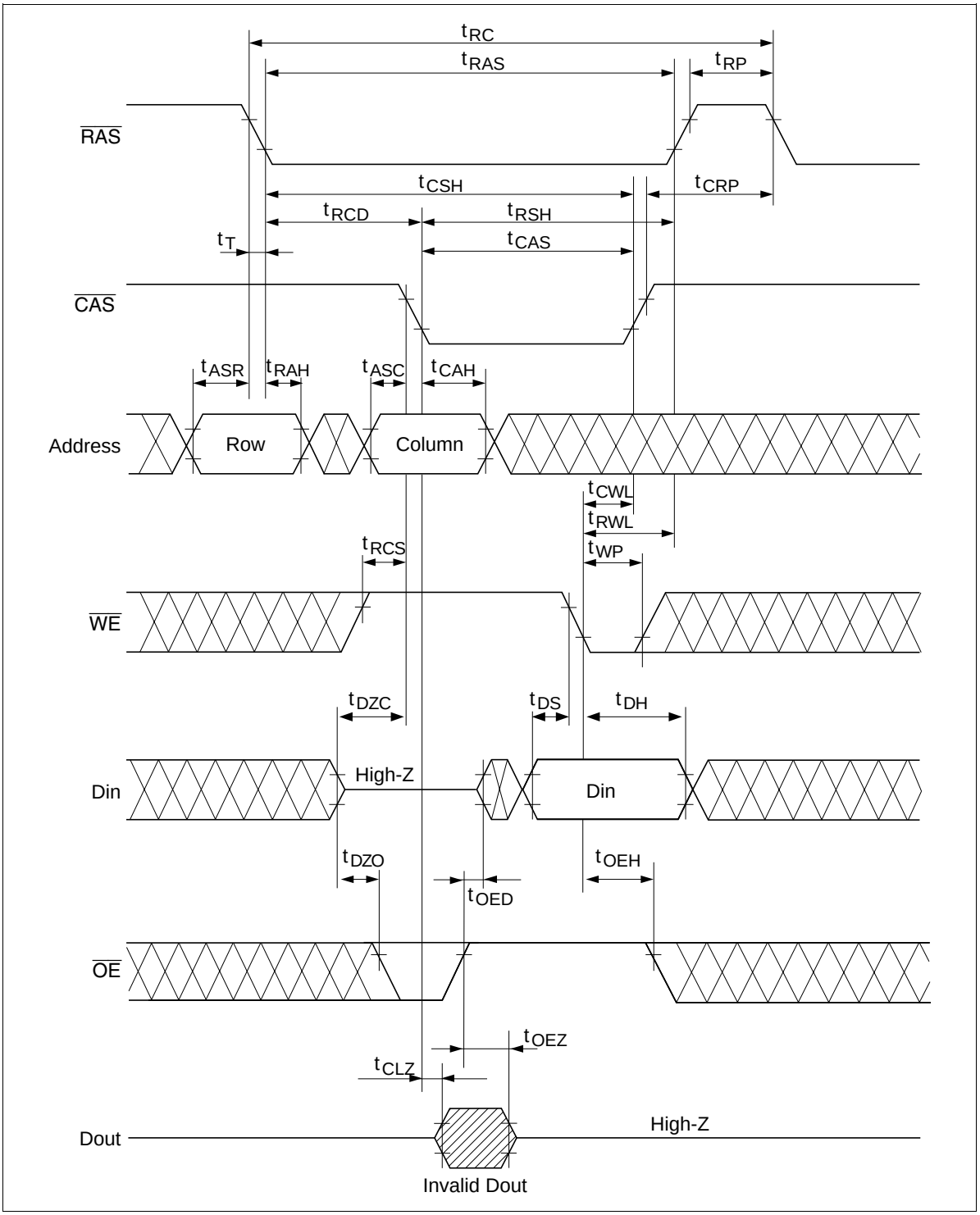
Read Cycle



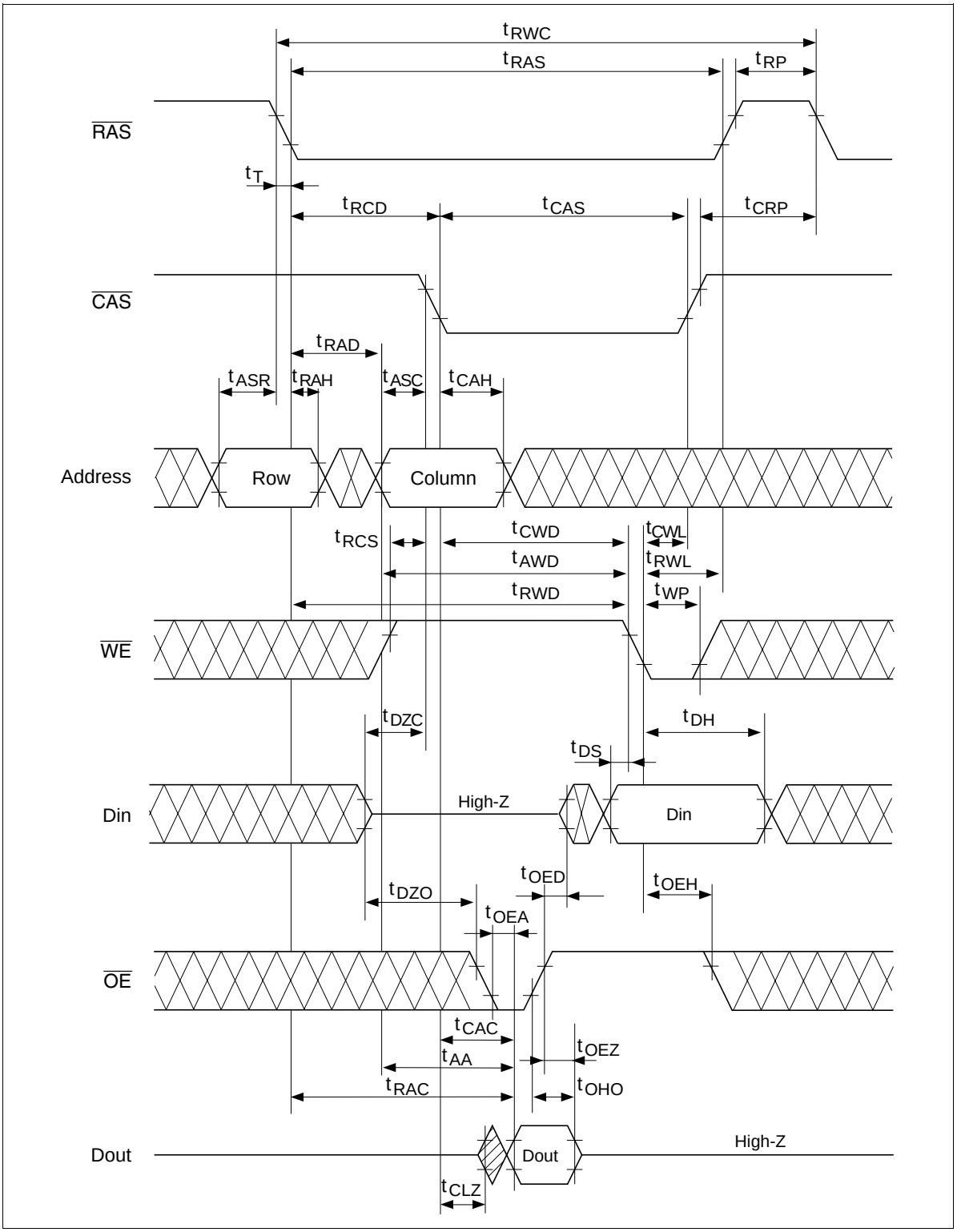
Early Write Cycle



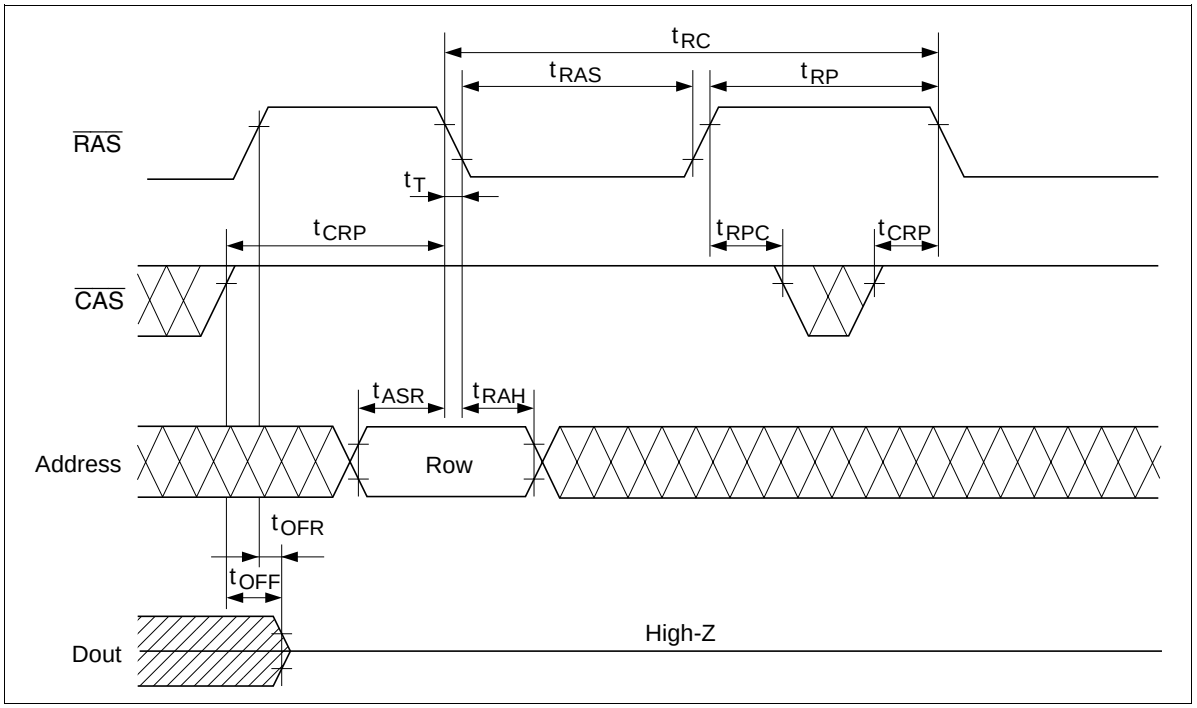
Delayed Write Cycle*[18]



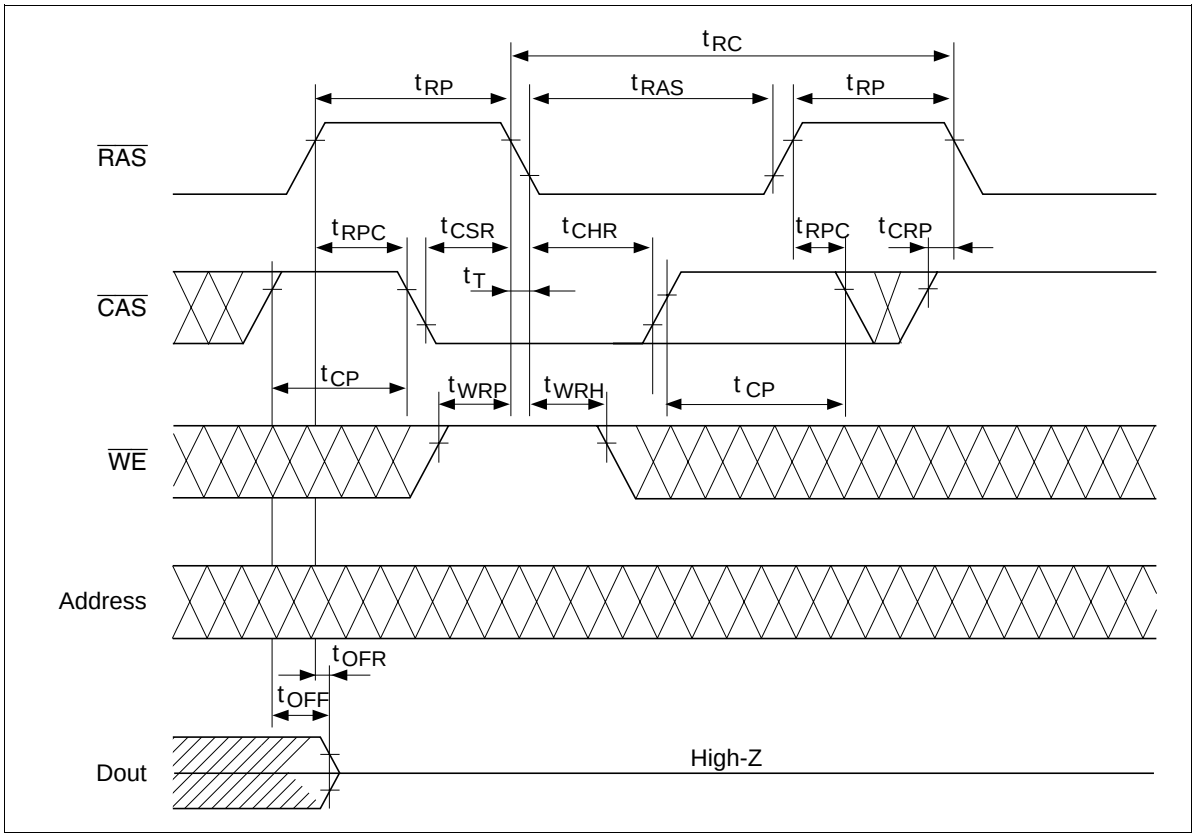
Read-Modify-Write Cycle*[18]



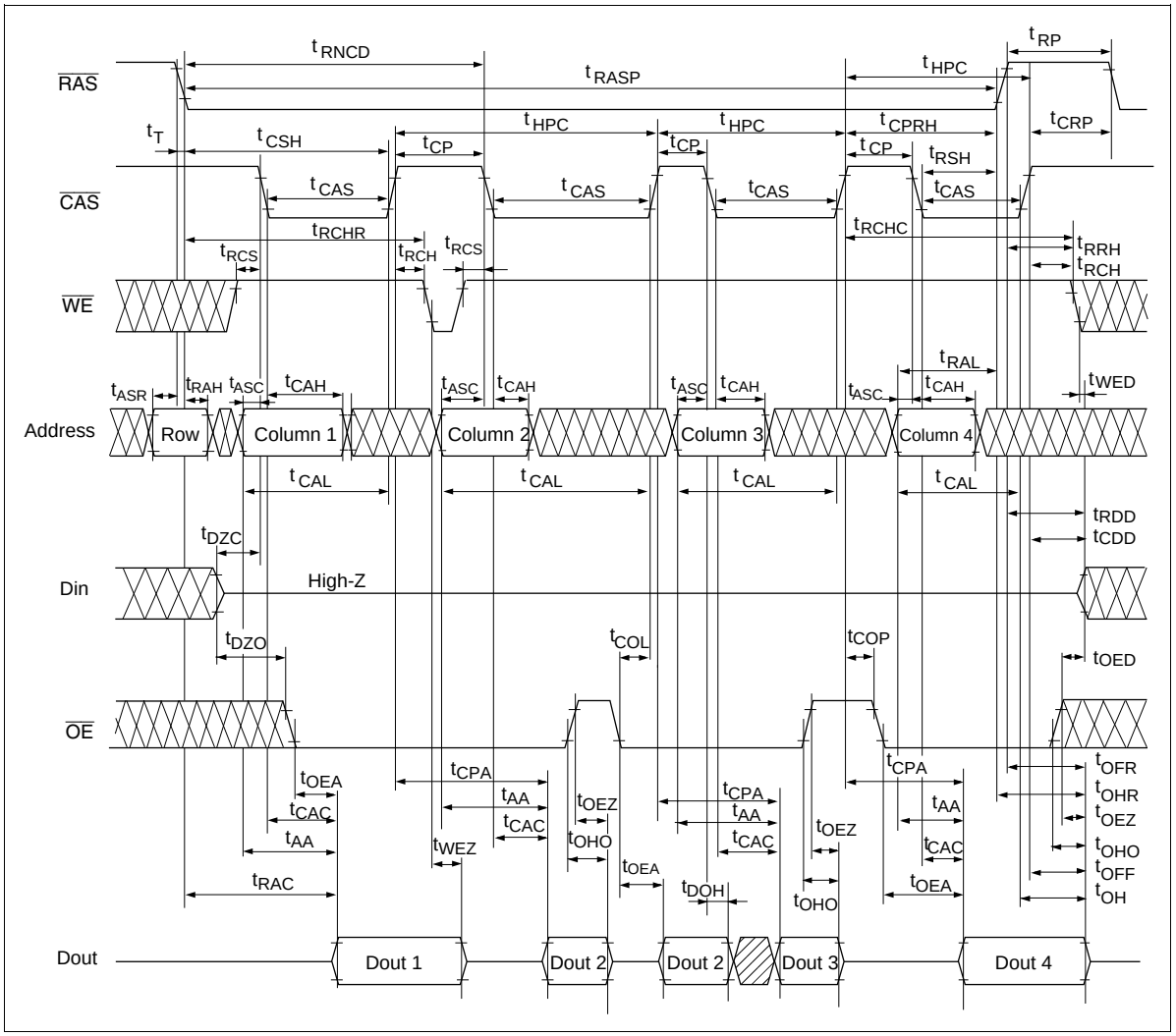
$\overline{\text{RAS}}$-Only Refresh Cycle



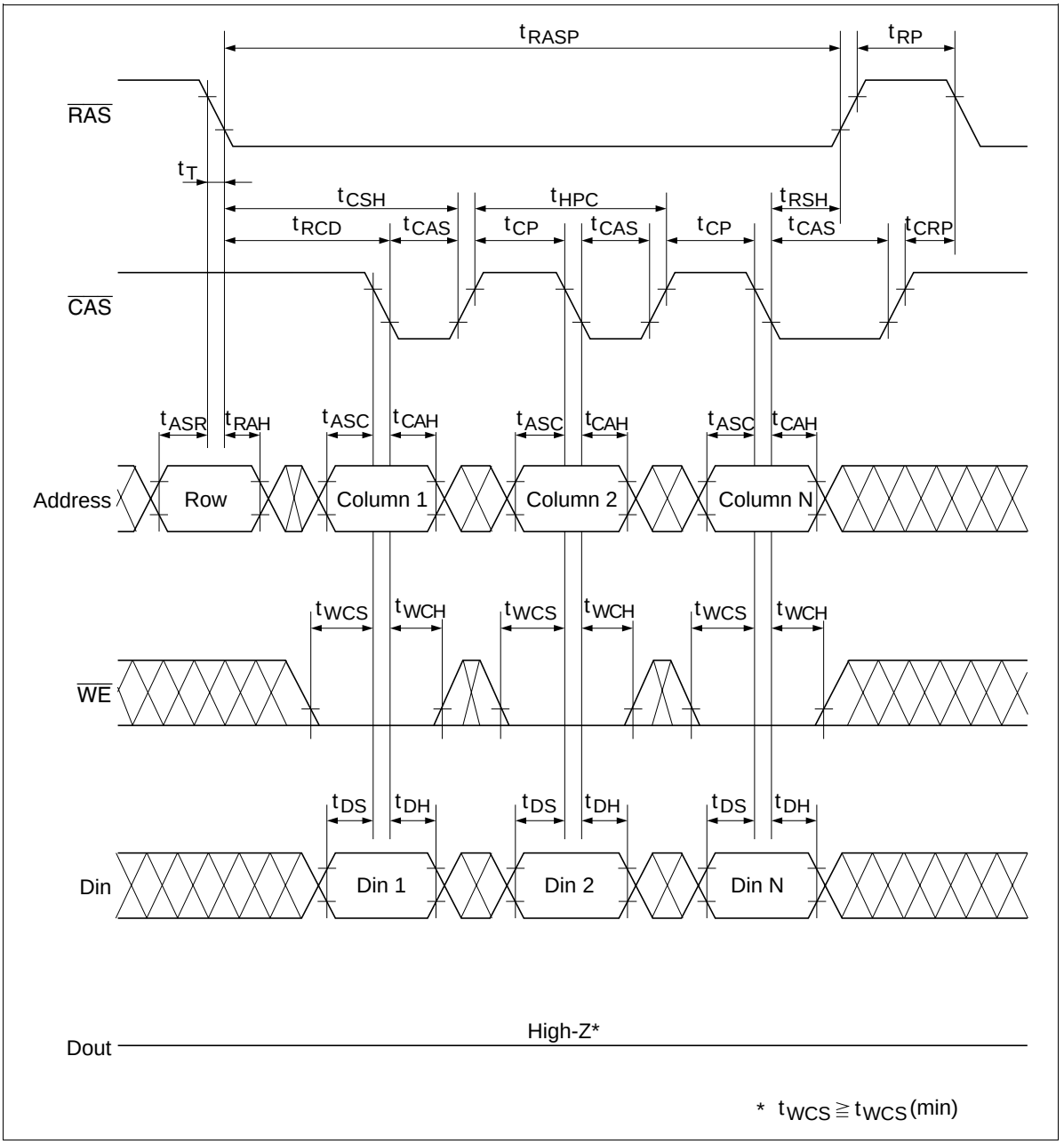
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



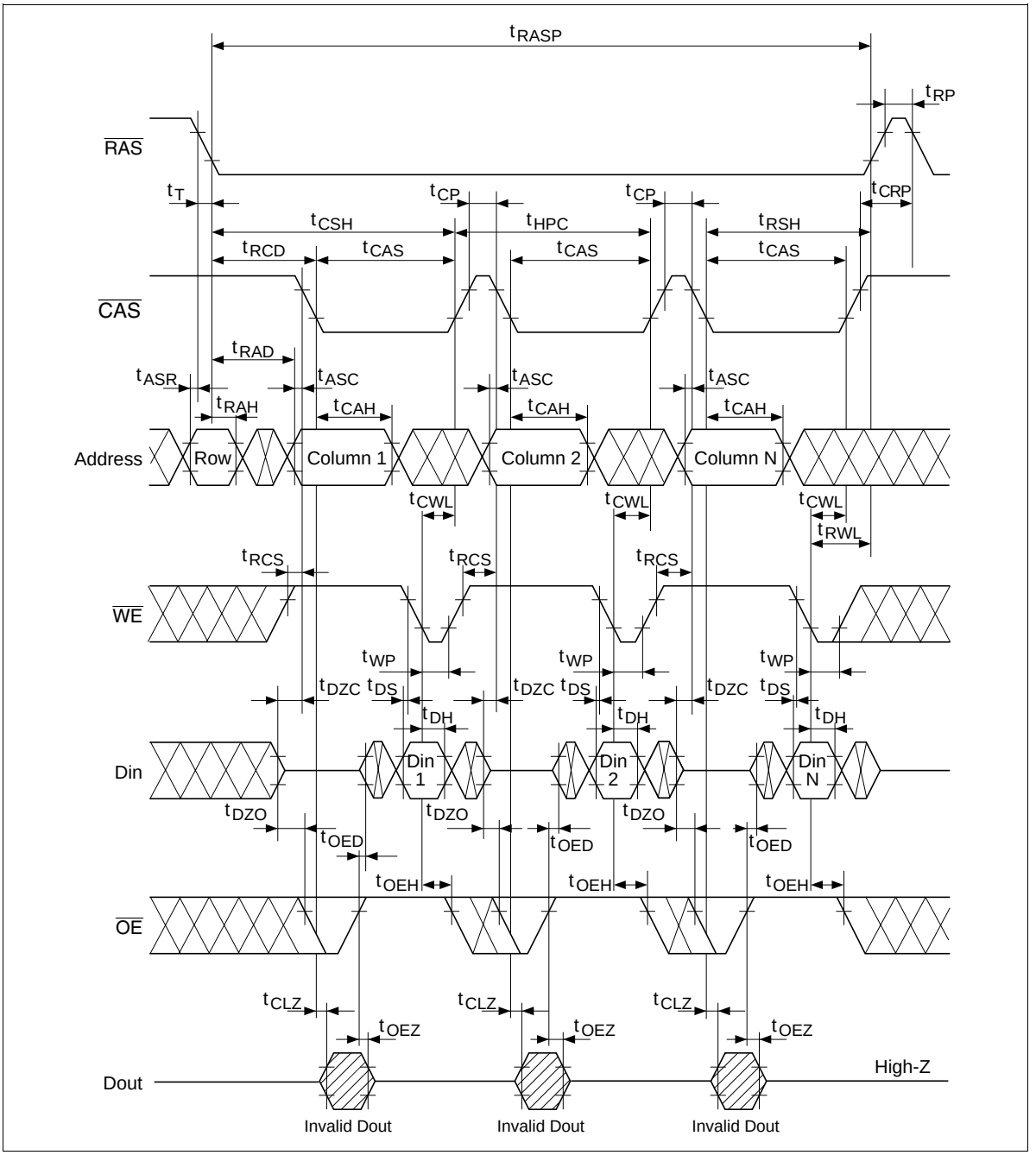
EDO Page Mode Read Cycle



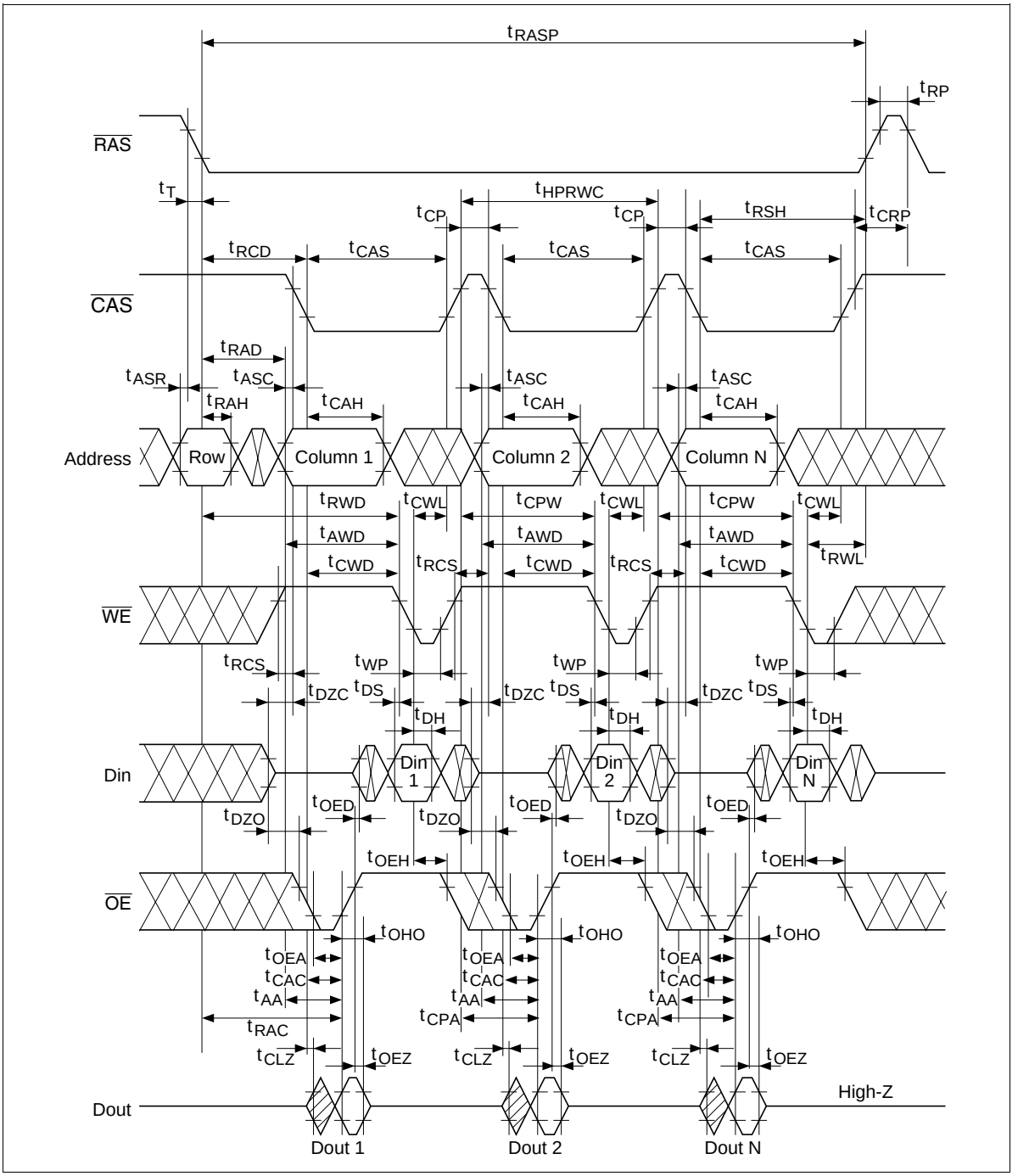
EDO Page Mode Early Write Cycle



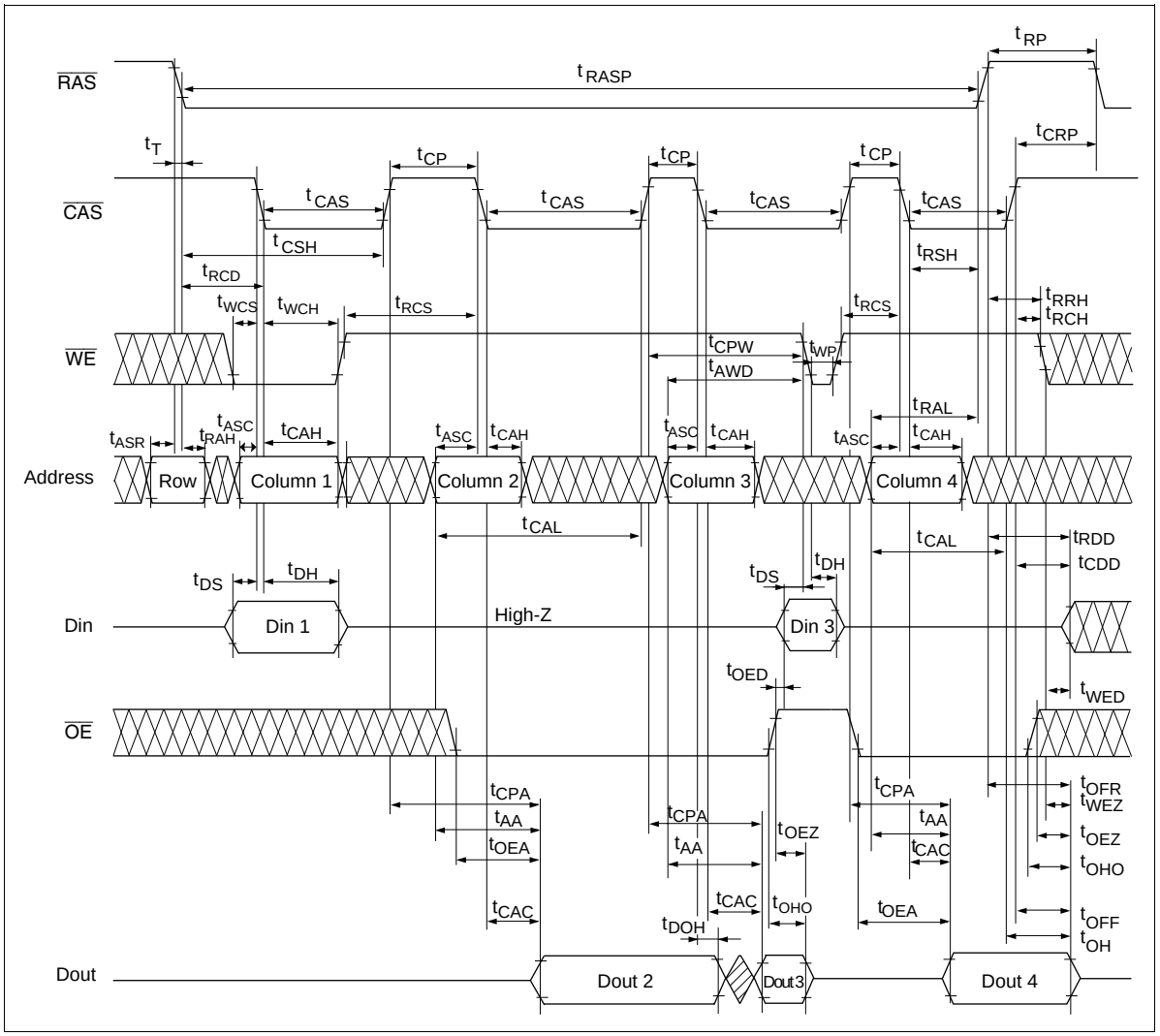
EDO Page Mode Delayed Write Cycle*[18]



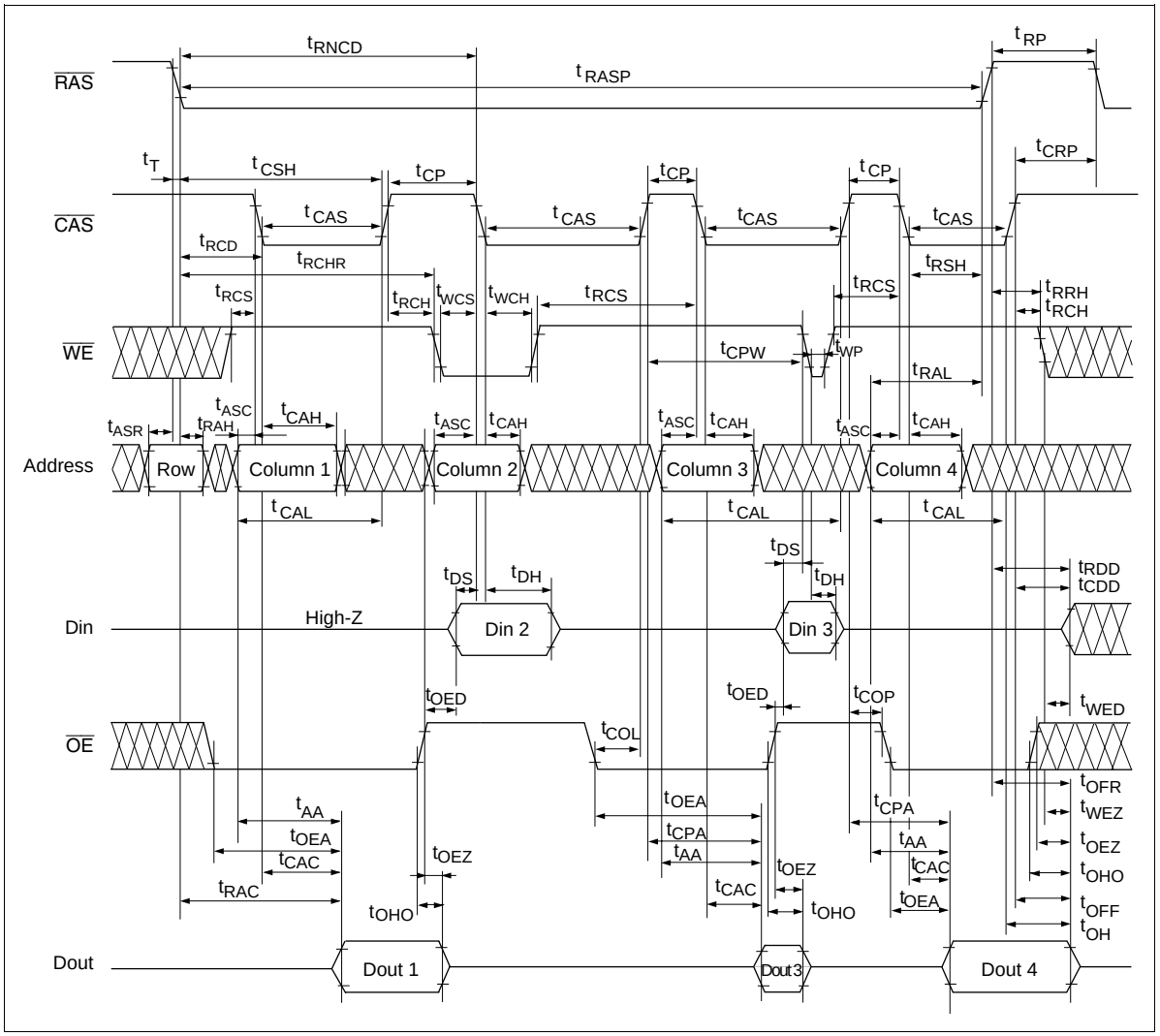
EDO Page Mode Read-Modify-Write Cycle*[18]



EDO Page Mode Mix Cycle (1)

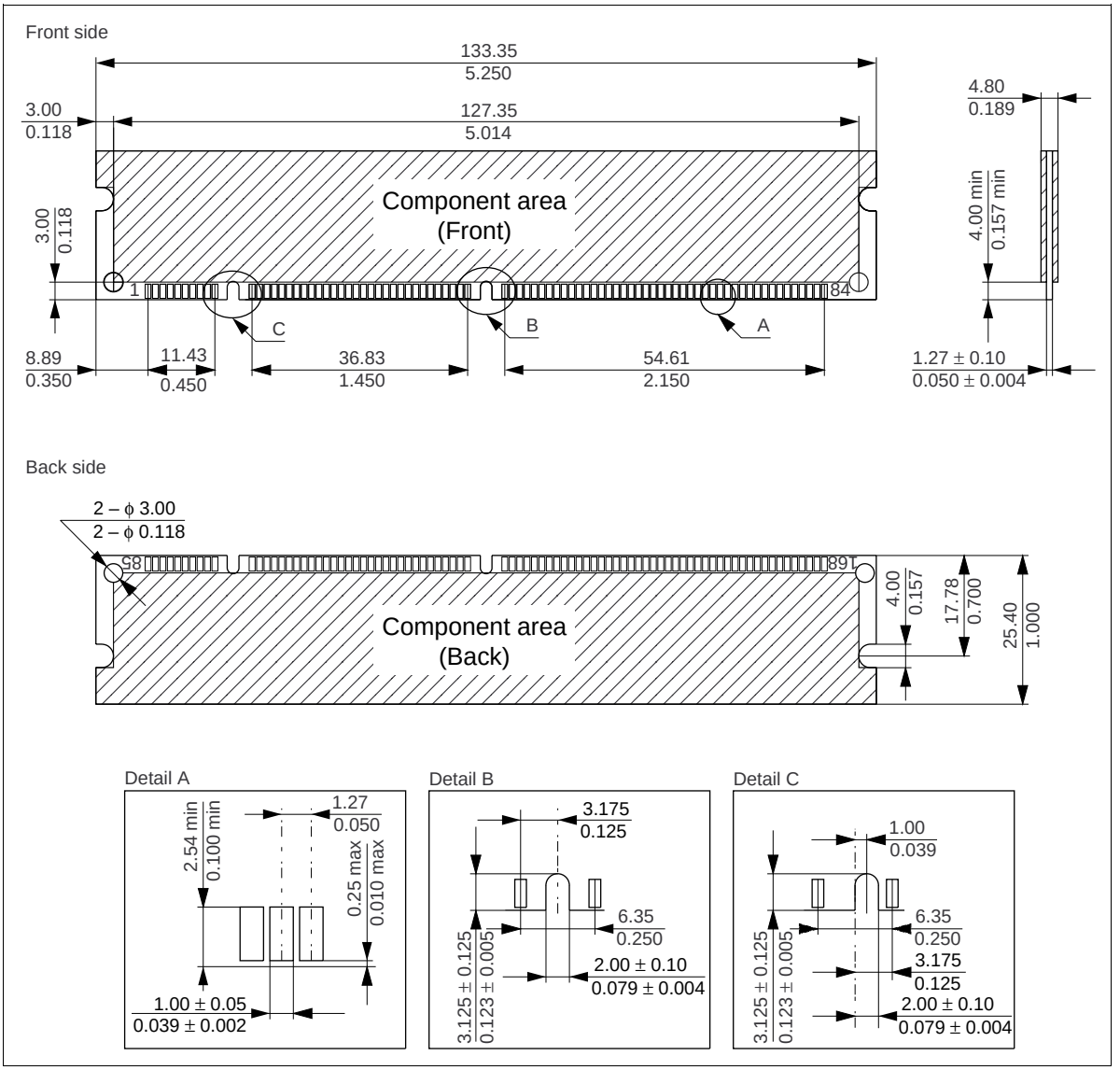


EDO Page Mode Mix Cycle (2)



Physical Outline

Unit: mm/inch



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1.0	Apr. 4, 1997	Initial issue		