
HB56SW464DB Series

4,194,304-word $\times$ 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-758A (Z)

Rev. 1.0

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Description

The HB56SW464DB is a $4\text{M} \times 64$ dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 16 pieces of 16-Mbit DRAM (HM51W16405) sealed in TCP package and 1 piece of serial EEPROM (24C02) for Presence Detect (PD). The HB56SW464DB offers Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56SW464DB is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56SW464DB makes high density mounting possible without surface mount technology. The HB56SW464DB provides common data inputs and outputs. Decoupling capacitors are mounted beside each TCP on the module board.

Features

- 144-pin Zig Zag Dual tabs socket type
 - Lead pitch: 0.80 mm
- Single 3.3 V (+0.3, -0.15 V) supply
- High speed
 - Access time: $t_{\text{RAC}} = 60/70 \text{ ns (max)}$
 $t_{\text{CAC}} = 15/18 \text{ ns (max)}$
- Low power dissipation
 - Active mode: 4.61/4.03 W (max)
 - Standby mode (TTL): 115.2 mW (max)
(CMOS): 57.6 mW (max)
(CMOS): 8.64 mW (max) (L-version)
- EDO mode capability
- Refresh period
 - 4096 refresh cycles: 64 ms
128 ms (L-version)
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Self refresh (only LS-version)

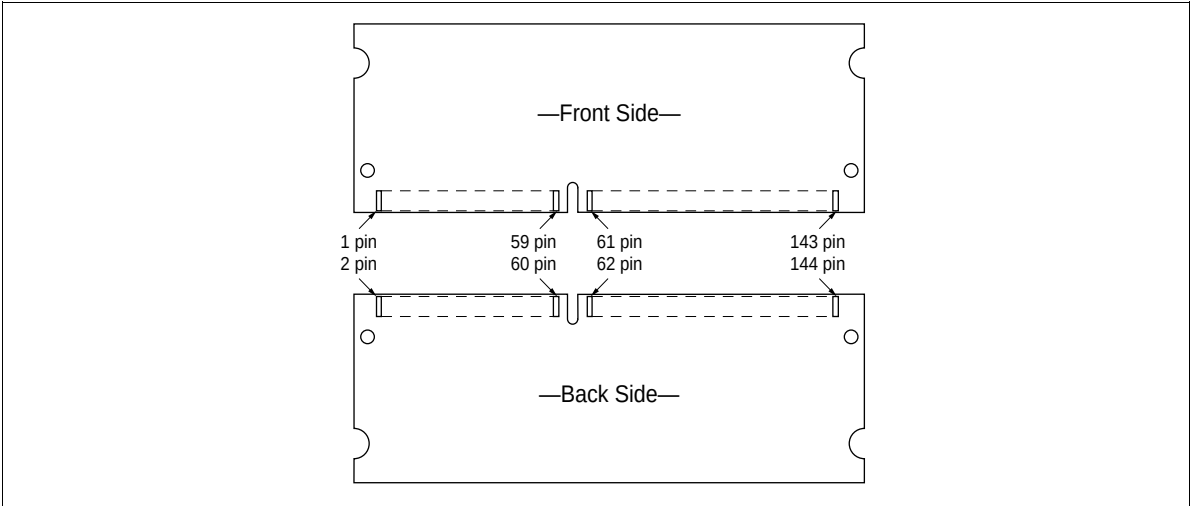
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- Recommend socket
Vendor Parts No.
AMP 316310-1

Ordering Information

Type No.	Access time	Package	Contact pad
HB56SW464DB-6	60 ns	Small Outline DIMM (144-pin)	Gold
HB56SW464DB-7	70 ns		
HB56SW464DB-6L	60 ns		
HB56SW464DB-7L	70 ns		
HB56SW464DB-6LS	60 ns		
HB56SW464DB-7LS	70 ns		

Pin Arrangement



Pin Arrangement

Front side

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	73	$\overline{\text{OE}}$	2	V _{SS}	74	NC
3	DQ0	75	V _{SS}	4	DQ32	76	V _{SS}
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	V _{CC}	10	DQ35	82	V _{CC}
11	V _{CC}	83	DQ16	12	V _{CC}	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51

Pin Arrangement (cont)

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
19	DQ7	91	V _{SS}	20	DQ39	92	V _{SS}
21	V _{SS}	93	DQ20	22	V _{SS}	94	DQ52
23	$\overline{\text{CE0}}$	95	DQ21	24	$\overline{\text{CE4}}$	96	DQ53
25	$\overline{\text{CE1}}$	97	DQ22	26	$\overline{\text{CE5}}$	98	DQ54
27	V _{CC}	99	DQ23	28	V _{CC}	100	DQ55
29	A0	101	V _{CC}	30	A3	102	V _{CC}
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	A11
35	V _{SS}	107	V _{SS}	36	V _{SS}	108	V _{SS}
37	DQ8	109	A9	38	DQ40	110	NC
39	DQ9	111	A10	40	DQ41	112	NC
41	DQ10	113	V _{CC}	42	DQ42	114	V _{CC}
43	DQ11	115	$\overline{\text{CE2}}$	44	DQ43	116	$\overline{\text{CE6}}$
45	V _{CC}	117	$\overline{\text{CE3}}$	46	V _{CC}	118	$\overline{\text{CE7}}$
47	DQ12	119	V _{SS}	48	DQ44	120	V _{SS}
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V _{SS}	127	DQ27	56	V _{SS}	128	DQ59
57	NC	129	V _{CC}	58	NC	130	V _{CC}
59	NC	131	DQ28	60	NC	132	DQ60
61	NC	133	DQ29	62	NC	134	DQ61
63	V _{CC}	135	DQ30	64	V _{CC}	136	DQ62
65	NC	137	DQ31	66	NC	138	DQ63
67	$\overline{\text{WE}}$	139	V _{SS}	68	NC	140	V _{SS}
69	$\overline{\text{RE0}}$	141	SDA	70	NC	142	SCL
71	NC	143	V _{CC}	72	NC	144	V _{CC}

Pin Description

Pin name	Function
A0 to A11	Address input — Row address : A0 to A11 — Column address : A0 to A9 — Refresh address : A0 to A11
DQ0 to DQ63	Data-in/data-out
$\overline{RE0}$	Row address strobe ($\overline{RAS}$)
$\overline{CE0}$ to $\overline{CE7}$	Column address strobe ($\overline{CAS}$)
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
SDA	Serial data for PD
SCL	Serial clock for PD
NC	No connection

Note: Serial-PD Data are not protected.

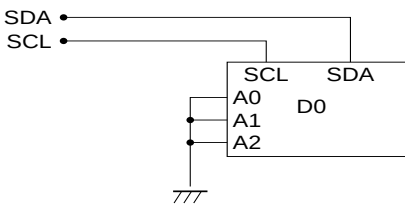
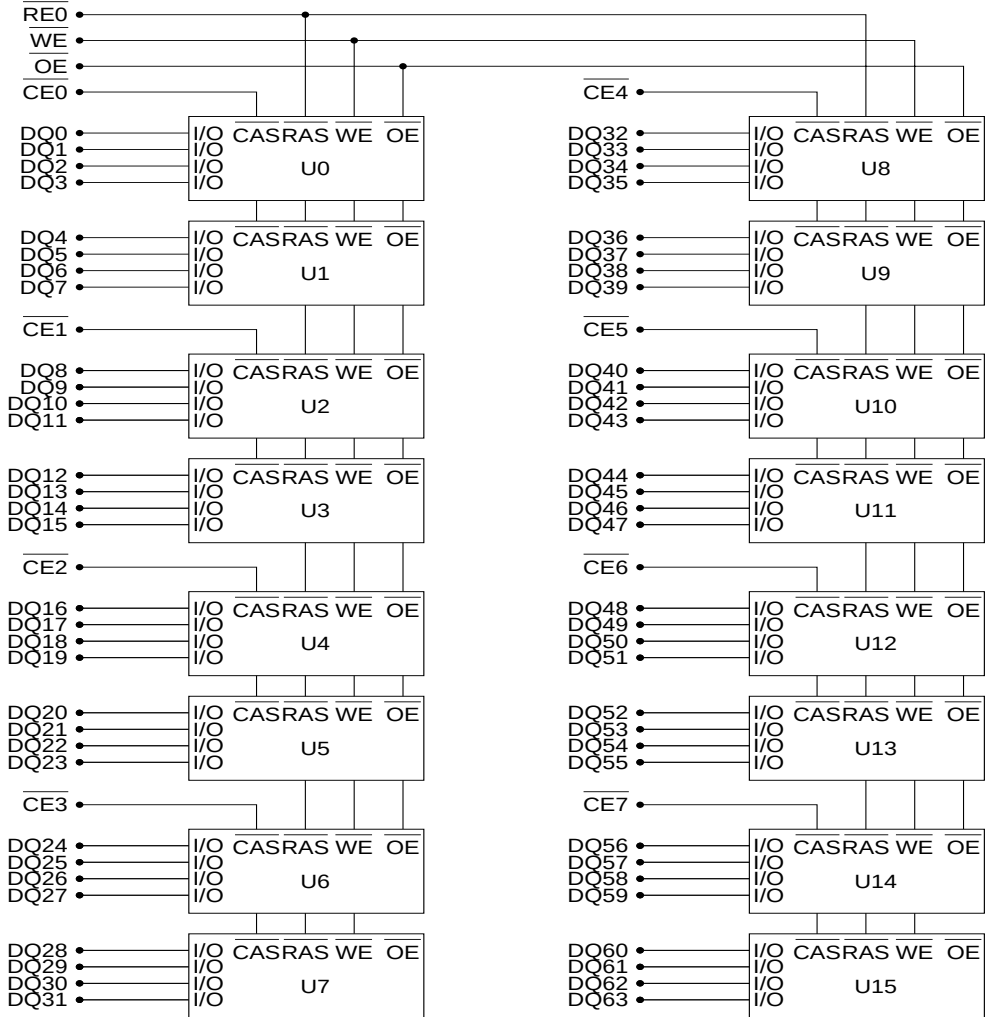
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Serial-PD Matrix*¹

Byte number	Function described		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comments
0	Number serial PD bytes		0	0	0	0	1	1	0	1	13
1	Serial memory		0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		0	0	0	0	0	0	1	0	EDO
3	Number of rows		0	0	0	0	1	1	0	0	12
4	Number of columns		0	0	0	0	1	0	1	0	10
5	Number of banks		0	0	0	0	0	0	0	1	1
6	Data width		0	1	0	0	0	0	0	0	64
7	Data width (continued)		0	0	0	0	0	0	0	0	0 (+)
8	Voltage interface		0	0	0	0	0	0	0	1	LVTTL (3.3 V)
9	$\overline{\text{RAS}}$ access time	60 ns	0	0	1	1	1	1	0	0	
		70 ns	0	1	0	0	0	1	1	0	
10	$\overline{\text{CAS}}$ access time	15 ns	0	0	0	0	1	1	1	1	
		18 ns	0	0	0	1	0	0	1	0	
11	Error detection/correction		0	0	0	0	0	0	0	0	None
12	Refresh period		0	0	0	0	0	0	0	0	Normal (15.625 μs)
	Refresh period (L-version)		0	0	0	0	0	0	1	1	Extended (31.3 μs)
	Refresh period (LS-version)		1	0	0	0	0	0	1	1	Self refresh Extended (31.3 μs)

Note: 1. 1: High Level (Serial data)
0: Low Level (Serial data)

Block Diagram



A0 to A11 ●————— U0 to U15

V_{CC} ●————— U0 to U15, D0

V_{SS} ●————— U0 to U15, D0

●——— C0 to C7

* U0 to U15	: HM51W16405
D0	: 24C02
C0 to C7	: Chip capacitor

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	16	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.15	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	−0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

DC Characteristics ($T_a = 0 \text{ to } +70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} + 0.3, -0.15 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I_{CC1}	—	1280	—	1120	mA	$t_{RC} = \text{min}$	1, 2
Standby current	I_{CC2}	—	32	—	32	mA	TTL interface $\overline{RAS}, \overline{CAS} = V_{IH}$ Dout = High-Z	
		—	16	—	16	mA	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	2.4	—	2.4	mA	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
$\overline{RAS}$ -only refresh current	I_{CC3}	—	1280	—	1120	mA	$t_{RC} = \text{min}$	2
Standby current	I_{CC5}	—	80	—	80	mA	$\overline{RAS} = V_{IH}, \overline{CAS} = V_{IL}$ Dout = enable	1
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I_{CC6}	—	1280	—	1120	mA	$t_{RC} = \text{min}$	
EDO page mode current	I_{CC7}	—	1120	—	1040	mA	$t_{HPC} = \text{min}$	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	6.4	—	6.4	mA	CMOS interface Dout = High-Z CBRrefresh: $t_{RC} = 31.3 \mu\text{s}$ $t_{RAS} \leq 0.3 \mu\text{s}$	4
Self refresh mode current (LS-version)	I_{CC11}	—	4	—	4	mA	CMOS interface $\overline{RAS}, \overline{CAS} \leq 0.2 \text{ V}$ Dout = High-Z	
Input leakage current	I_{LI}	-10	10	-10	10	μA	$0 \text{ V} \leq V_{in} \leq 4.6 \text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	μA	$0 \text{ V} \leq V_{out} \leq 4.6 \text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.
4. $V_{IH} \geq V_{CC} - 0.2 \text{ V}$, $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$

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Capacitance (Ta = 25°C, V_{CC} = 3.3 V +0.3, -0.15 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	90	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I2}	—	120	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C _{I3}	—	30	pF	1, 2
I/O capacitance (DQ)	C _{I/O}	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}}$ = V_{IH} to disable Dout.

AC Characteristics ($T_a = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} + 0.3, -0.15 \text{ V}$, $V_{SS} = 0 \text{ V}$) *¹, *², *¹⁸, *¹⁹**Test Conditions**

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	45	14	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	12	30	12	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	13	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7
Refresh period (4,096 cycles)	t_{REF}	—	64	—	64	ms	
Refresh period (4,096 cycles) (L-version)	t_{REF}	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	22
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13, 22
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	ns	22
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	ns	
$\overline{\text{RAS}}$ next $\overline{\text{CAS}}$ delay time	t_{RNCD}	60	—	70	—	ns	

Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	10	—	13	—	ns	15

Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	49	—	57	—	ns	14
$\overline{OE}$ hold time $\overline{WE}$	t_{OEh}	15	—	18	—	ns	

Refresh Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	

EDO Page Mode Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode cycle time	t _{HPC}	25	—	30	—	ns	20
EDO page mode RAS pulse width	t _{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	35	—	40	ns	9, 17
RAS hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	35	—	40	—	ns	
Output data hole time from $\overline{\text{CAS}}$ low	t _{DOH}	3	—	3	—	ns	9, 17
$\overline{\text{CAS}}$ hold time referred $\overline{\text{OE}}$	t _{COL}	10	—	13	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ setup time	t _{COP}	5	—	5	—	ns	
Read command hold time from $\overline{\text{CAS}}$ precharge	t _{RCHC}	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	t _{HPRWC}	68	—	79	—	ns	
$\overline{\text{WE}}$ delay time from $\overline{\text{CAS}}$ precharge	t _{CPW}	54	—	62	—	ns	14

Self Refresh Mode (only LS-version)

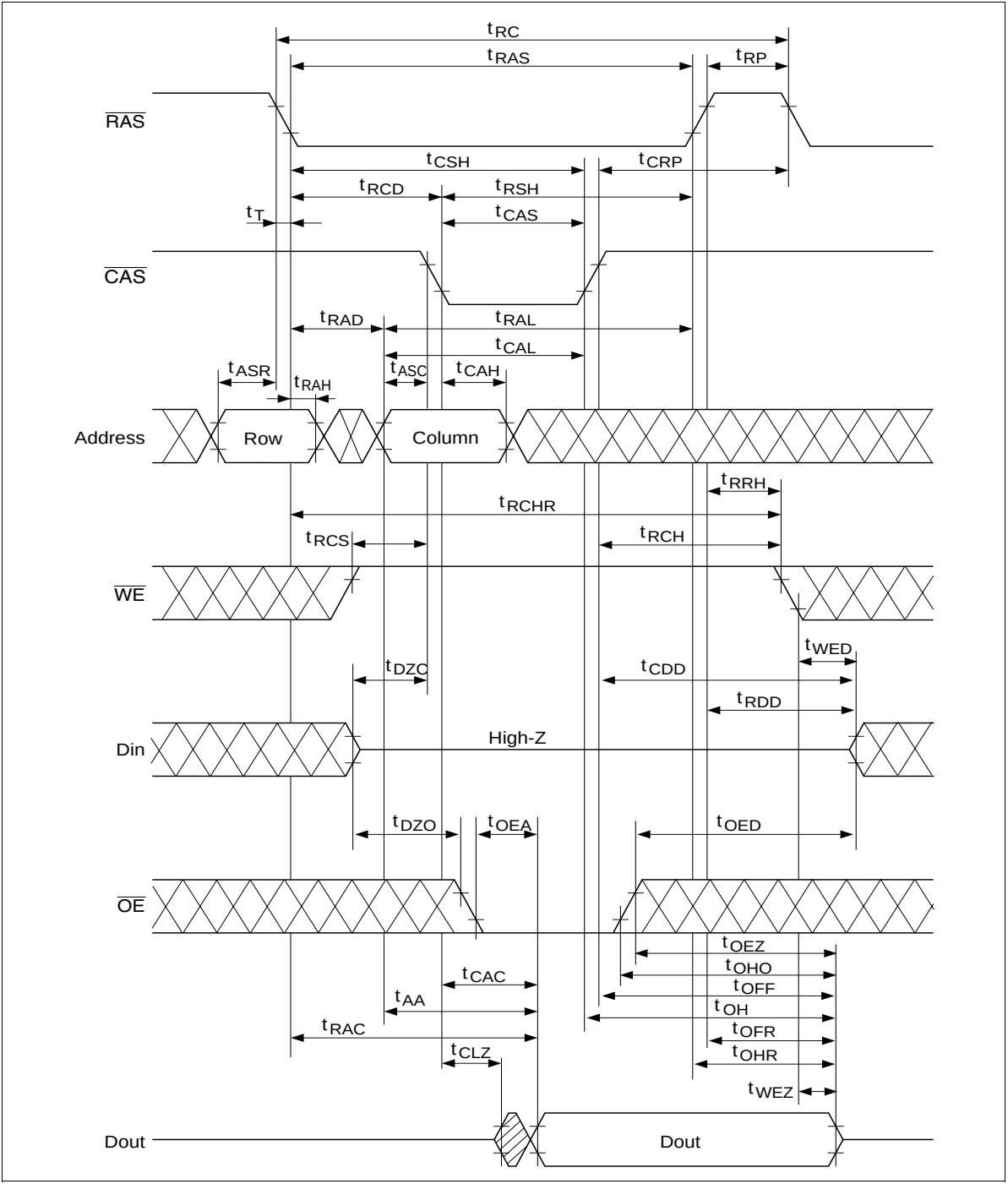
Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
RAS pulse width (Self refresh)	t _{RASS}	100	—	100	—	μs	
RAS precharge time (Self refresh)	t _{RPS}	110	—	130	—	ns	
$\overline{\text{CAS}}$ hold time (Self refresh)	t _{CHS}	−50	—	−50	—	ns	

- Notes:
1. AC measurements assume $t_T = 2 \text{ ns}$.
 2. An initial pause of $200 \mu\text{s}$ is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
 3. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only; if $t_{\text{RCD}} \geq t_{\text{RAD}}(\text{max}) + t_{\text{AA}}(\text{max}) - t_{\text{CAC}}(\text{max})$, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.
 8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$.
 11. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$.
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} , and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ or $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device. After $\overline{\text{RAS}}$ is reset, if $t_{\text{OEH}} \geq t_{\text{CWL}}$, the DQ pin will remain open circuit (high impedance); $t_{\text{OEH}} < t_{\text{OEH}}$, invalid data will be out at each DQ.
 19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 20. $t_{\text{HPC}}(\text{min})$ can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2t_T$) becomes greater than the specified $t_{\text{HPC}}(\text{min})$ value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
 21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}} / V_{\text{SS}}$ line noise, which causes to degrade $V_{\text{IH}} \text{ min.} / V_{\text{IL}} \text{ max level.}$
 22. Data output turns off and becomes high impedance from later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .

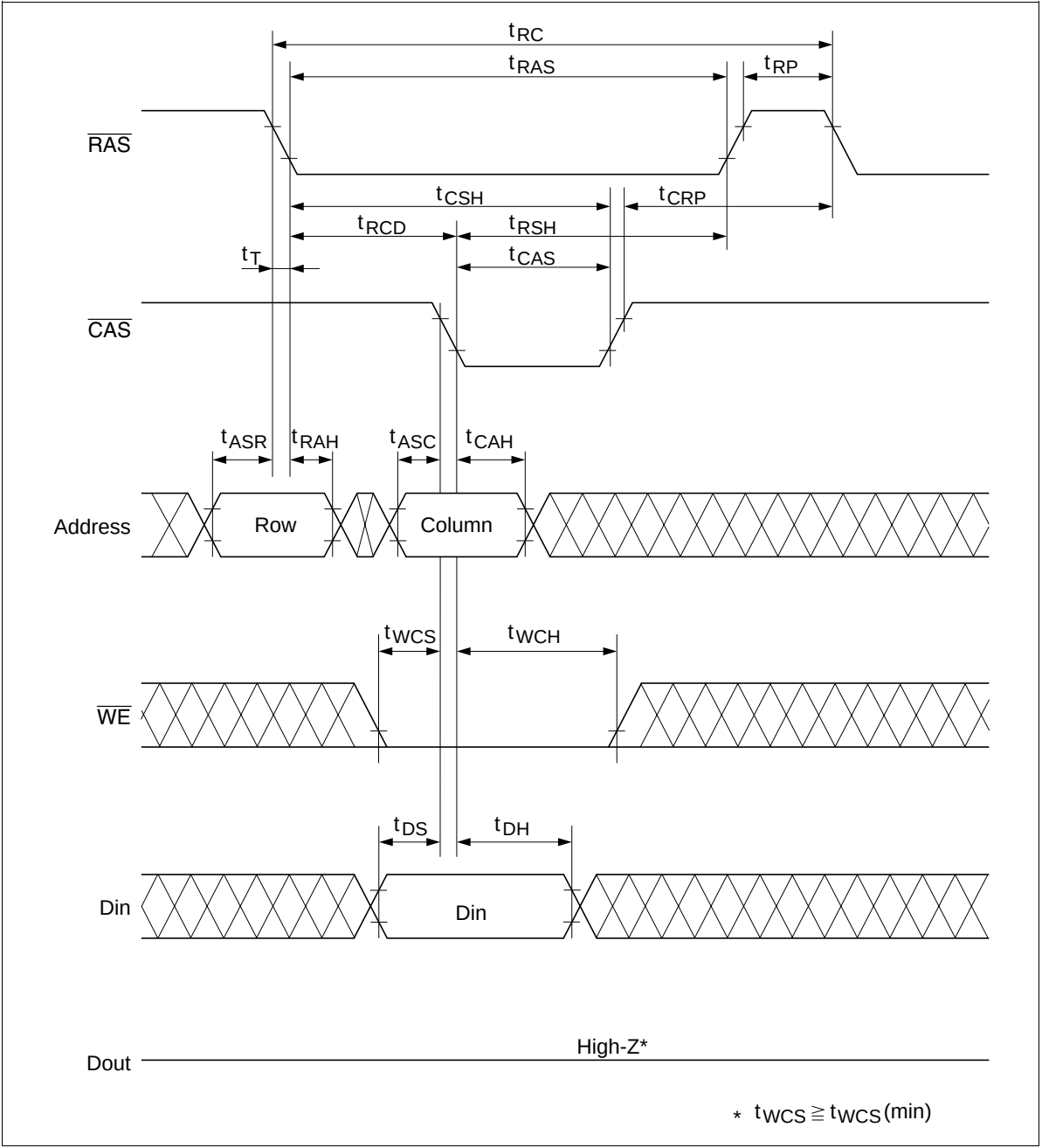
23. Please do not use t_{RASS} timing, $10\ \mu\text{s} \leq t_{\text{RASS}} \leq 100\ \mu\text{s}$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{\text{RASS}} \geq 100\ \mu\text{s}$, then $\overline{\text{RAS}}$ precharge time should use t_{RPS} instead of t_{RP} .
24. If you use distributed CBR refresh mode with $15.6\ \mu\text{s}$ interval in normal read/write cycle, CBR refresh should be executed within $15.6\ \mu\text{s}$ immediately after exiting from and before entering into self refresh mode.
25. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 of distributed CBR refresh with $15.6\ \mu\text{s}$ interval should be executed within 64 ms immediately after exiting from and before entering into the self refresh mode.
26. XXX: H or L (H: $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$, L: $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$)
/////: Invalid Dout
- When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Timing Waveforms*26

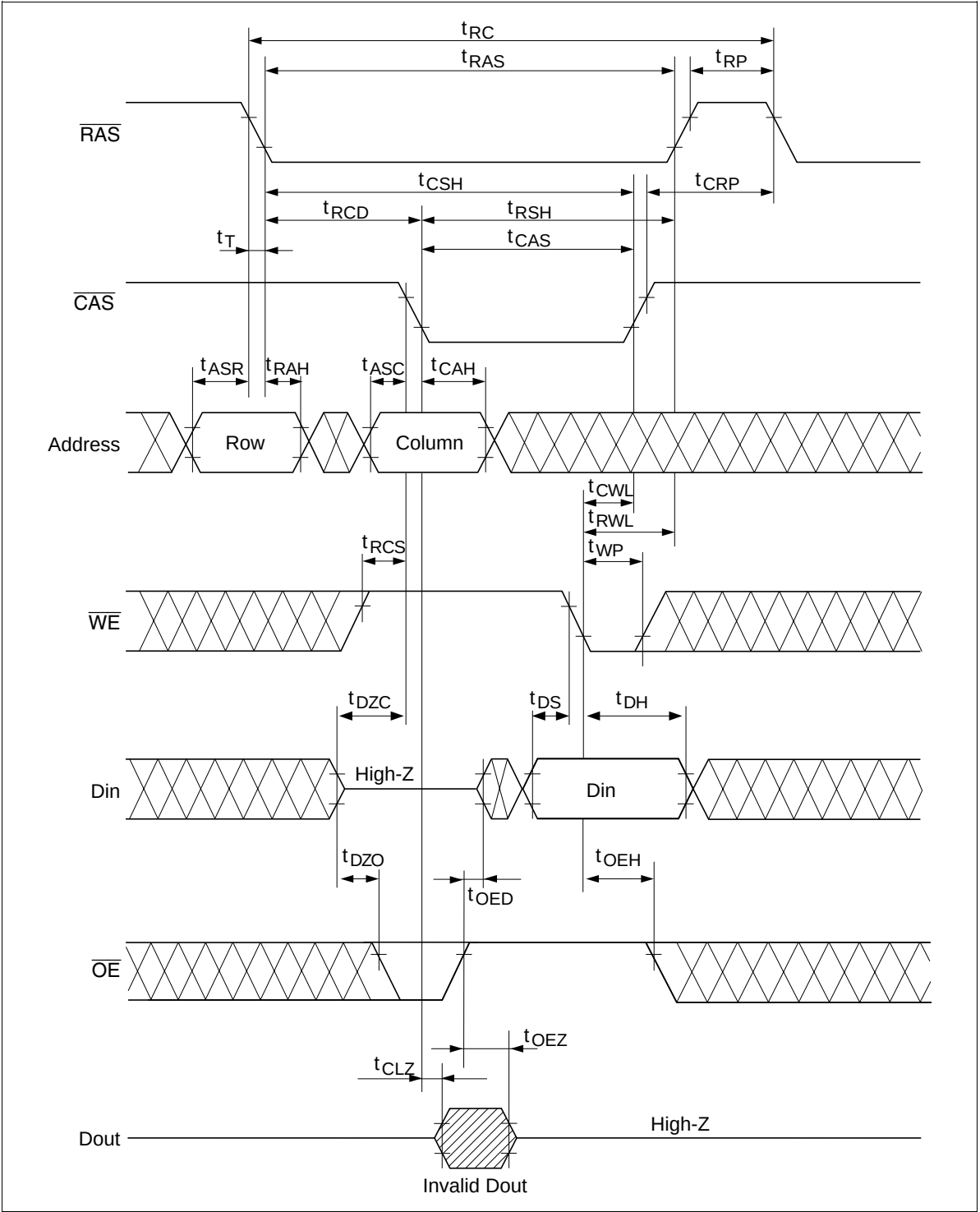
Read Cycle



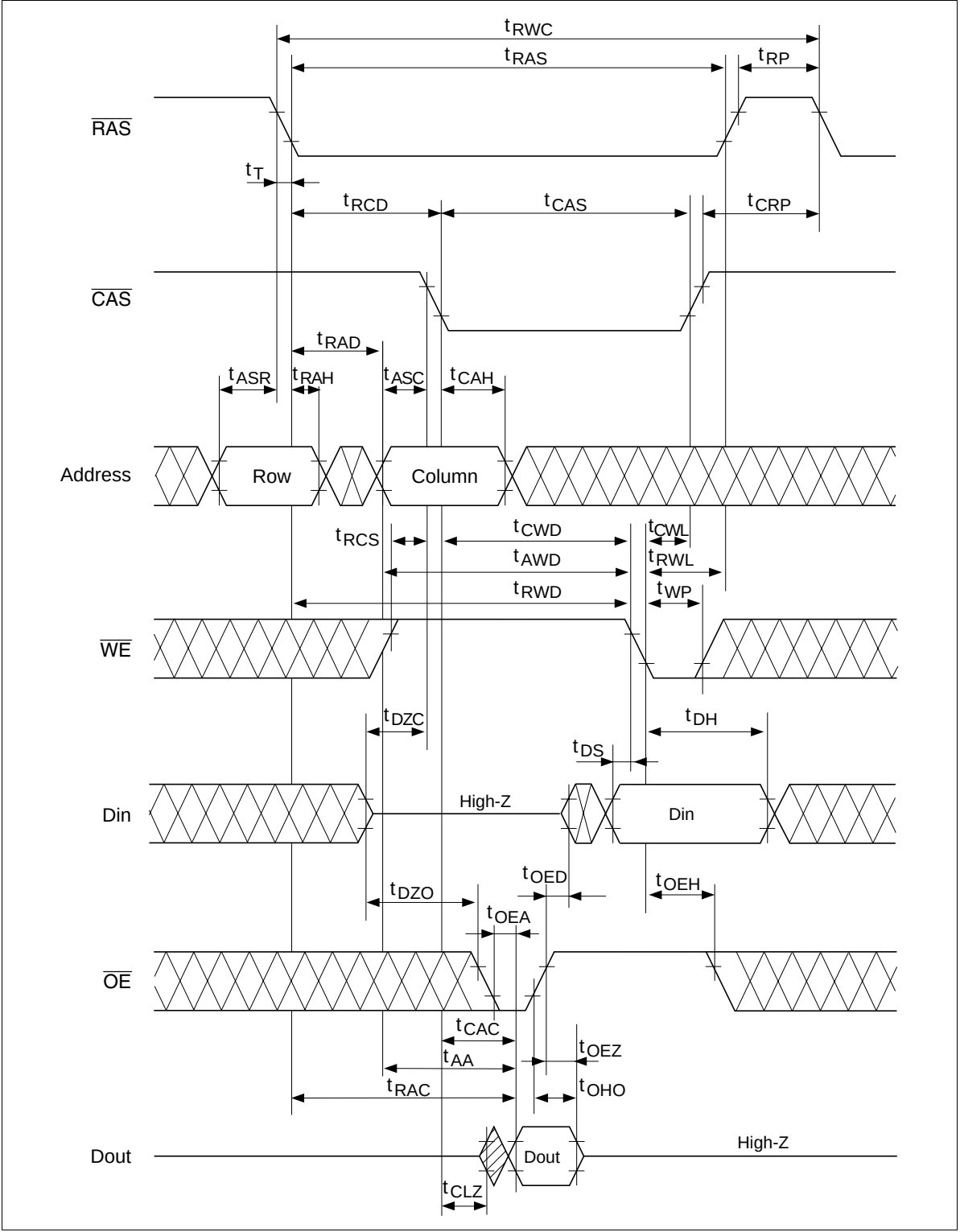
Early Write Cycle



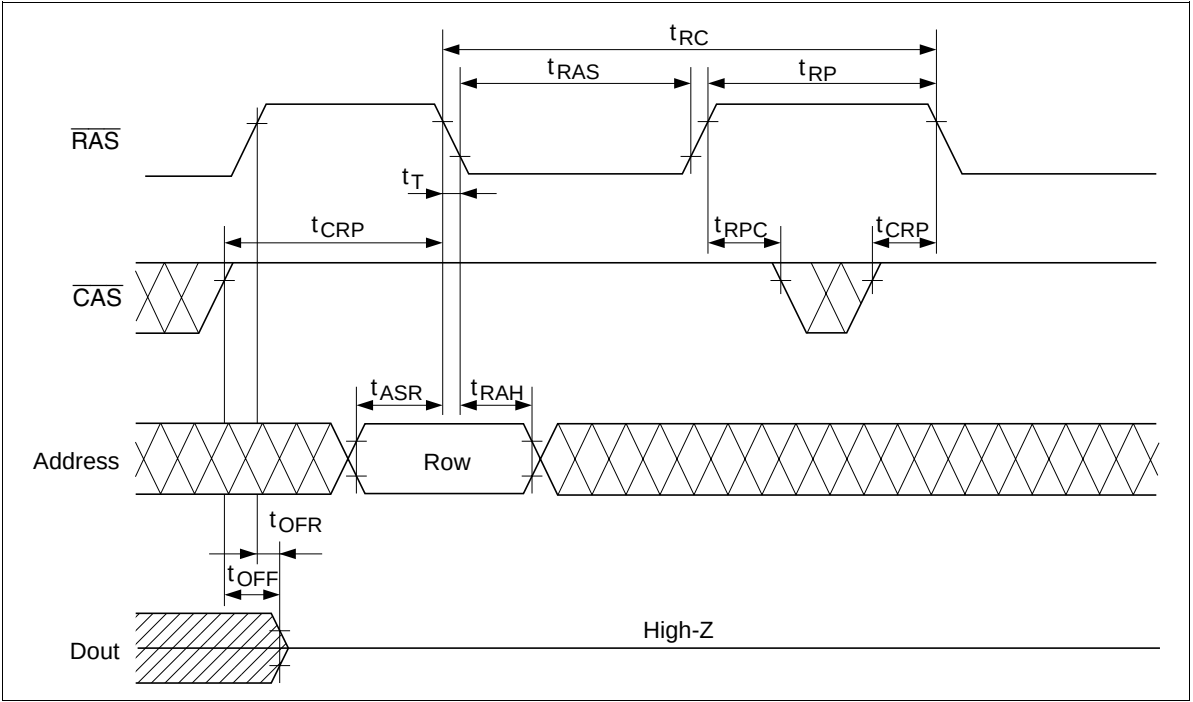
Delayed Write Cycle*18

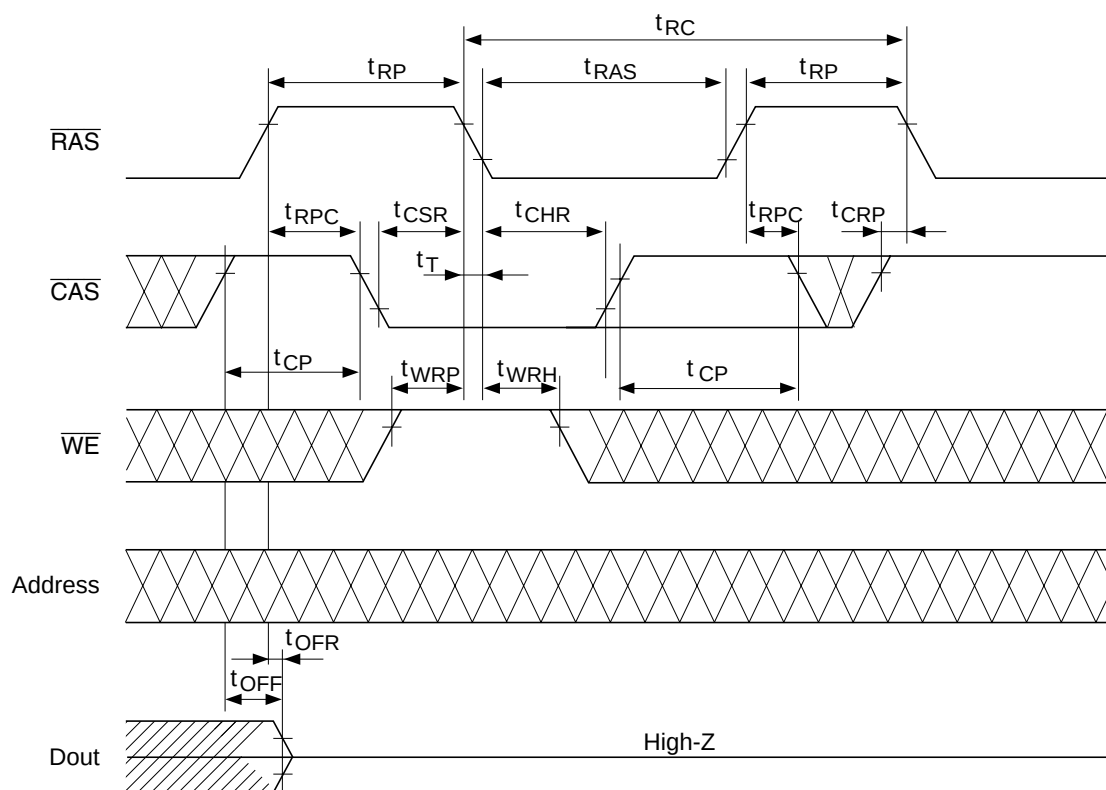


Read-Modify-Write Cycle*18

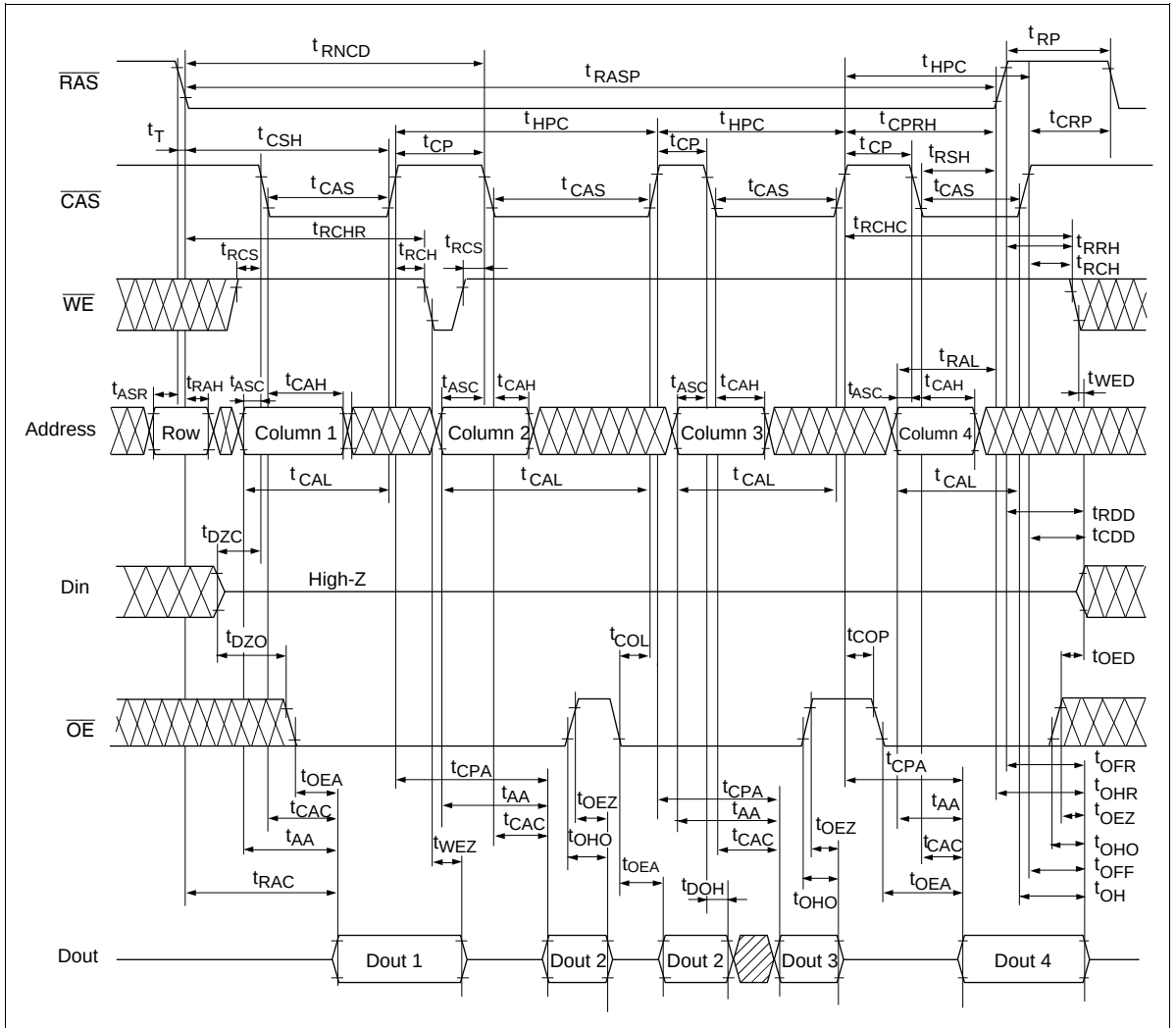


RAS-Only Refresh Cycle

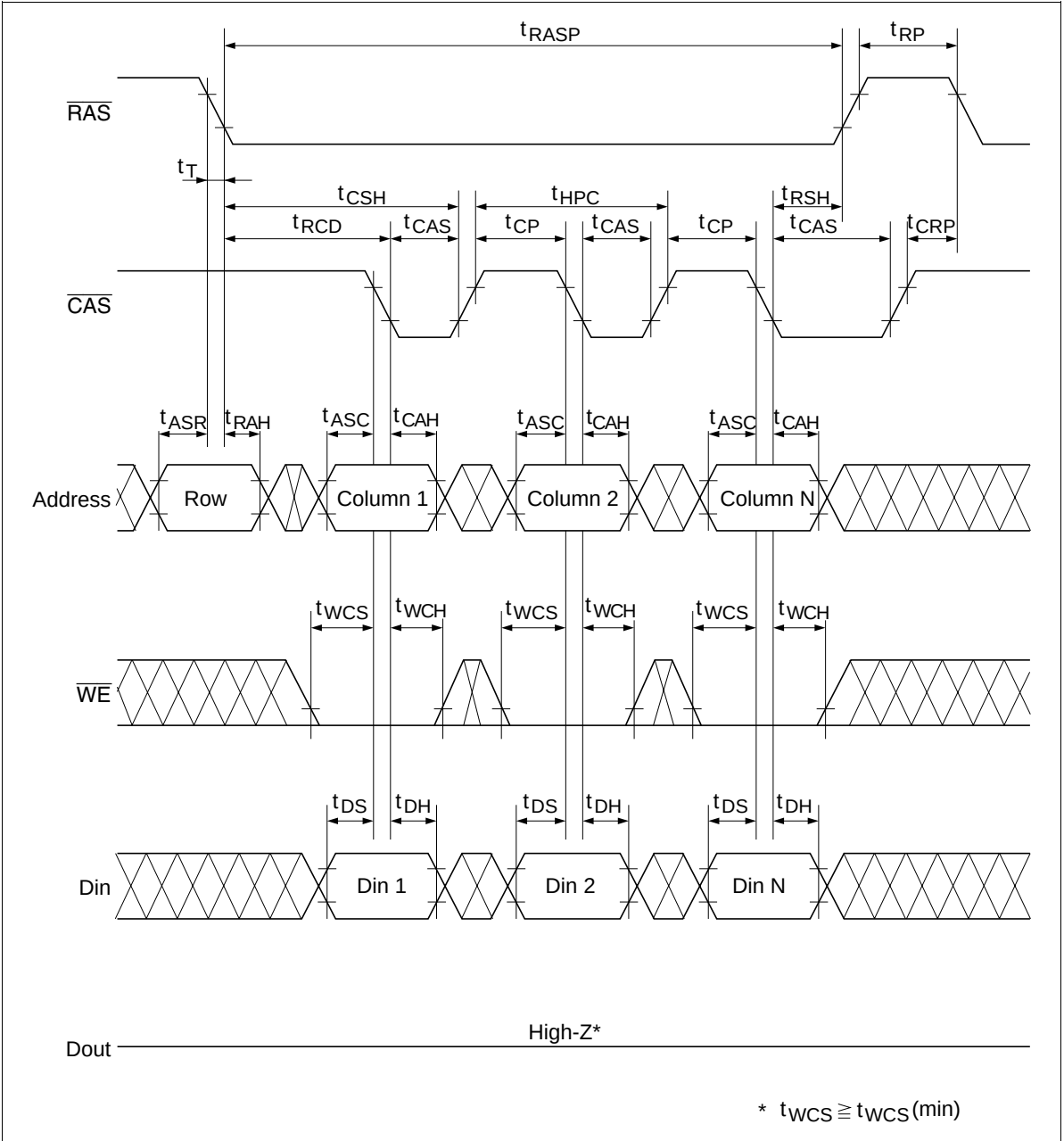




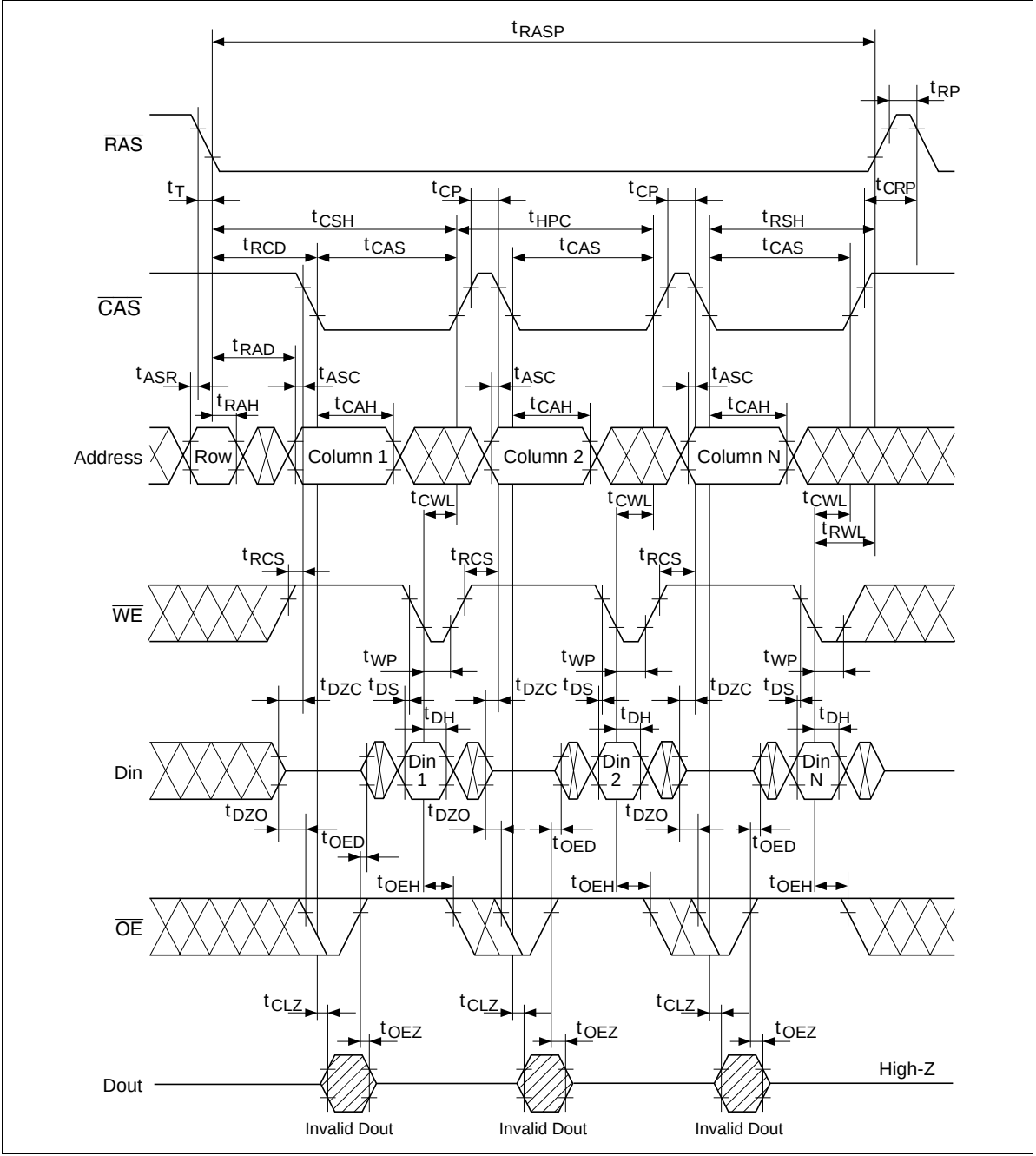
EDO Page Mode Read Cycle



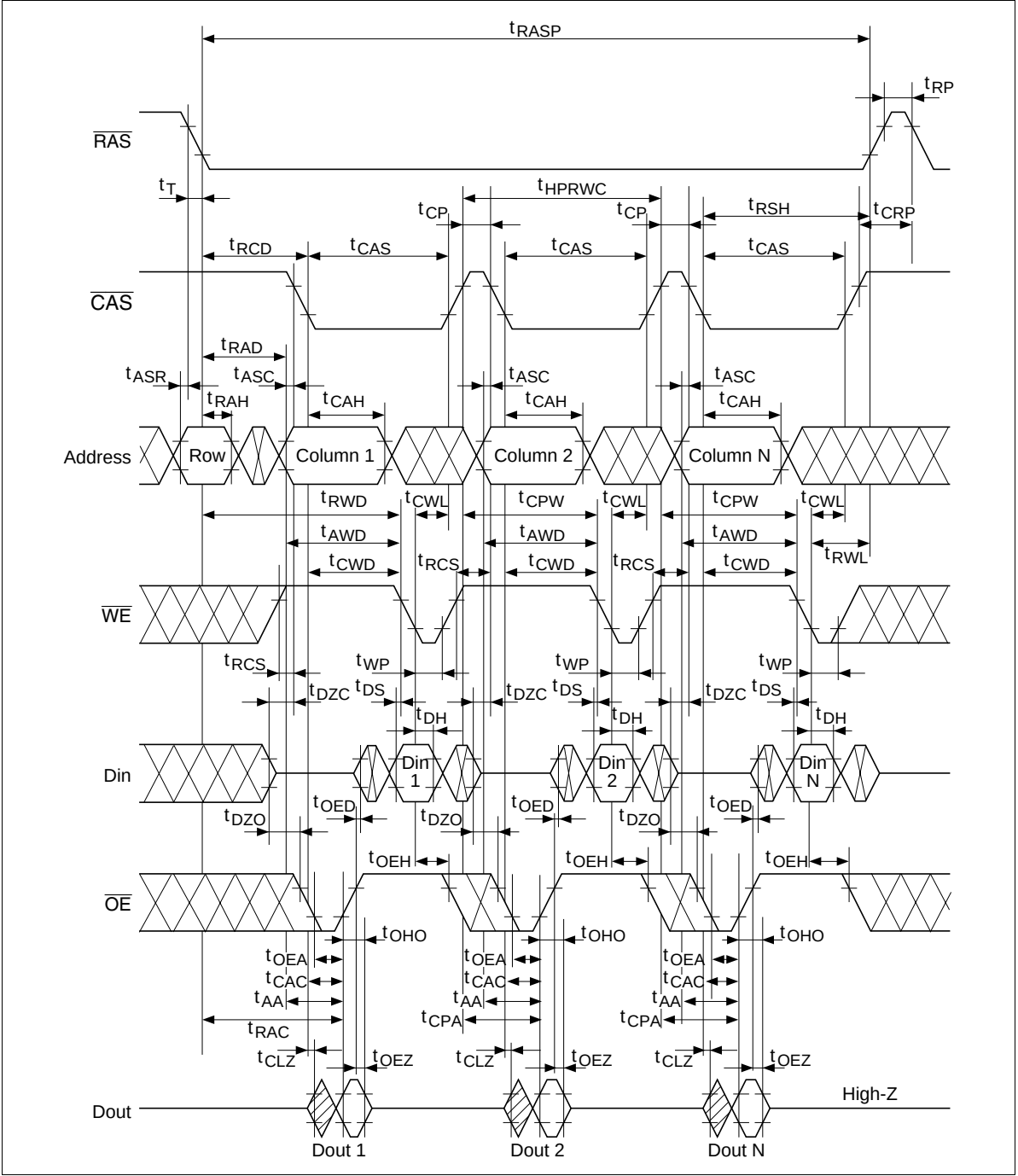
EDO Page Mode Early Write Cycle



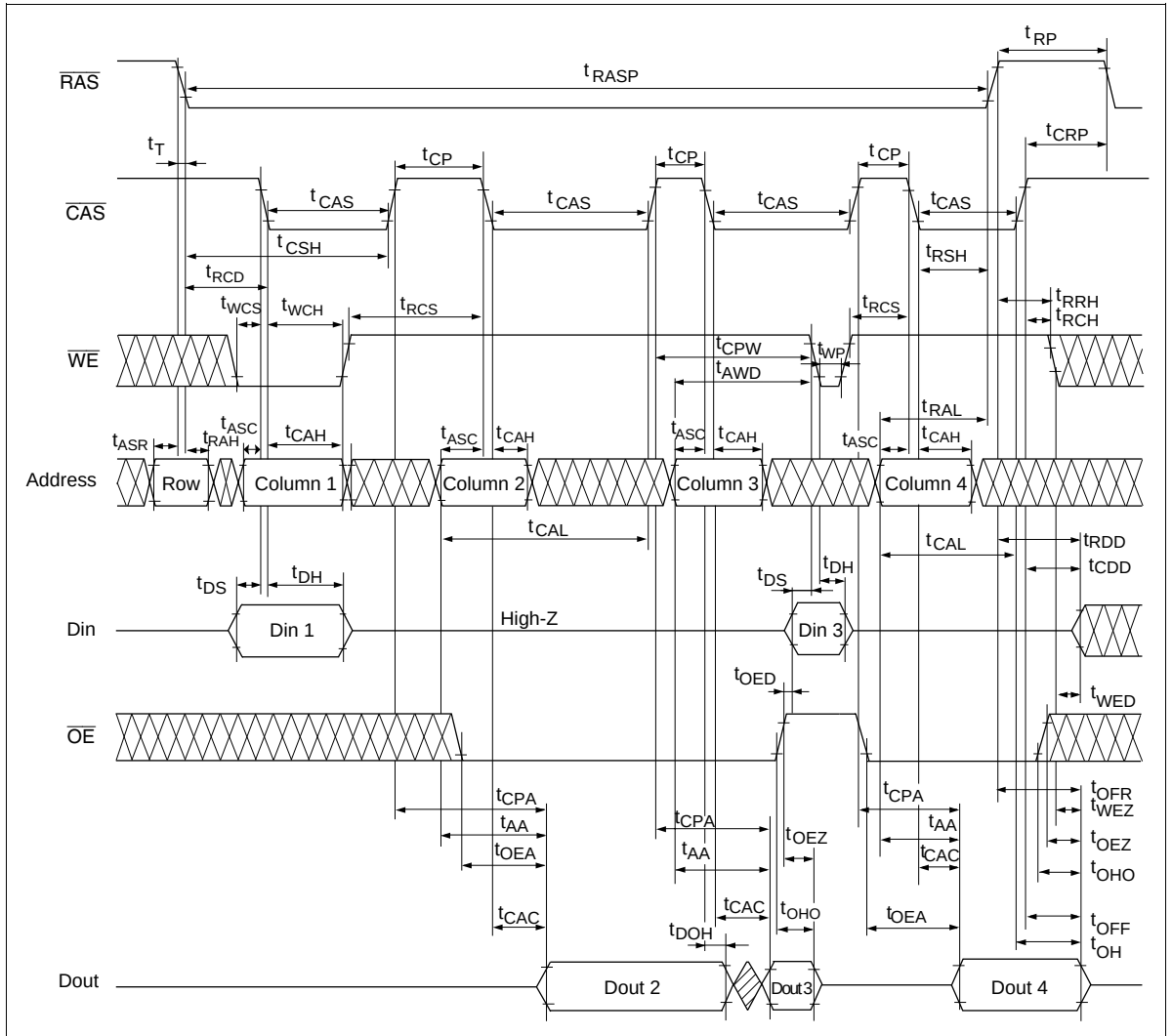
EDO Page Mode Delayed Write Cycle*18



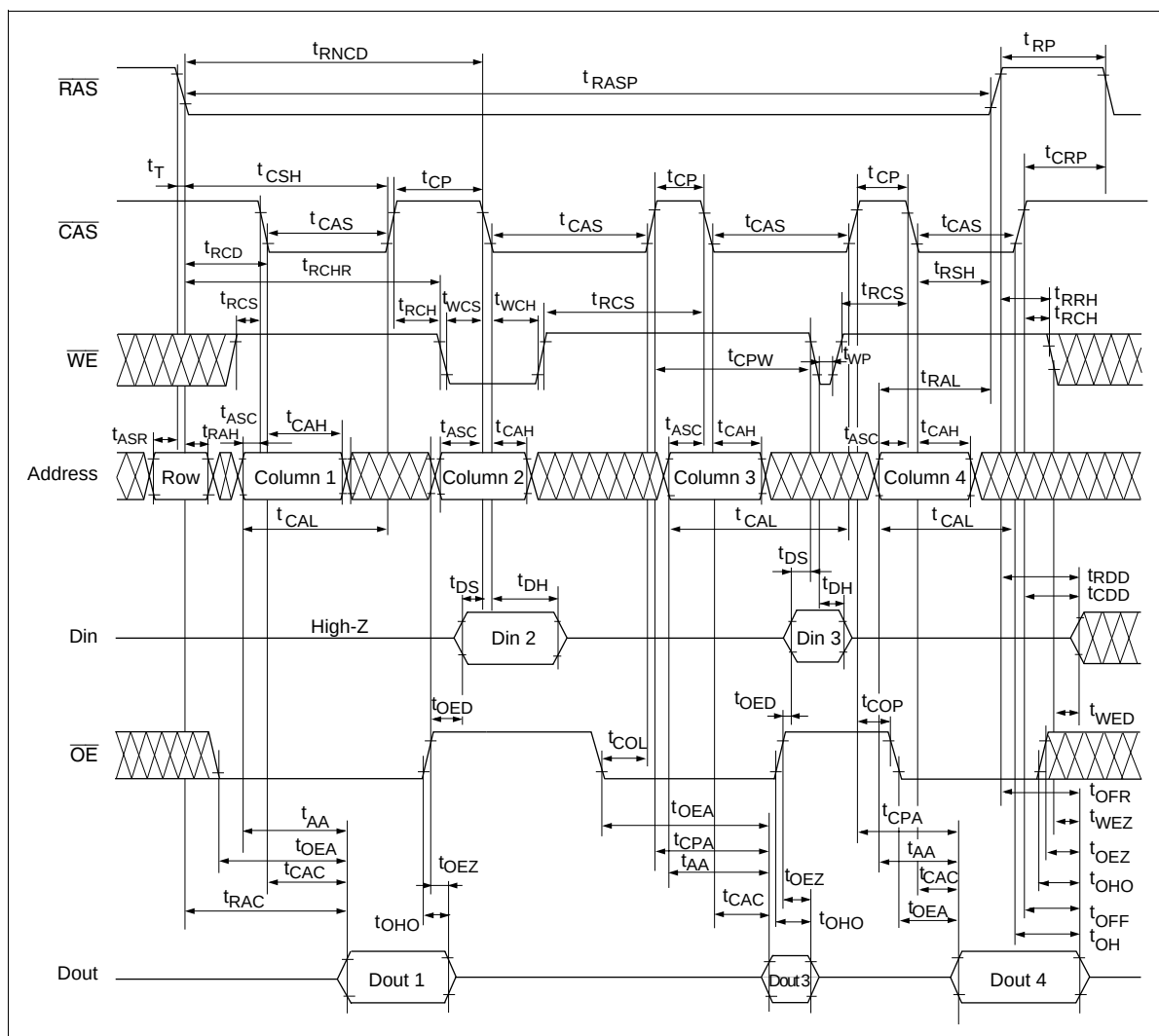
EDO Page Mode Read-Modify-Write Cycle*18



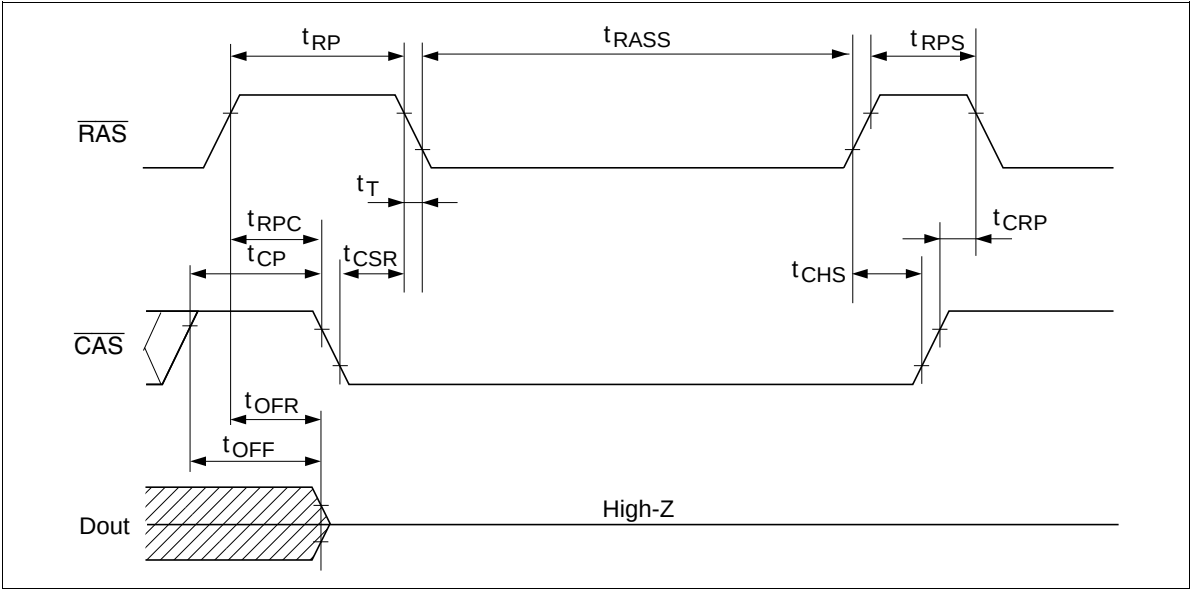
EDO Page Mode Mix Cycle (1)



EDO Page Mode Mix Cycle (2)

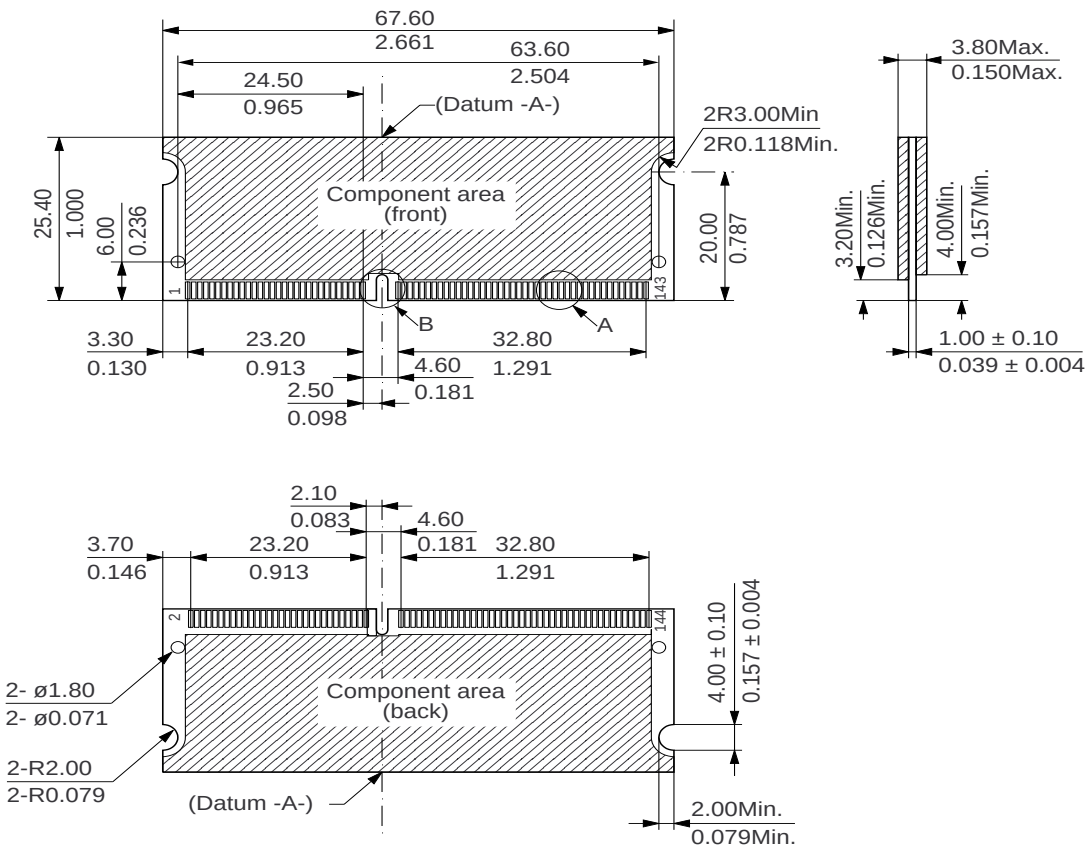


Self Refresh Cycle (only LS-version)* ^{23, 24, 25}

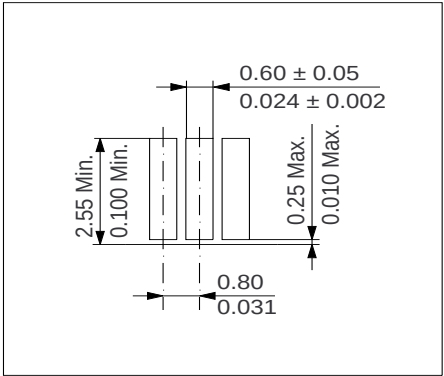


Physical Outline

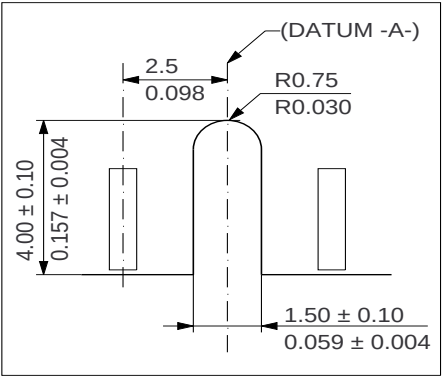
Unit: mm/inch



Detail A



Detail B



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HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

HB56SW464DB Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Mar. 20, 1997	Initial issue		
