HB56S1636 Series, HB56S1632 Series

16,777,216-word × 36-bit High Density Dynamic RAM Module
16,777,216-word × 32-bit High Density Dynamic RAM Module

HITACHI

ADE-203-694A (Z)
Rev. 1.0
May. 16, 1997

Description

The HB56S1636 is a 16M × 36 dynamic RAM module, mounted 36 pieces of 16-Mbit DRAM (HM5116105) sealed in TCP package. The HB56S1632 is a 16M × 32 dynamic RAM module, mounted 32 pieces of 16-Mbit DRAM (HM5116105) sealed in TCP package. An outline of the HB56S1636, HB56S1632 is 72-pin single in-line package. Therefore, the HB56S1636, HB56S1632 make high density mounting possible without surface mount technology. The HB56S1636, HB56S1632 provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

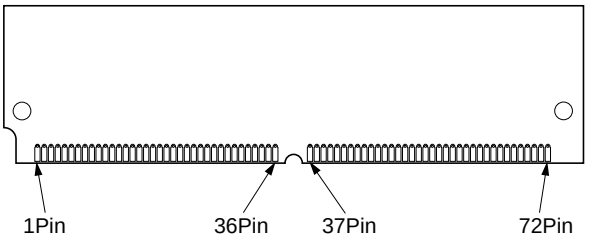
- 72-pin single in-line package
  - Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - Access time: t_{RAC} = 60 ns (max)
- Low power dissipation
  - Active mode: 15.12 W (max) (HB56S1636 Series)
    13.44 W (max) (HB56S1632 Series)
  - Standby mode (TTL): 378 mW (max) (HB56S1636 Series)
    (TTL): 336 mW (max) (HB56S1632 Series)
    (CMOS): 189 mW (max) (HB56S1636 Series)
    (CMOS): 168 mW (max) (HB56S1632 Series)
- EDO page mode capability
- 4,096 refresh cycles: 64 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Hitachi semiconductor

Ordering Information

Type No.	Access time	Package	Contact pad
HB56S1636BSC-6	60 ns	72-pin SIP socket type	Gold
HB56S1632BSC-6	60 ns		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	A10	37	DQ17 (NC)*2	55	DQ12
2	DQ0	20	DQ4	38	DQ35 (NC)*4	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	A11	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26 (NC)*3	53	DQ11	71	NC
18	A6	36	DQ8 (NC)*1	54	DQ29	72	V_{SS}

Notes: 1. DQ8: HB56S1636, NC: HB56S1632
2. DQ17: HB56S1636, NC: HB56S1632
3. DQ26: HB56S1636, NC: HB56S1632
4. DQ35: HB56S1636, NC: HB56S1632

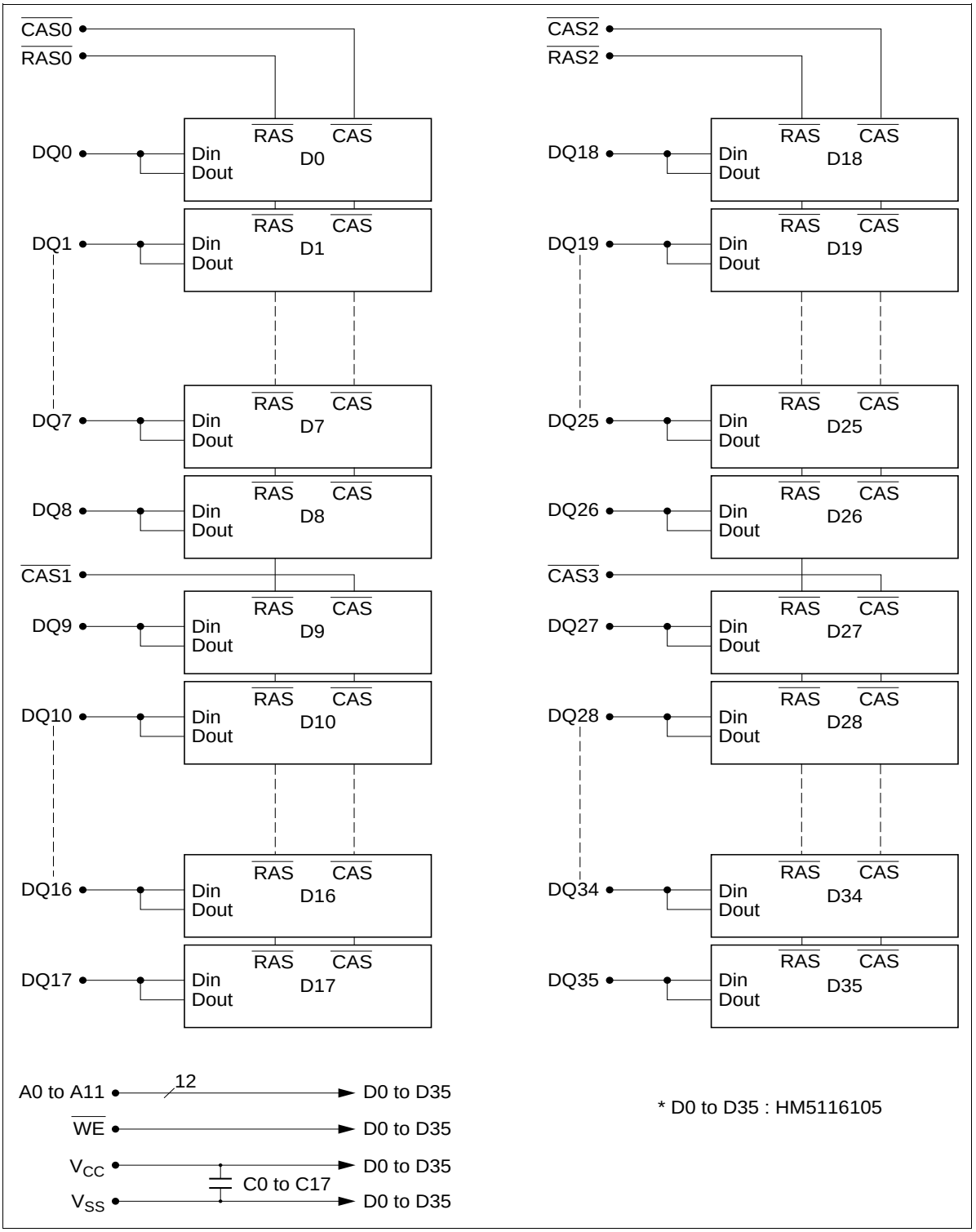
Pin Description

Pin name	Function
A0 to A11	Address inputs — Row address: A0 to A11 — Column address: A0 to A11 — Refresh address: A0 to A11
DQ0 to DQ35	Data-in/Data-out
$\overline{RAS0}$, $\overline{RAS2}$	Row address strobe
$\overline{CAS0}$ to $\overline{CAS3}$	Column address strobe
$\overline{WE}$	Read/Write enable
V_{cc}	Power supply
V_{ss}	Ground
PD1 to PD4	Presence detect pin
NC	No connection

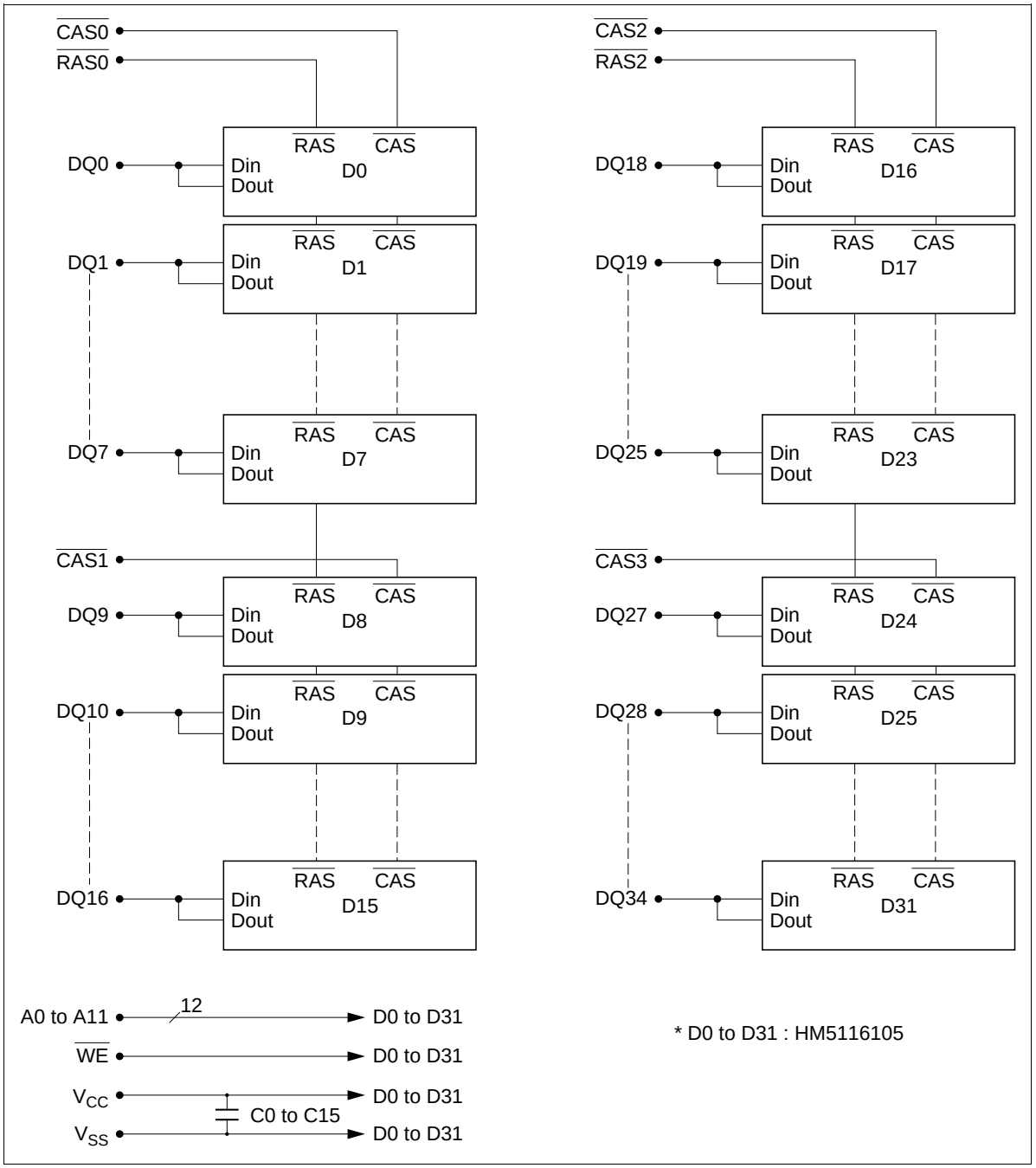
Presence Detect Pin Arrangement

Pin No.	Pin name	60 ns
67	PD1	V_{ss}
68	PD2	V_{ss}
69	PD3	NC
70	PD4	NC

Block Diagram (HB56S1636)



Block Diagram (HB56S1632)



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation (HB56S1636)	Pt	36	W
Power dissipation (HB56S1632)	Pt	32	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56S1636)

		60 ns				
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	2880	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	72	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	36	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	2880	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	180	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	2880	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	3600	mA	t_{HPC} = min	1, 3
Input leakage current	I_{LI}	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	µA	0 V ≤ Vout ≤ 5.5 V, Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56S1632)

		60 ns				
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	2560	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	64	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	32	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	2560	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	160	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	2560	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	3200	mA	t_{HPC} = min	1, 3
Input leakage current	I_{LI}	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	µA	0 V ≤ Vout ≤ 5.5 V, Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56S1636)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	195	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	267	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	146	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	83	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	25	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56S1632)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	175	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	239	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	132	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	76	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	25	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70˚C, V_{CC} = 5 V ±5%, V_{SS} = 0 V) *[1], *[2], *[18]

Test Conditions

- Input rise and fall times: 2 ns
- Input level: 0 V, 3.0V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, and Refresh Cycles (Common parameters)

		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	104	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	ns	
Row address setup time	t_{ASR}	0	—	ns	
Row address hold time	t_{RAH}	10	—	ns	
Column address setup time	t_{ASC}	0	—	ns	
Column address hold time	t_{CAH}	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	48	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	ns	
Transition time (rise and fall)	t_T	2	50	ns	5
Refresh period (4,096 cycles)	t_{REF}	—	64	ms	

Read Cycle

		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	15	ns	7, 8, 15
Access time from address	t_{AA}	—	30	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	ns	10
Read command hold time from $\overline{RAS}$	t_{RCHR}	60	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	18	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	ns	
Output data hold time	t_{OH}	3	—	ns	19
Output buffer turn-off time	t_{OFF}	—	15	ns	11, 19
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	ns	
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	ns	19
Output buffer turn-off time to $\overline{RAS}$	t_{OFR}	—	15	ns	19
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	15	ns	
$\overline{WE}$ to Din delay time	t_{WED}	15	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	15	—	ns	
$\overline{RAS}$ to next $\overline{CAS}$ delay time	t_{RNCD}	60	—	ns	

Write Cycle

		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	ns	12
Write command hold time	t_{WCH}	10	—	ns	
Write command pulse width	t_{WP}	10	—	ns	
Data-in setup time	t_{DS}	0	—	ns	13
Data-in hold time	t_{DH}	10	—	ns	13

Refresh Cycle

		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	ns	

EDO Page Mode Cycle

		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	25	—	ns	16
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	ns	7, 15
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	ns	7, 15
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	ns	

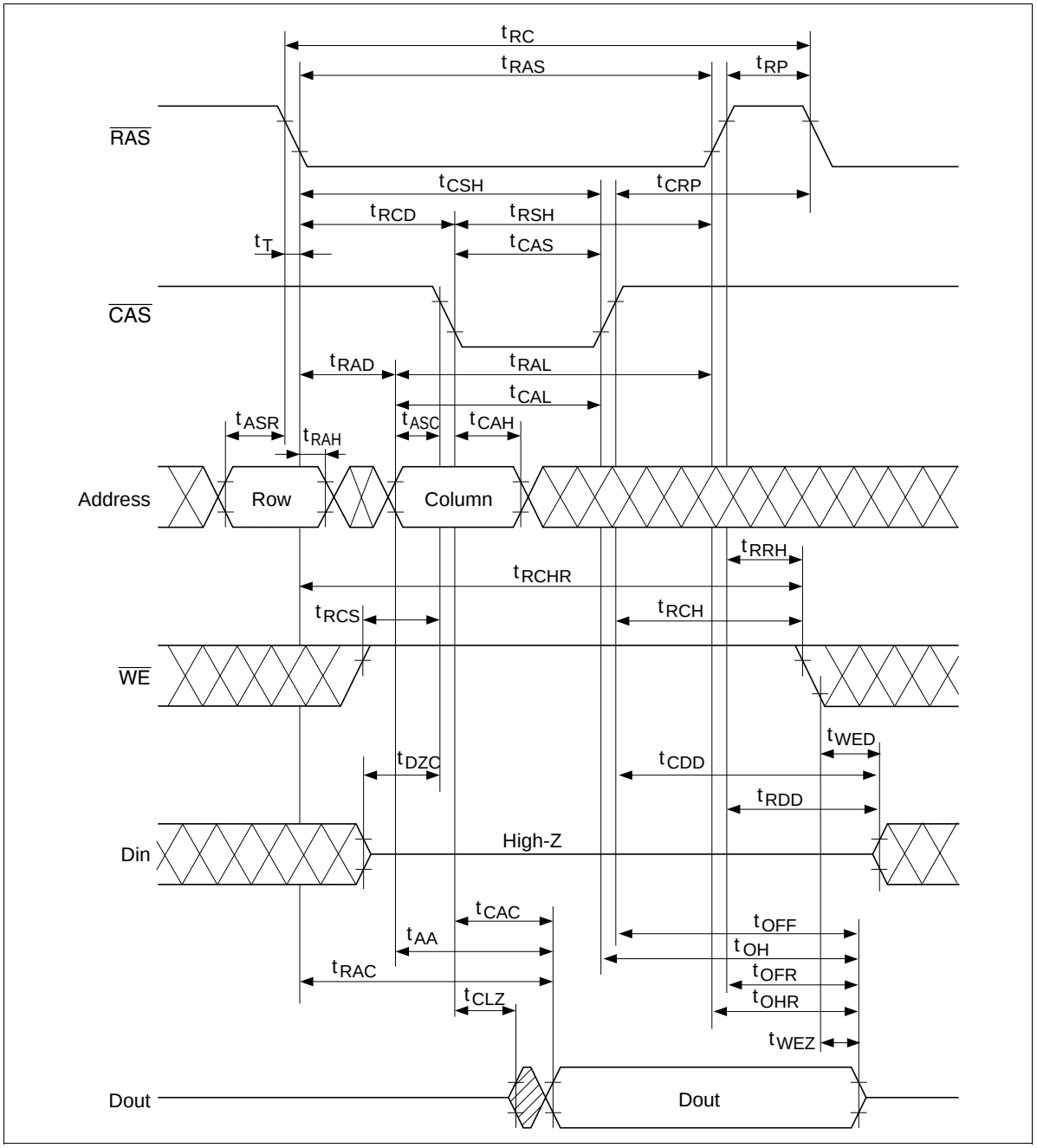
Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RCD}$ (max) + t_{AA} (max) - t_{CAC} (max), then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and t_{RCD} + t_{CAC} (max) $\geq t_{RAD}$ + t_{AA} (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and t_{RCD} + t_{CAC} (max) $\leq t_{RAD}$ + t_{AA} (max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
11. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
12. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
13. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
15. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
16. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles.
17. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
19. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.
20. XXX: H or L (H: V_{IH} (min) $\leq V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) $\leq V_{IN} \leq V_{IL}$ (max))

    ///////: Invalid Dout

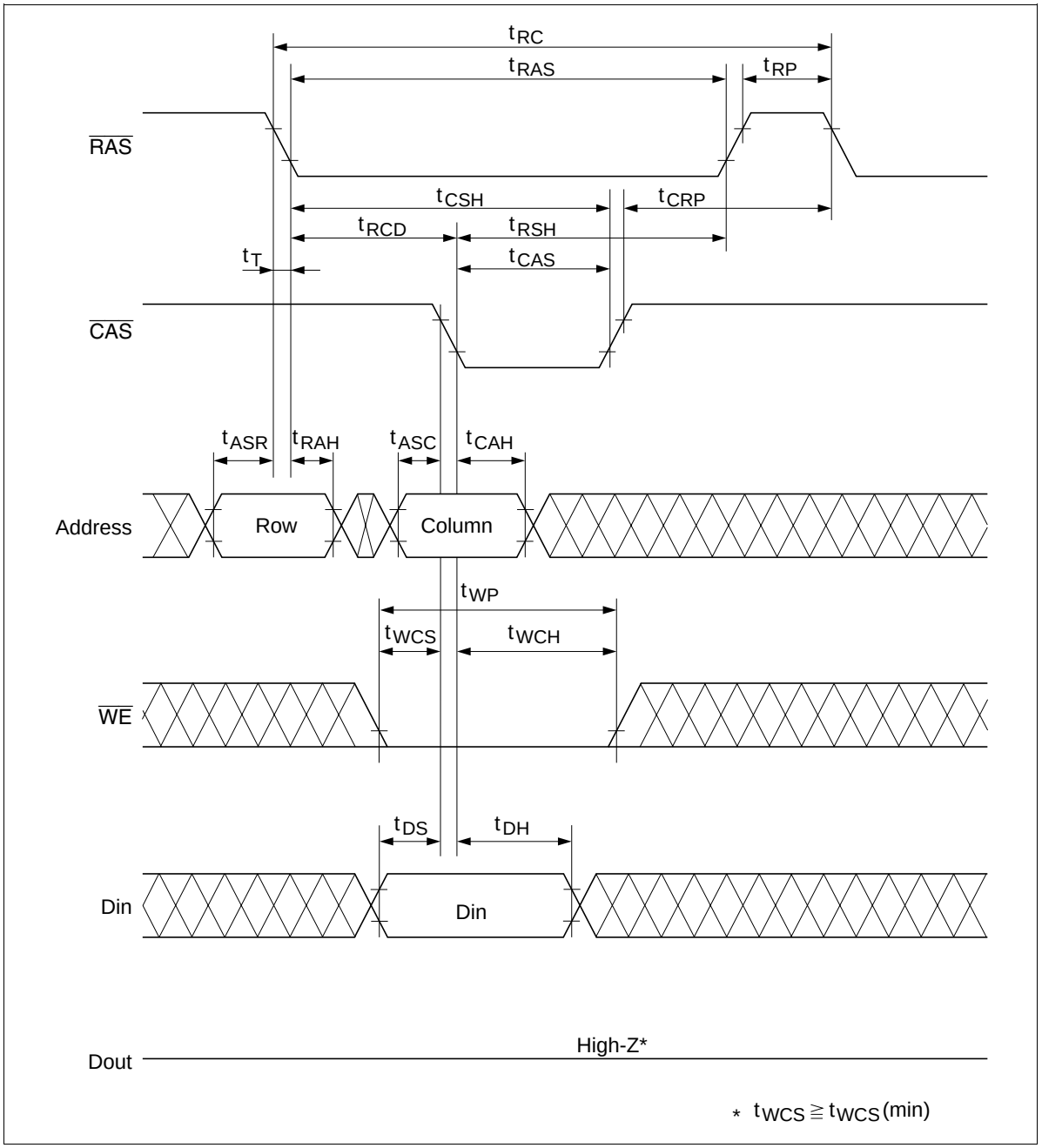
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[20]

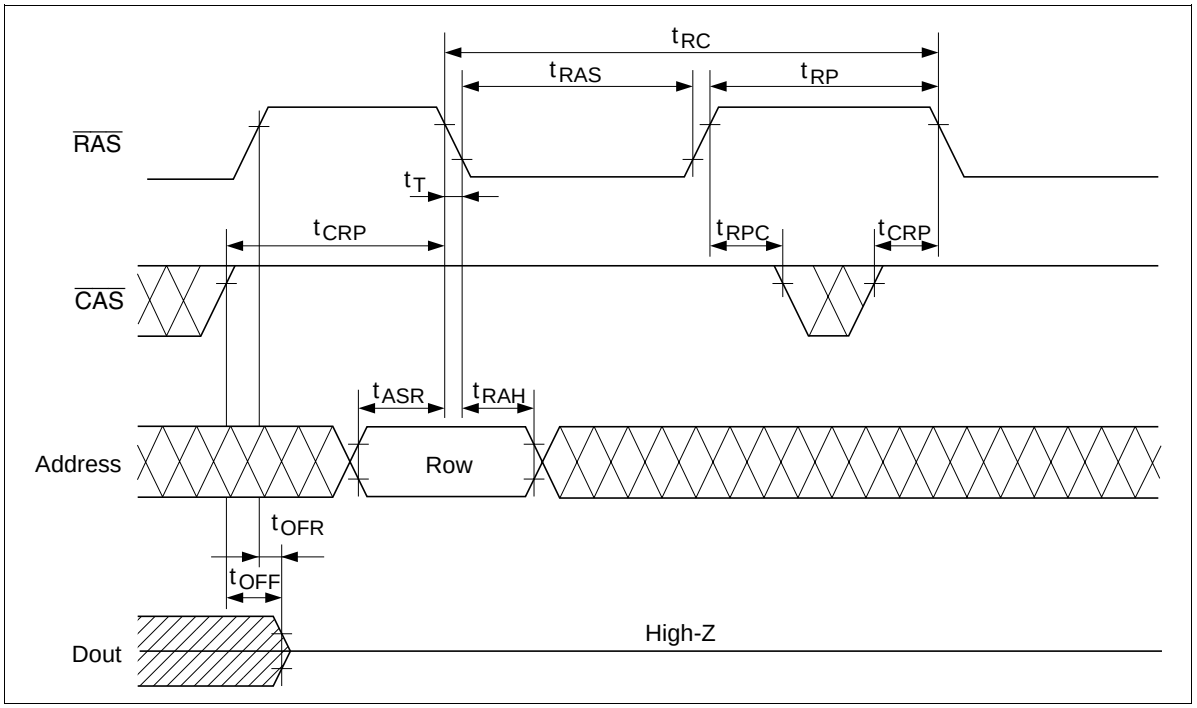
Read Cycle



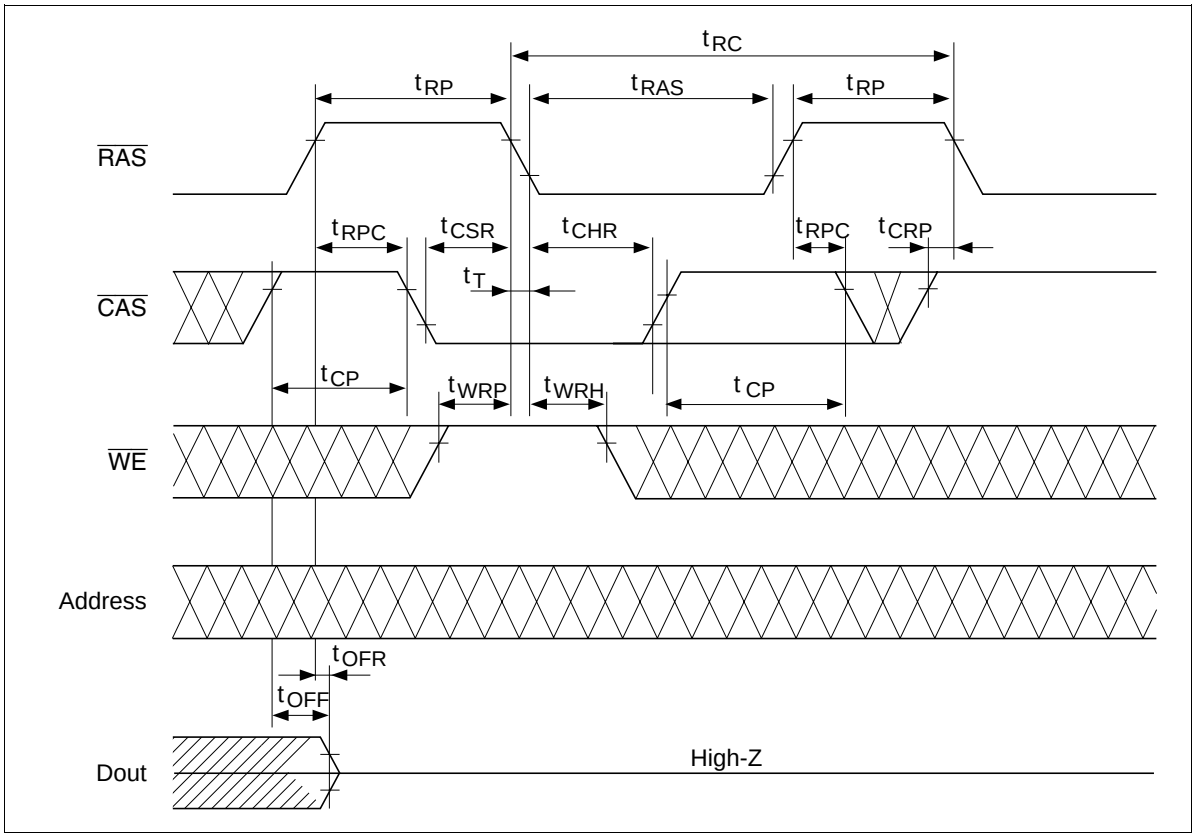
Early Write Cycle



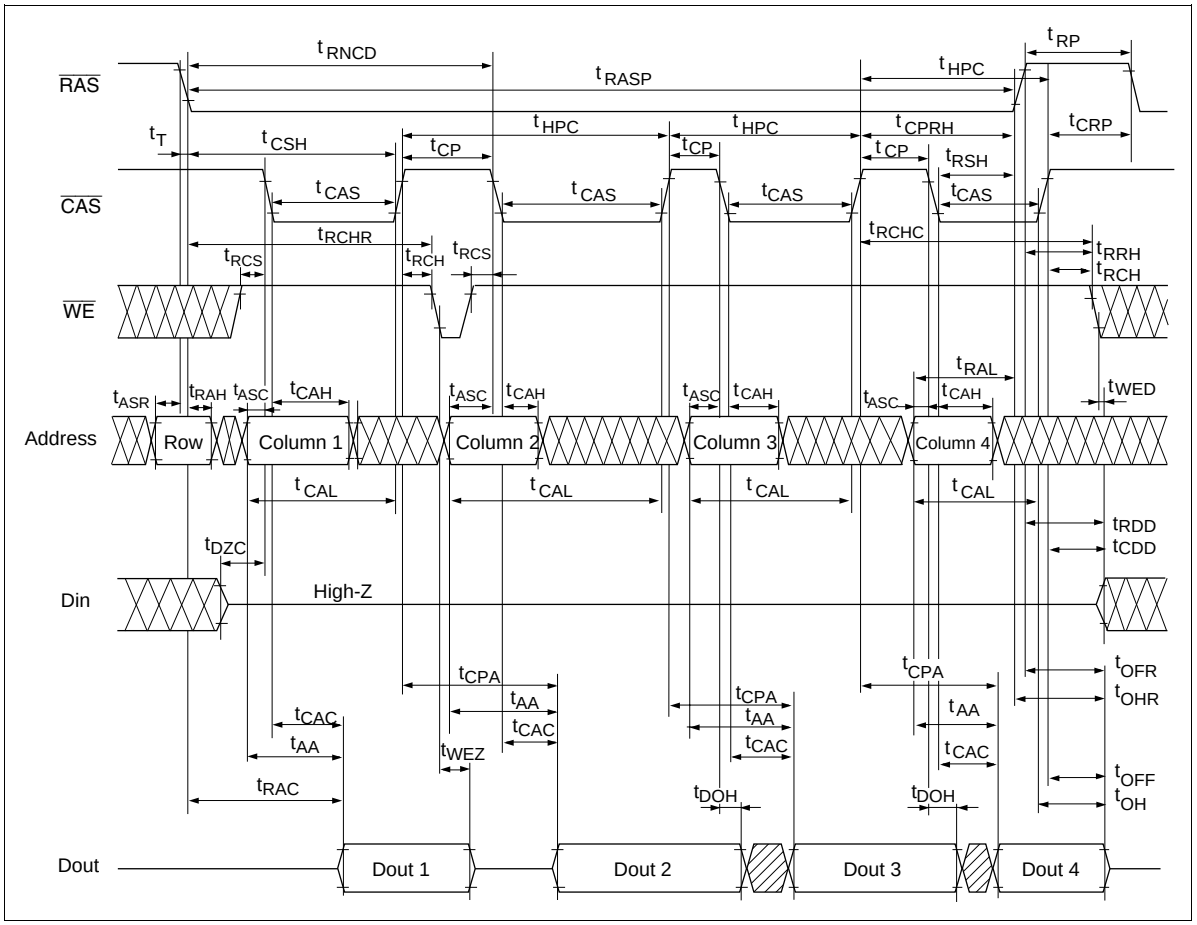
$\overline{\text{RAS}}$-Only Refresh Cycle



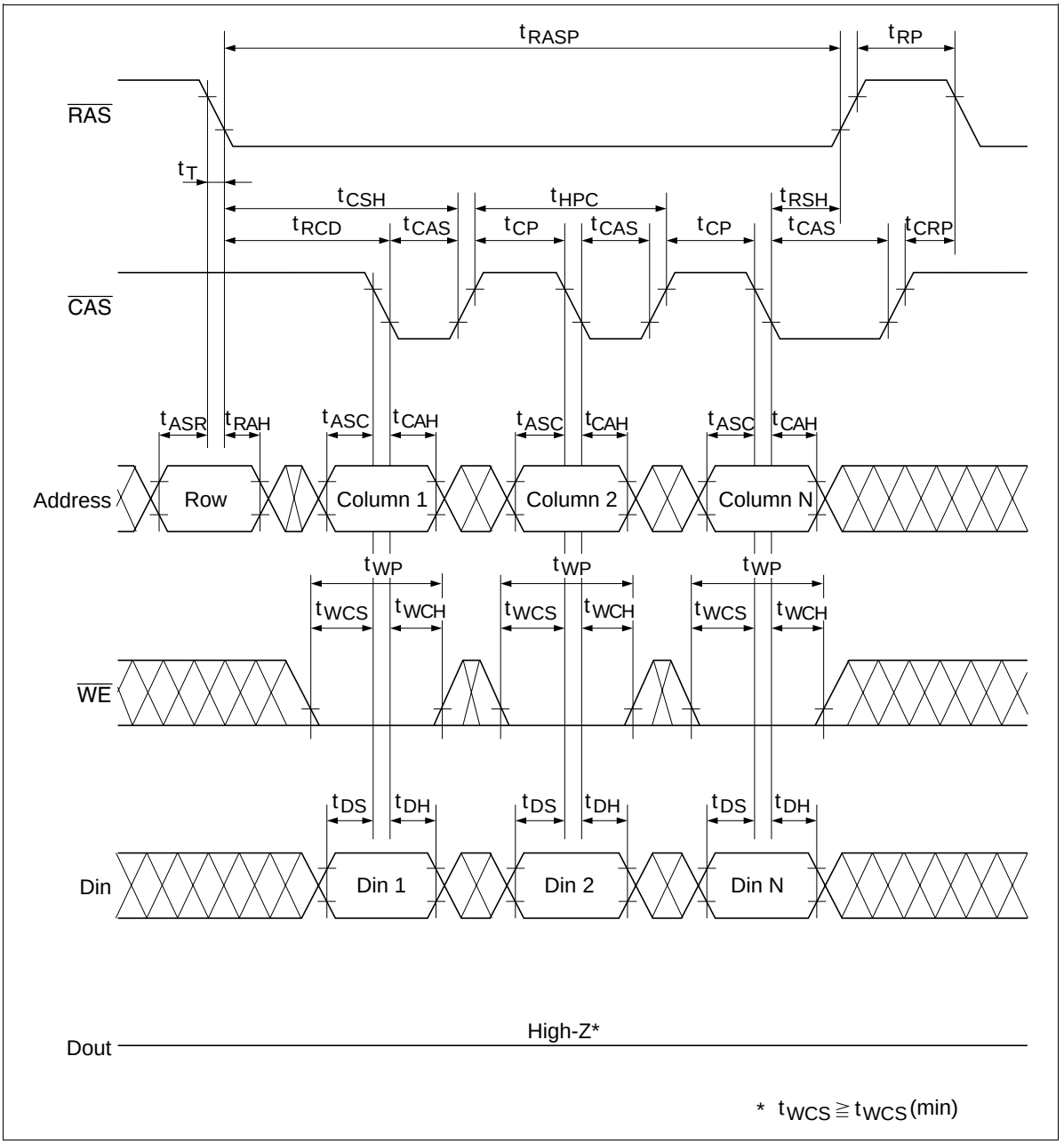
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



EDO Page Mode Read Cycle

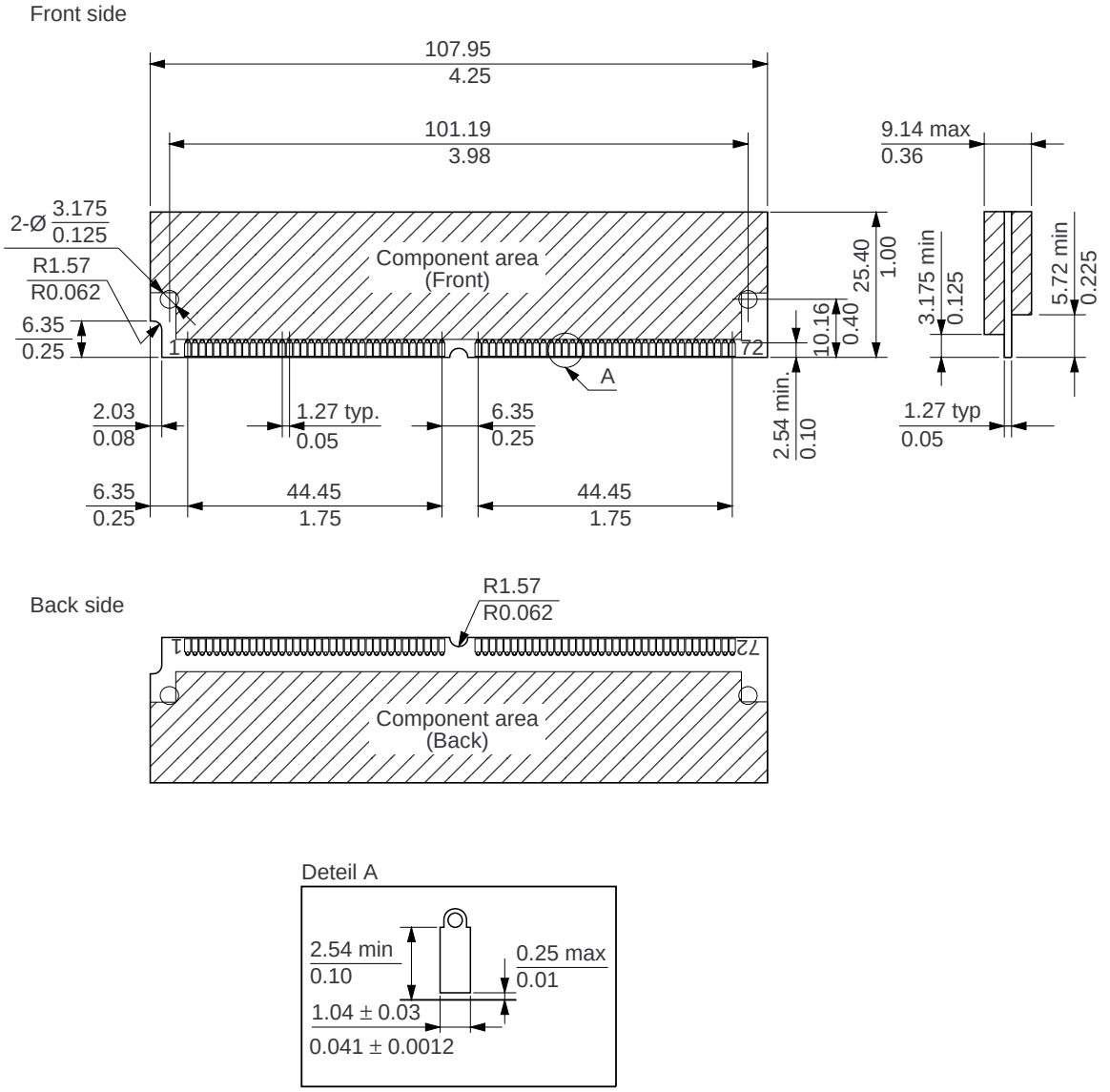


EDO Page Mode Early Write Cycle



Physical Outline

Unit: mm / inch



Note: Tolerance on all dimensions ±0.13/0.005 unless otherwise specified.

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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Dec. 25, 1996	Initial issue	T. Sugano	K. Inoue
1.0	May. 16, 1997	DC Characteristics I_{LI} test conditions: 0 V ≤ Vin ≤ 7.0 V to 0 V ≤ Vin ≤ 5.5 V I_{LO} test conditions: 0 V ≤ Vout ≤ 7.0 V to 0 V ≤ Vout ≤ 5.5 V V_{OH} test conditions: –5 mA to –2 mA V_{OL} test conditions: 4.2 mA to 2 mA AC Characteristics t_{RRH} min: 0 ns to 5 ns Addition of t_{RNCD} t_{RPC} min: 0 ns to 5 ns Addition of notes12, 16, 17, 18 and 19 Timing Waveforms Deletion of Hidden refresh Addition of t_{RNCD} for EDO Page Mode Read		