
HB56HW164EJN Series

1,048,576-word $\times$ 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-696A (Z)

Rev.1.0

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Description

The HB56HW164EJN belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56HW164EJN is a 1M $\times$ 64 dynamic RAM module, mounted 4 pieces of 16-Mbit DRAM (HM51W18165) sealed in SOJ package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56HW164EJN offers Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56HW164EJN is 168-pin socket type package (dual lead out). Therefore, the HB56HW164EJN makes high density mounting possible without surface mount technology. The HB56HW164EJN provides common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 168-pin socket type package (Dual lead out)
 - Outline: 133.35 mm (Length) $\times$ 25.40 mm (Height) $\times$ 5.28 mm (Thickness)
 - Lead pitch: 1.27 mm
- Single 3.3 V (± 0.3 V) supply
- High speed
 - Access time: $t_{\text{RAC}} = 60/70\text{ns}$ (max)
 $t_{\text{CAC}} = 15/18\text{ns}$ (max)
- Low power dissipation
 - Active mode: 2.45/2.16W (max)
 - Standby mode (TTL): 28.8 mW (max)
(CMOS): 2.16 mW (max) (L-version)
- JEDEC standard outline unbuffered 8-byte DIMM
- EDO page mode capability
- Refresh period
 - 1024 refresh cycles: 16 ms
128 ms (L-version)

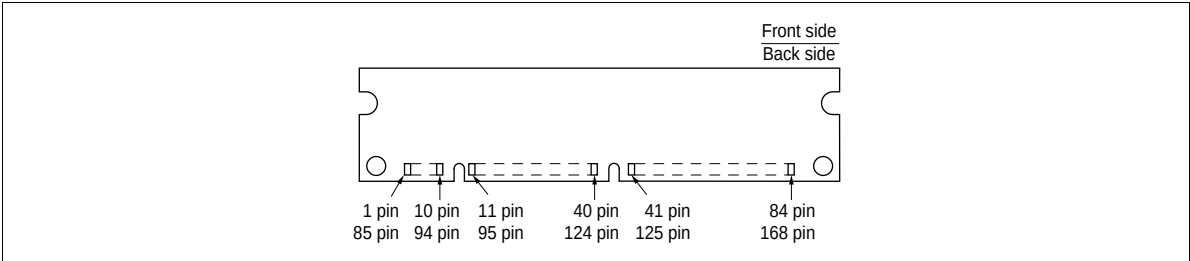
HB56HW164EJN Series

- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)

Ordering Information

Type No.	Access time	Package	Contact pad
HB56HW164EJN-6	60 ns	168-pin dual lead out socket type	Gold
HB56HW164EJN-7	70 ns		
HB56HW164EJN-6L	60 ns		
HB56HW164EJN-7L	70 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ32	128	NC
3	DQ1	45	$\overline{\text{RAS2}}$	87	DQ33	129	NC
4	DQ2	46	$\overline{\text{CAS2}}$	88	DQ34	130	$\overline{\text{CAS6}}$
5	DQ3	47	$\overline{\text{CAS3}}$	89	DQ35	131	$\overline{\text{CAS7}}$
6	V _{CC}	48	$\overline{\text{WE2}}$	90	V _{CC}	132	NC
7	DQ4	49	V _{CC}	91	DQ36	133	V _{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{CC}	101	DQ45	143	V _{CC}
18	V _{CC}	60	DQ20	102	V _{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	NC	105	NC	147	NC
22	NC	64	V _{SS}	106	NC	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V _{CC}	68	V _{SS}	110	V _{CC}	152	V _{SS}
27	$\overline{\text{WE0}}$	69	DQ24	111	NC	153	DQ56
28	$\overline{\text{CAS0}}$	70	DQ25	112	$\overline{\text{CAS4}}$	154	DQ57
29	$\overline{\text{CAS1}}$	71	DQ26	113	$\overline{\text{CAS5}}$	155	DQ58
30	$\overline{\text{RAS0}}$	72	DQ27	114	NC	156	DQ59
31	$\overline{\text{OE0}}$	73	V _{CC}	115	NC	157	V _{CC}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62

Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	NC	121	A9	163	NC
38	NC	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V _{CC}	82	SDA	124	V _{CC}	166	SA1
41	V _{CC}	83	SCL	125	NC	167	SA2
42	NC	84	V _{CC}	126	NC	168	V _{CC}

Pin Description

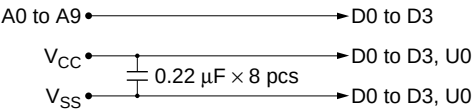
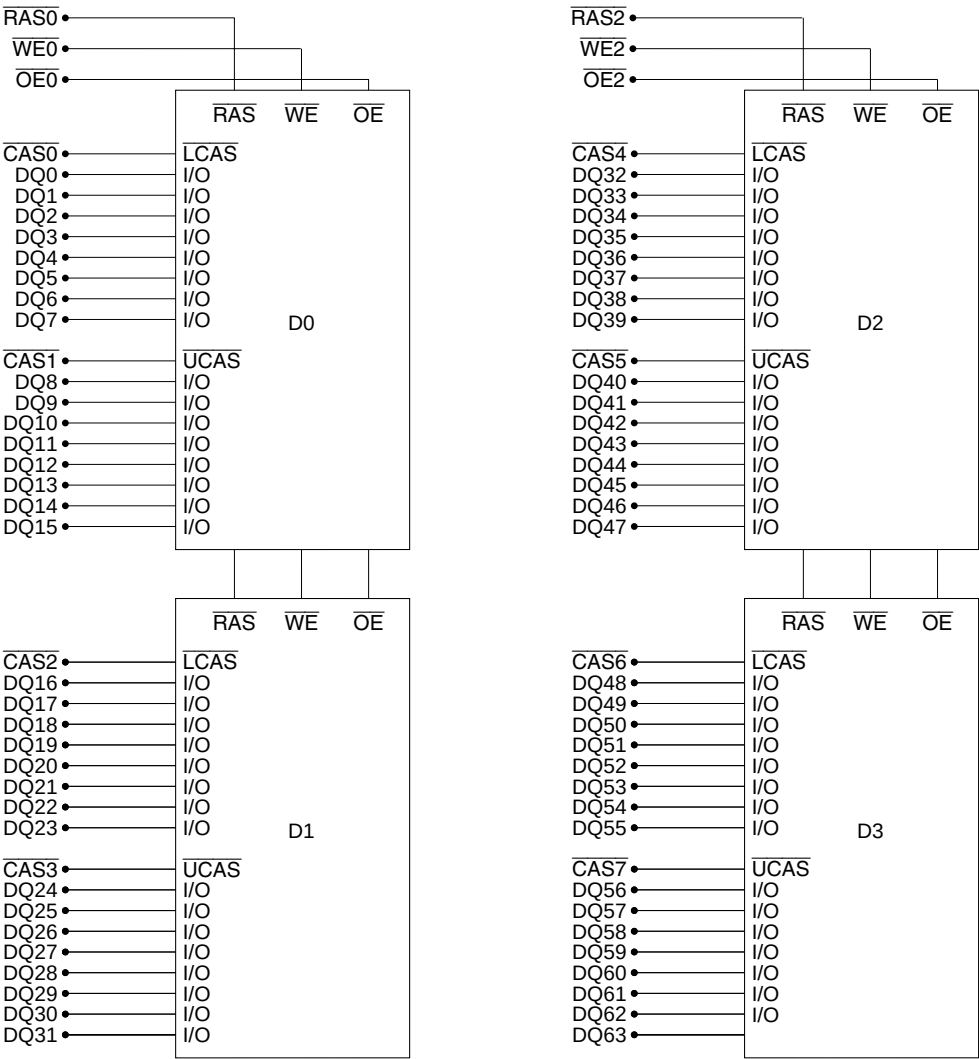
Pin name	Function
A0 to A9	Address input — Row address: A0 to A9 — Column address: A0 to A9 — Refresh address: A0 to A9
DQ0 to DQ63	Data-in/data-out
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row address strobe
$\overline{\text{CAS0}}$ to $\overline{\text{CAS7}}$	Column address strobe
$\overline{\text{WE0}}, \overline{\text{WE2}}$	Read/Write enable
$\overline{\text{OE0}}, \overline{\text{OE2}}$	Output enable
SDA	Serial data for PD
SCL	Serial clock for PD
SA0 to SA2	Serial address for PD
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Serial PD Matrix

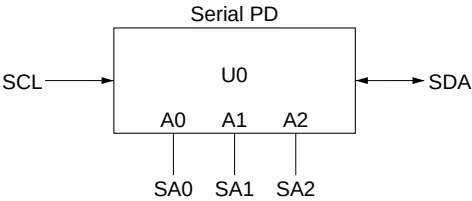
Byte number	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comments
0	Number Serial PD Bytes	0	0	0	0	1	1	0	1	13
1	Serial Memory	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental Memory Type	0	0	0	0	0	0	1	0	EDO
3	Number of Rows	0	0	0	0	1	0	1	0	10
4	Number of Columns	0	0	0	0	1	0	1	0	10
5	Number of Banks	0	0	0	0	0	0	0	1	1
6	Data Width	0	1	0	0	0	0	0	0	64
7	Data Width (continued)	0	0	0	0	0	0	0	0	0 (+)
8	Voltage Interface	0	0	0	0	0	0	0	1	3.3 Volt
9	$\overline{\text{RAS}}$ Access Time 60 ns	0	0	1	1	1	1	0	0	
	70 ns	0	1	0	0	0	1	1	0	
10	$\overline{\text{CAS}}$ Access Time 15 ns	0	0	0	0	1	1	1	1	
	18 ns	0	0	0	1	0	0	1	0	
11	Error Detection/Corraction	0	0	0	0	0	0	0	0	None-parity
12	Refresh Period	0	0	0	0	0	0	0	0	Normal (15.625 μs)
	Refresh Period (L-version)	1	0	0	0	0	1	0	1	Self refresh (125 μs)

Note: Serial-PD data are not protected.
1: High level (Serial data)
0: Low level (Serial data)

Block Diagram



* D0 to D3 : HM51W18165
U0 : 24C02



- Note
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
 2. The SCL pull-up resistor is recommended because of the normal SCL line inactive "High" state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	4	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0 \text{ to } 70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	−0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V)

Parameter	Symbol	60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I _{CC1}	—	680	—	600	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	8	—	8	mA	TTL interface R _{AS} , C _{AS} = V _{IH} Dout = High-Z	
		—	4	—	4	mA	CMOS interface R _{AS} , C _{AS} ≥ V _{CC} − 0.2 V Dout = High-Z	
Standby current (L-version)	I _{CC2}	—	0.6	—	0.6	mA	CMOS interface R _{AS} , C _{AS} ≥ V _{CC} − 0.2 V Dout = High-Z	
R _{AS} -only refresh current	I _{CC3}	—	680	—	600	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	20	—	20	mA	R _{AS} = V _{IH} , C _{AS} = V _{IL} Dout = enable	1
C _{AS} -before-R _{AS} refresh current	I _{CC6}	—	680	—	600	mA	t _{RC} = min	
EDO page mode current	I _{CC7}	—	740	—	660	mA	t _{HPC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I _{CC10}	—	1.6	—	1.6	mA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 125 μs t _{RAS} ≤ 0.3 μs	4
Self refresh mode current (L-version)	I _{CC11}	—	1	—	1	mA	CMOS interface R _{AS} , C _{AS} ≤ 0.2 V Dout = High-Z	
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while R_{AS} = V_{IL}.
3. Address can be changed once or less while C_{AS} = V_{IH}.
4. V_{IH} ≥ V_{CC} − 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{II}	—	40	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I2}	—	34	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C _{I3}	—	27	pF	1
I/O capacitance (DQ)	C _{I/O}	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V) *¹, *², *¹⁸, *¹⁹

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

HB56HW164EJN Series

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	104	—	124	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	13	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	10	10000	13	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	ns	
Column address hold time	t _{CAH}	10	—	13	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	45	20	52	ns	3
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	30	15	35	ns	4
$\overline{\text{RAS}}$ hold time	t _{RSH}	15	—	18	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	40	—	45	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	t _{OED}	15	—	18	—	ns	5
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	t _{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	2	50	2	50	ns	7
Refresh period (1,024 cycles)	t _{REF}	—	16	—	16	ms	
Refresh period (1,024 cycles) (L-version)	t _{REF}	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	22
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13, 22
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	ns	22
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	ns	
$\overline{\text{RAS}}$ next $\overline{\text{CAS}}$ delay time	t_{RNCDD}	60	—	70	—	ns	

Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	t _{WCS}	0	—	0	—	ns	14
Write command hold time	t _{WCH}	10	—	13	—	ns	
Write command pulse width	t _{WP}	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	10	—	13	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	10	—	13	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	ns	15
Data-in hold time	t _{DH}	10	—	13	—	ns	15

Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Read-modify-write cycle time	t _{RWC}	136	—	161	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	79	—	92	—	ns	14
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	34	—	40	—	ns	14
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	49	—	57	—	ns	14
$\overline{\text{OE}}$ hold time $\overline{\text{WE}}$	t _{OEH}	15	—	18	—	ns	

Refresh Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{\text{CAS}}$ setup time (CBR refresh cycle)	t _{CSR}	5	—	5	—	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh cycle)	t _{CHR}	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	t _{RPC}	0	—	0	—	ns	

EDO Page Mode Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode cycle time	t_{HPC}	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	ns	
Output data hole time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	t_{HPRWC}	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	54	—	62	—	ns	14

Self Refresh Mode (L-version)

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{\text{RAS}}$ pulse width (Self refresh)	t_{RASS}	100	—	100	—	μs	
$\overline{\text{RAS}}$ precharge time (Self refresh)	t_{RPS}	110	—	130	—	ns	
$\overline{\text{CAS}}$ hold time (Self refresh)	t_{CHS}	-50	—	-50	—	ns	

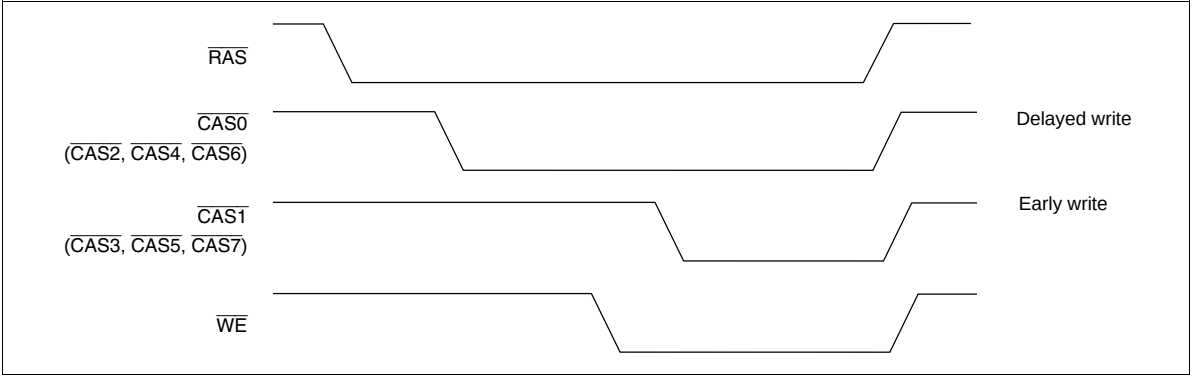
- Notes:
1. AC measurements assume $t_f = 2 \text{ ns}$.
 2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{\text{RCD}} \geq t_{\text{RAD}} (\text{max}) + t_{\text{AA}} (\text{max}) - t_{\text{CAC}} (\text{max})$, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}} (\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 11. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. $t_{\text{OFF}} (\text{max})$ and $t_{\text{OEZ}} (\text{max})$ define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} , and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$, and $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ or $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}} (\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device. After $\overline{\text{RAS}}$ is reset, if $t_{\text{OEH}} \geq t_{\text{CWL}}$, the DQ pin will remain open circuit (high impedance); $t_{\text{OEH}} < t_{\text{OEH}}$, invalid data will be out at each DQ.
 19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.

20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
22. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} , and between t_{OFF} and t_{OFF} .
23. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP} .
24. If you use distributed CBR refresh mode with $15.6 \mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6 \mu s$ immediately after exiting from and before entering into self refresh mode.
25. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 of distributed CBR refresh with $15.6 \mu s$ interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
27. XXX: H or L (H: $V_{IH} (\min) \leq V_{IN} \leq V_{IH} (\max)$, L: $V_{IL} (\min) \leq V_{IN} \leq V_{IL} (\max)$)
 //////////////: Invalid Dout
 When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

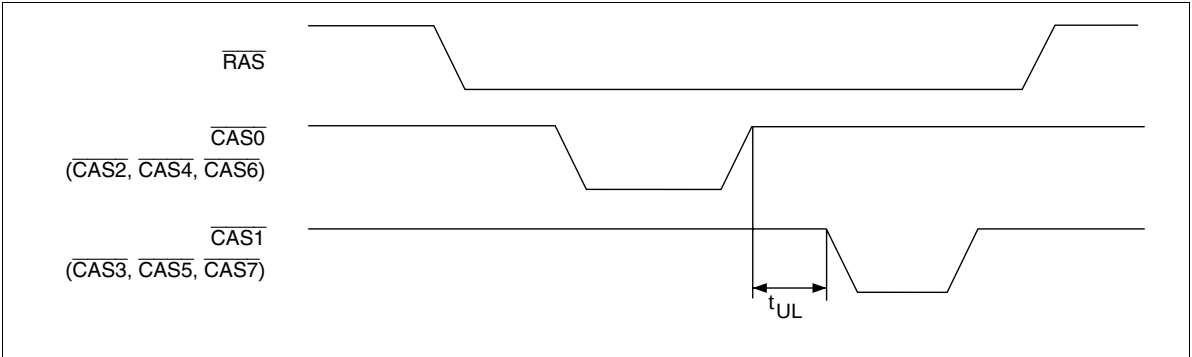
Notes concerning 2CAS control

Please do not separate the 2CASs ($\overline{\text{CAS}}0$ and $\overline{\text{CAS}}1$ (or $\overline{\text{CAS}}2$, $\overline{\text{CAS}}4$, $\overline{\text{CAS}}6$ and $\overline{\text{CAS}}3$, $\overline{\text{CAS}}5$, $\overline{\text{CAS}}7$)) operation timing intentionally. However skew between 2CASs are allowed under the following conditions.

- 1. Each of the 2CASs should satisfy the timing specifications individually.
- 2. Different operation mode for upper/lower byte is not allowed: such as following.



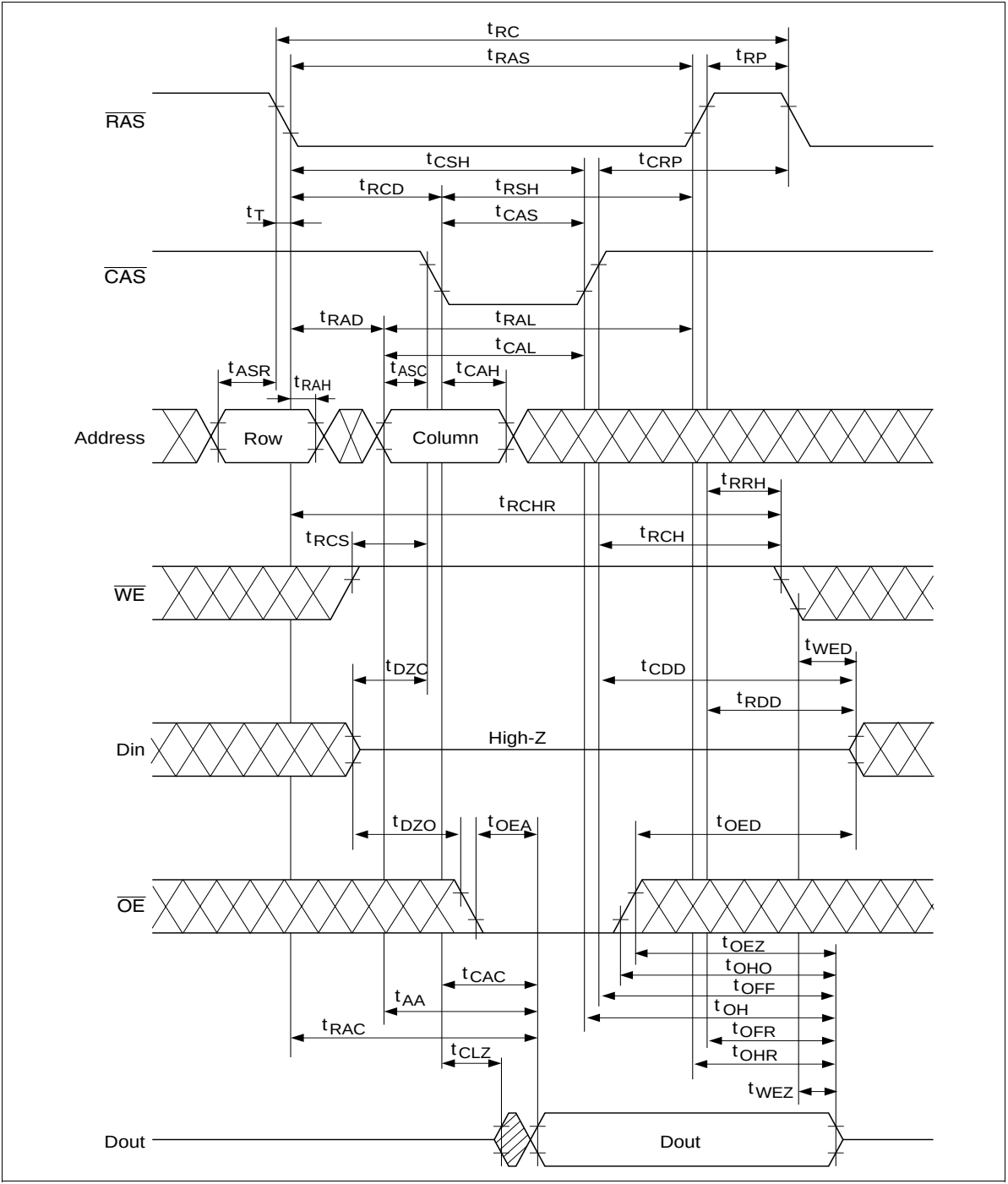
- 3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{\text{CP}} \leq t_{\text{UL}}$) is satisfied, page mode can be performed.



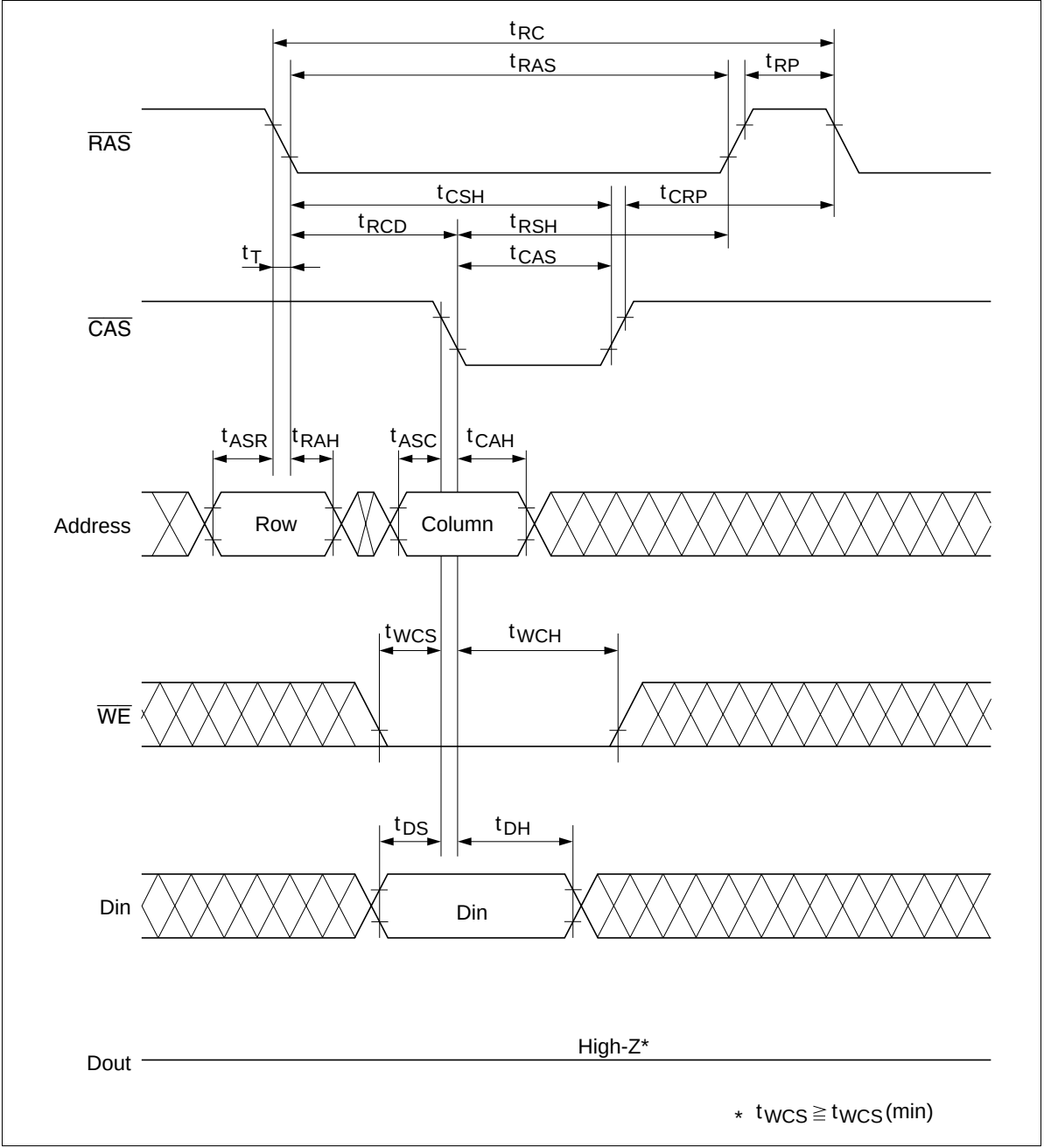
- 4. Byte control operation by remaining $\overline{\text{CAS}}0$ ($\overline{\text{CAS}}2$, $\overline{\text{CAS}}4$, $\overline{\text{CAS}}6$) or $\overline{\text{CAS}}1$ ($\overline{\text{CAS}}3$, $\overline{\text{CAS}}5$, $\overline{\text{CAS}}7$) high is guaranteed.

Timing Waveforms*27

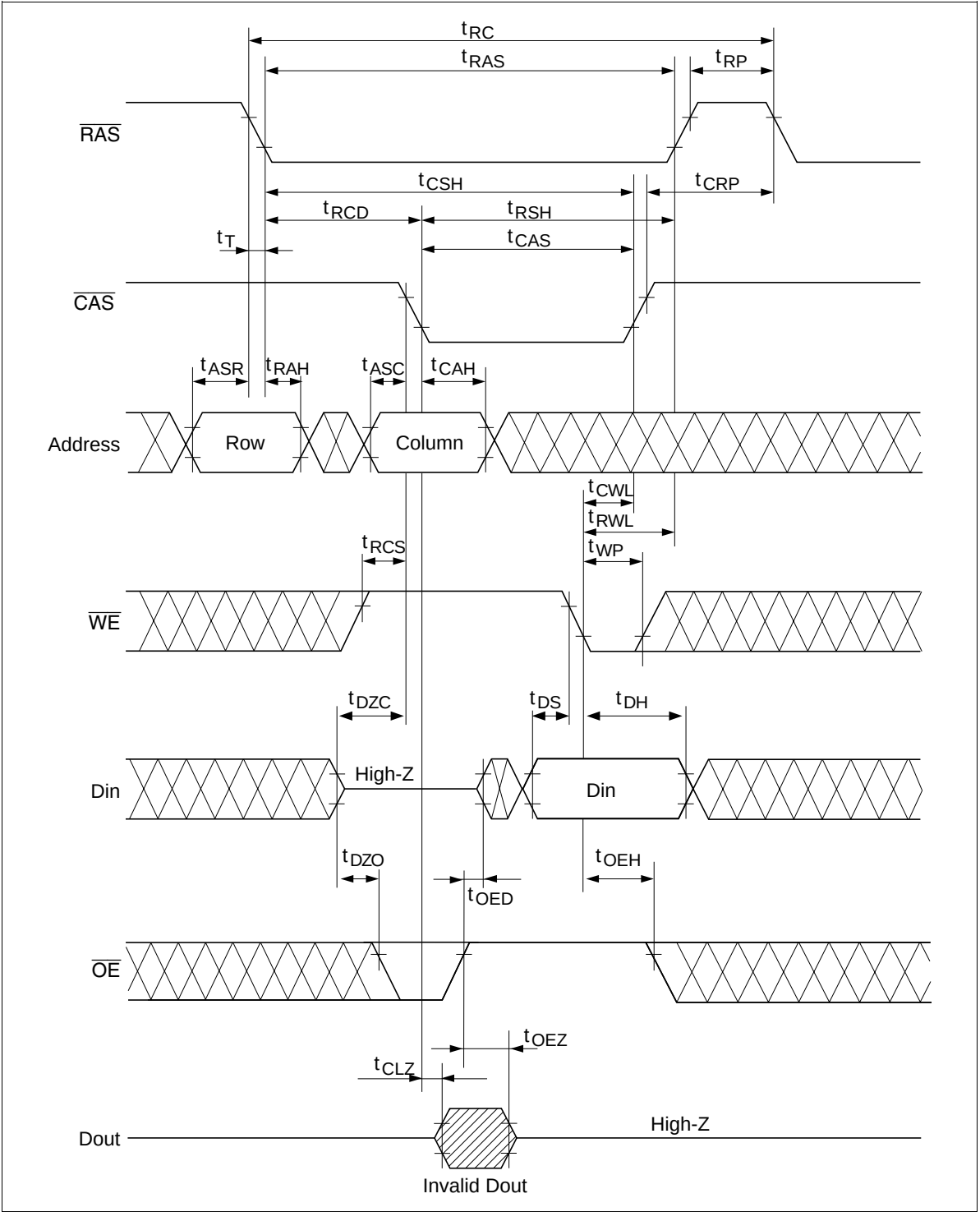
Read Cycle



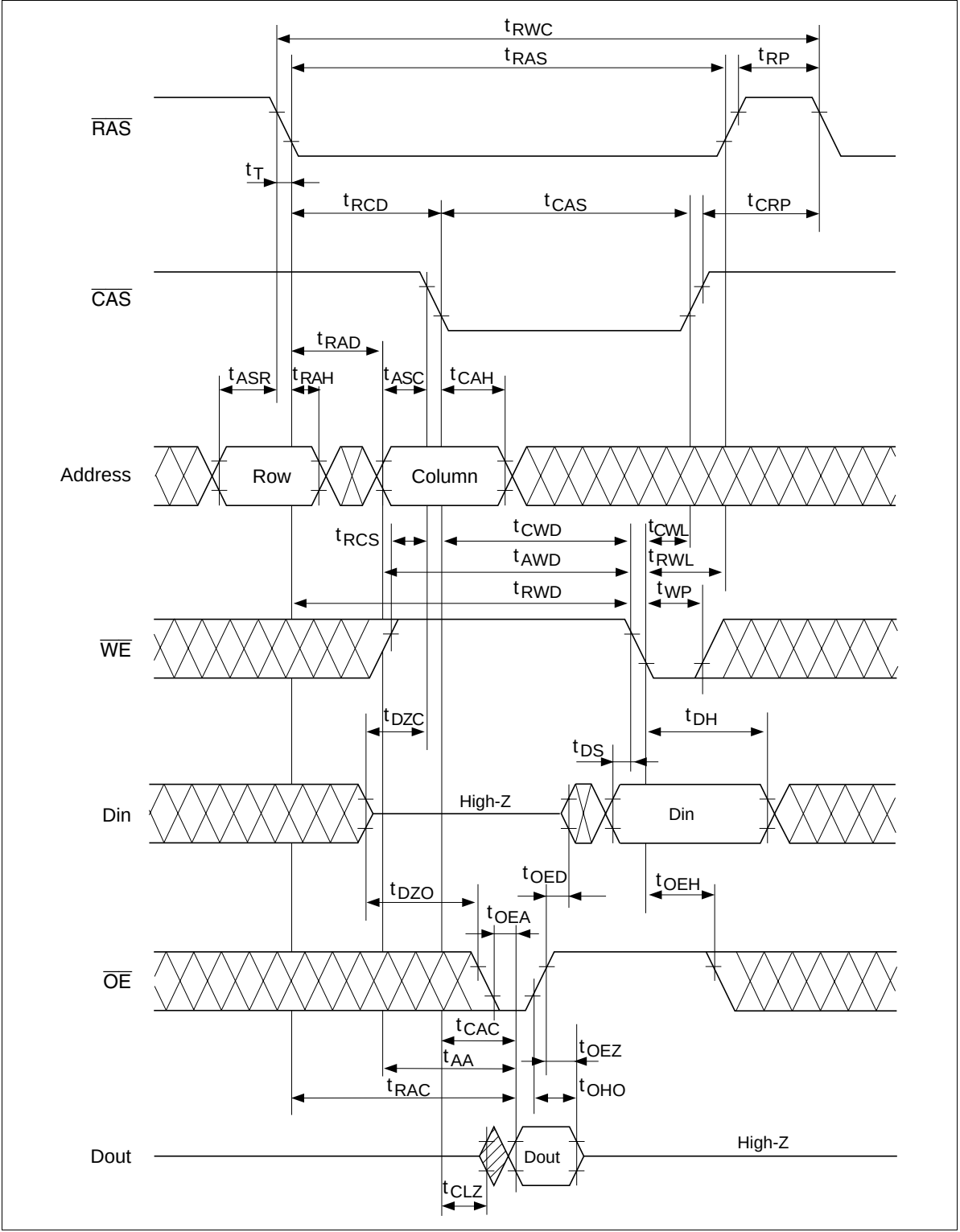
Early Write Cycle



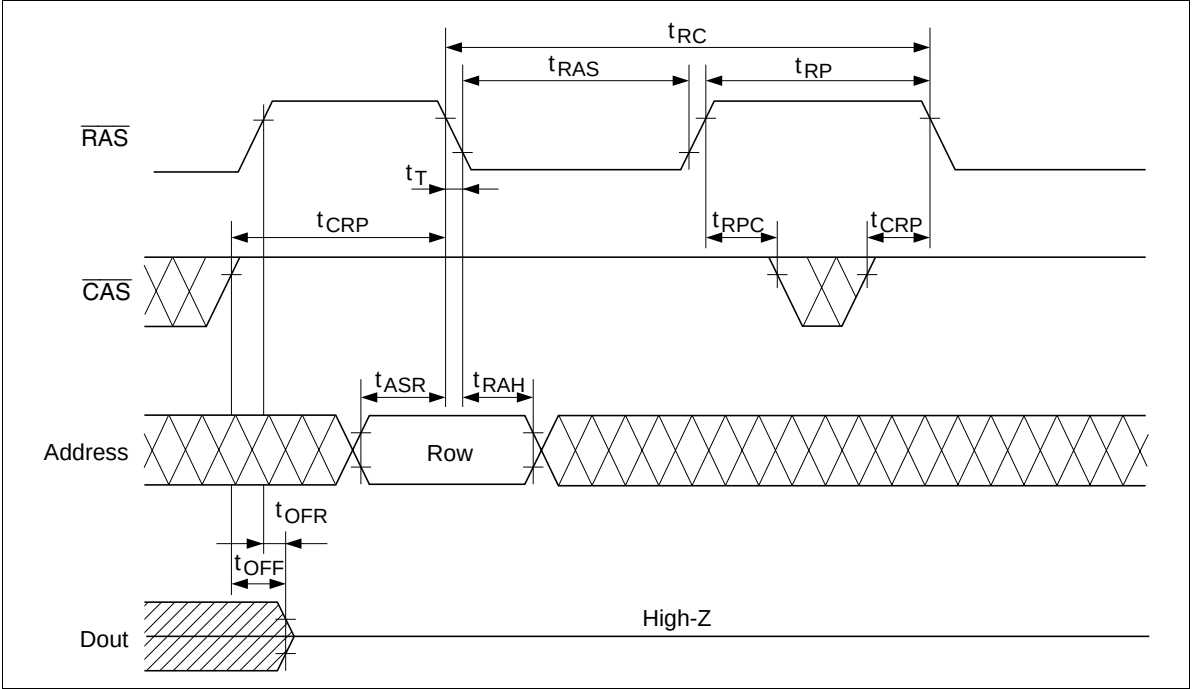
Delayed Write Cycle*18



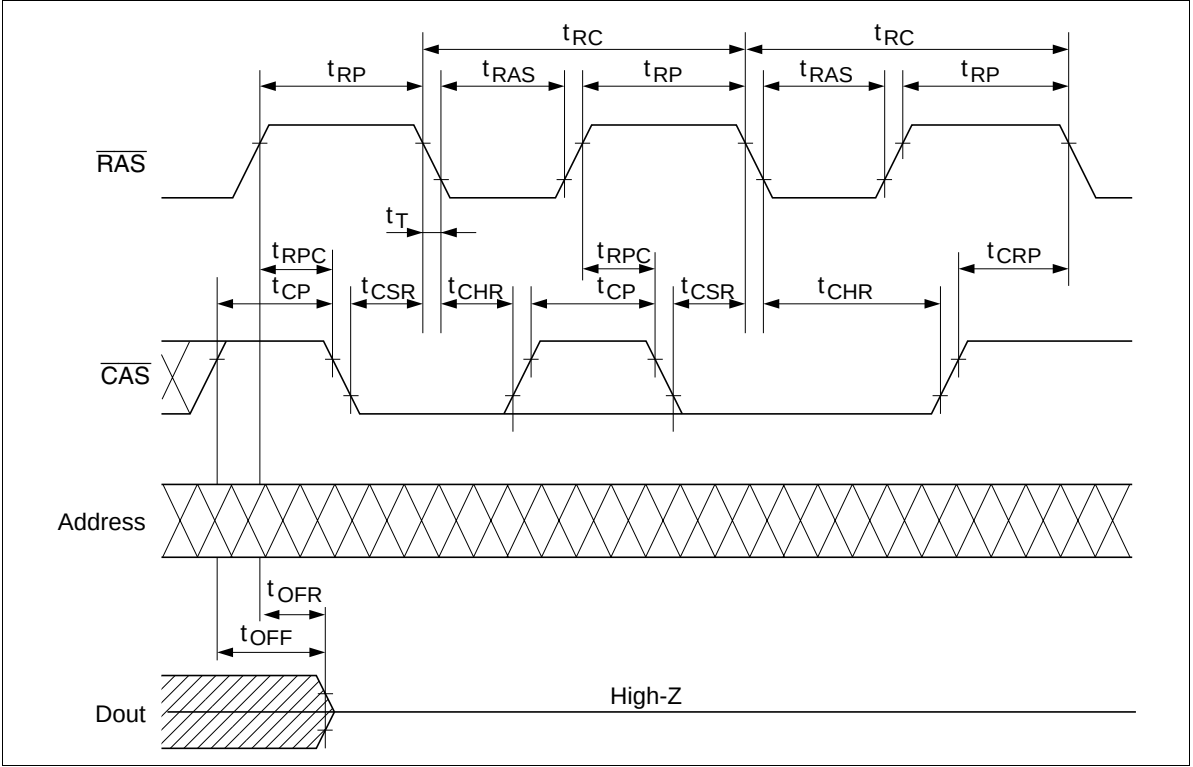
Read-Modify-Write Cycle*18



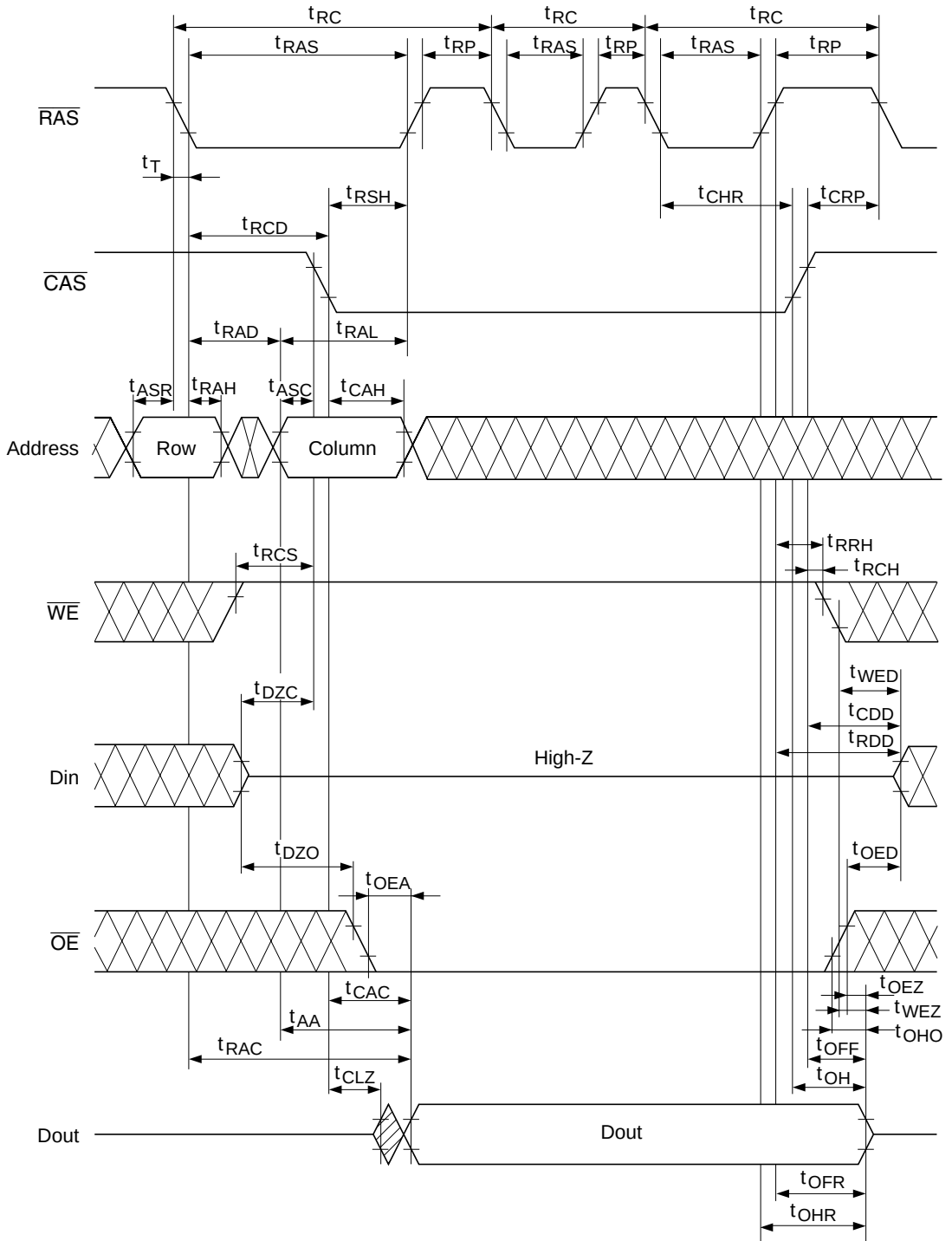
RAS-Only Refresh Cycle



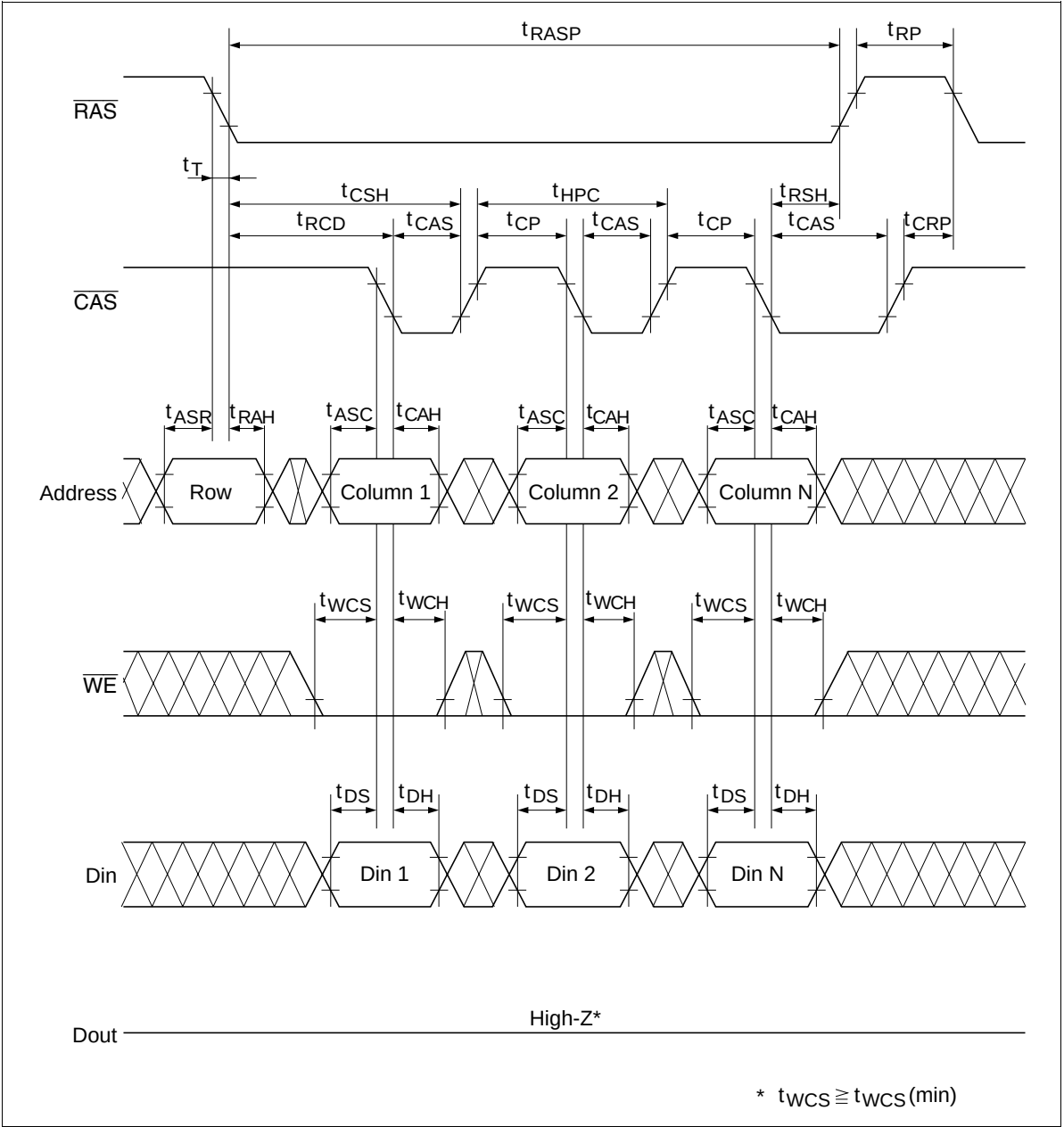
CAS-Before-RAS Refresh Cycle



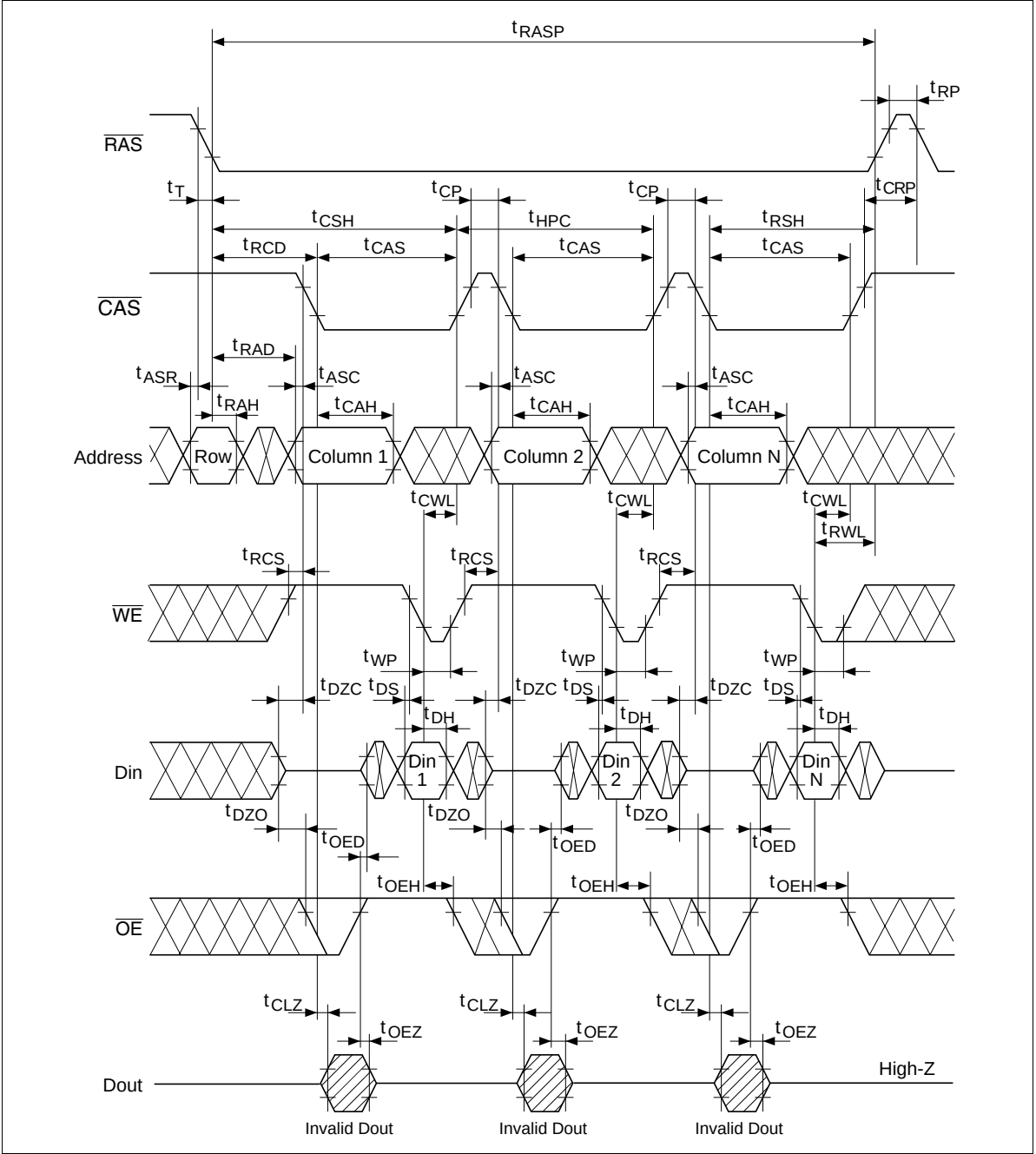
Hidden Refresh Cycle



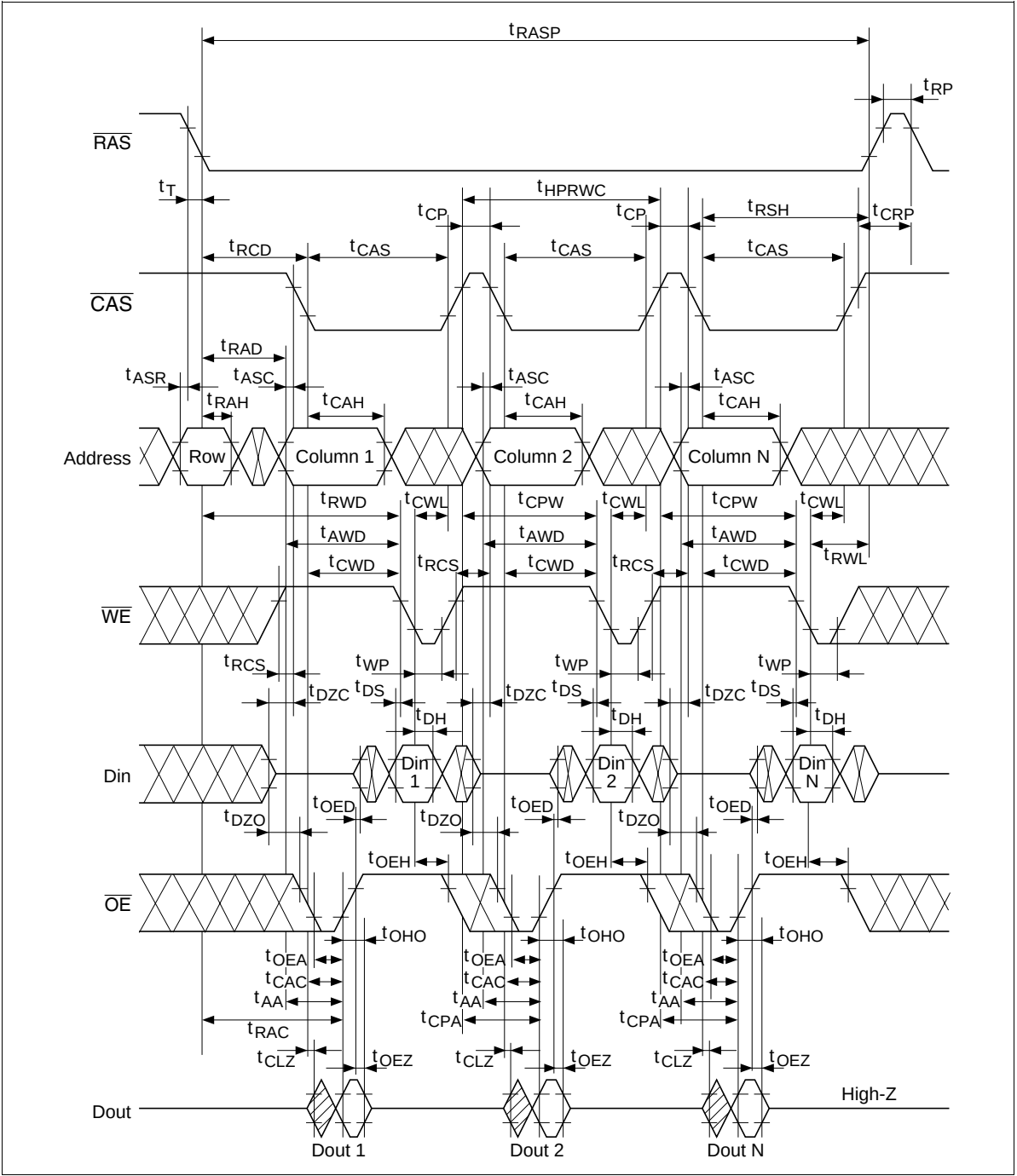
EDO Page Mode Early Write Cycle



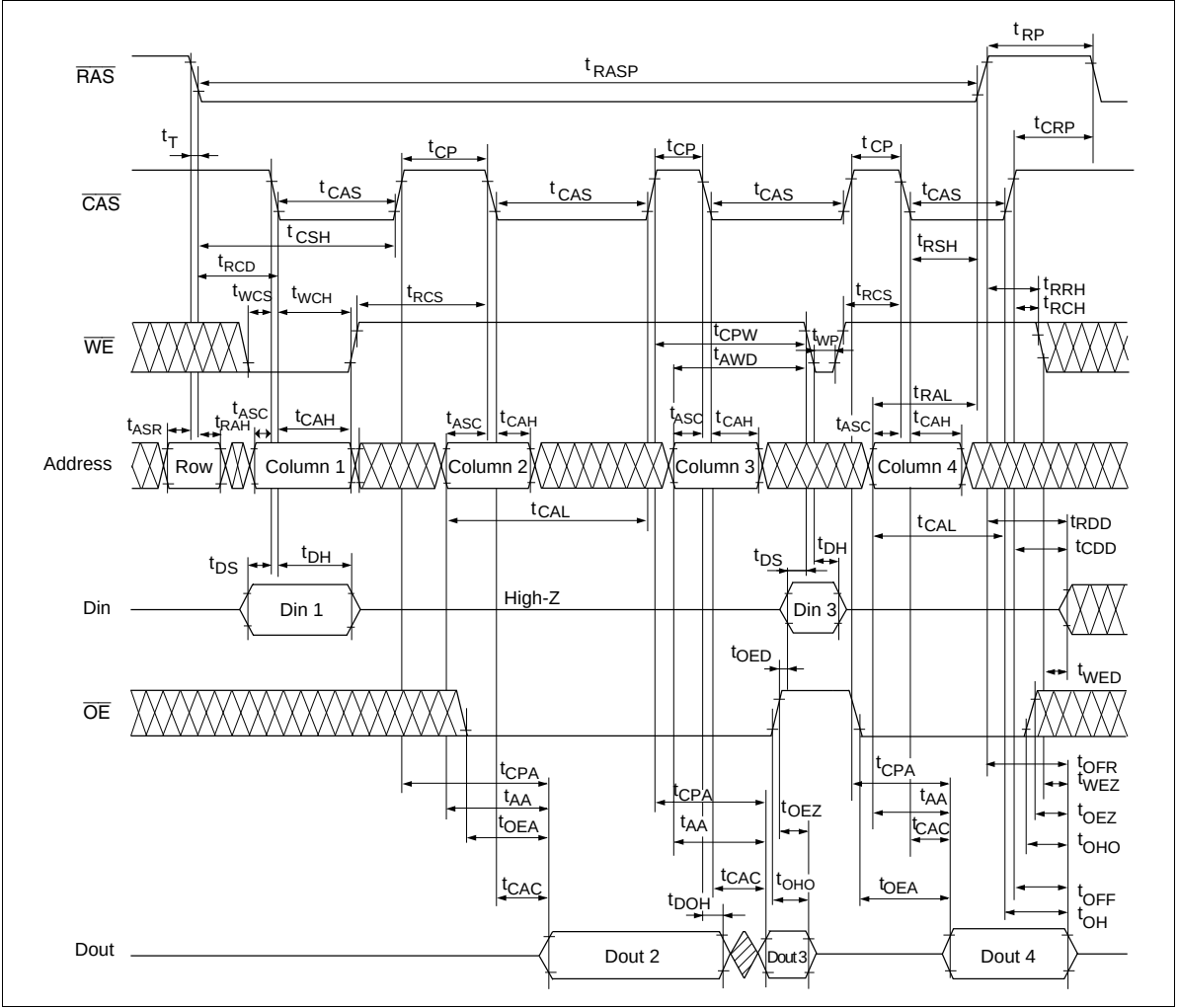
EDO Page Mode Delayed Write Cycle*18



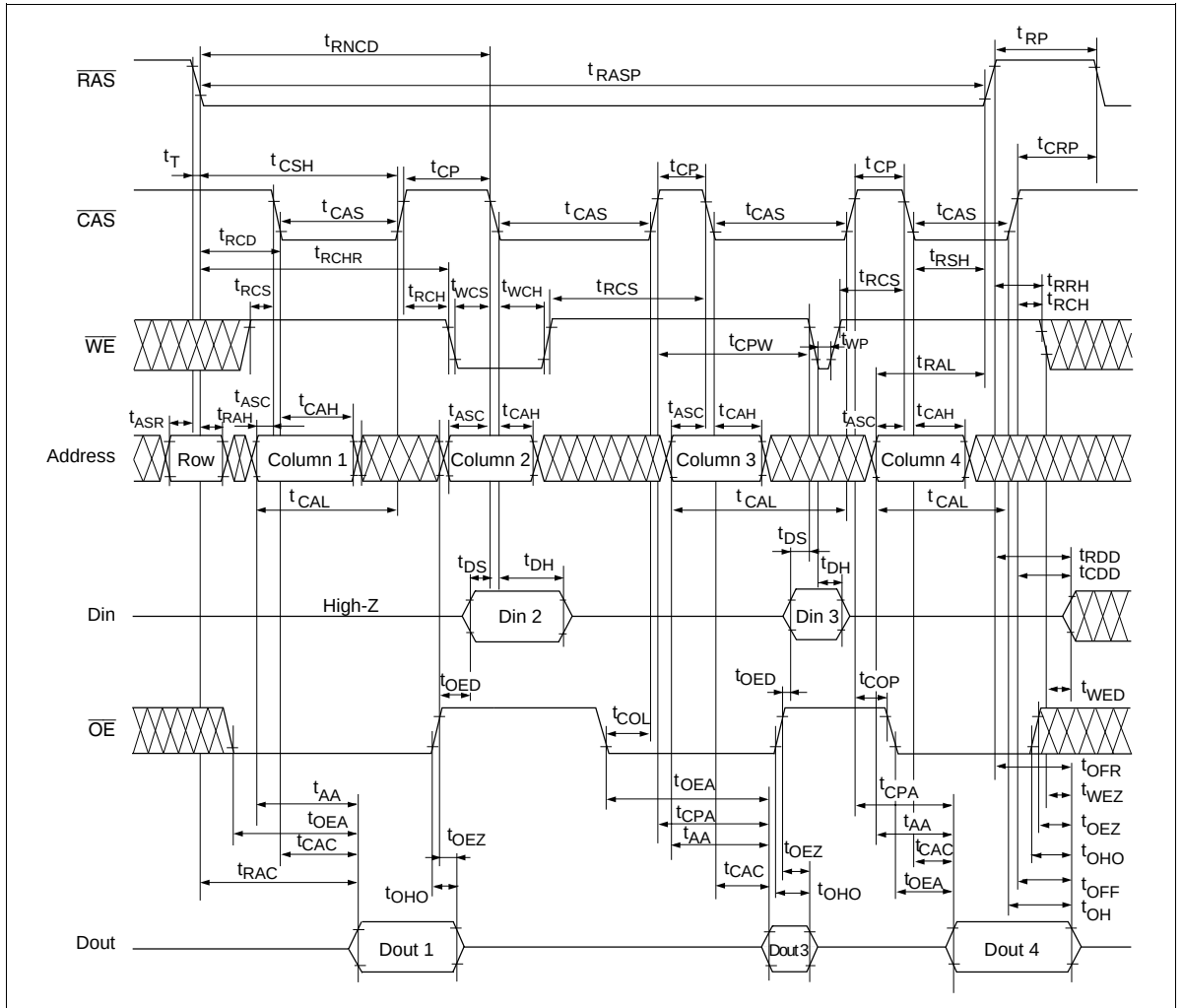
EDO Page Mode Read-Modify-Write Cycle*18



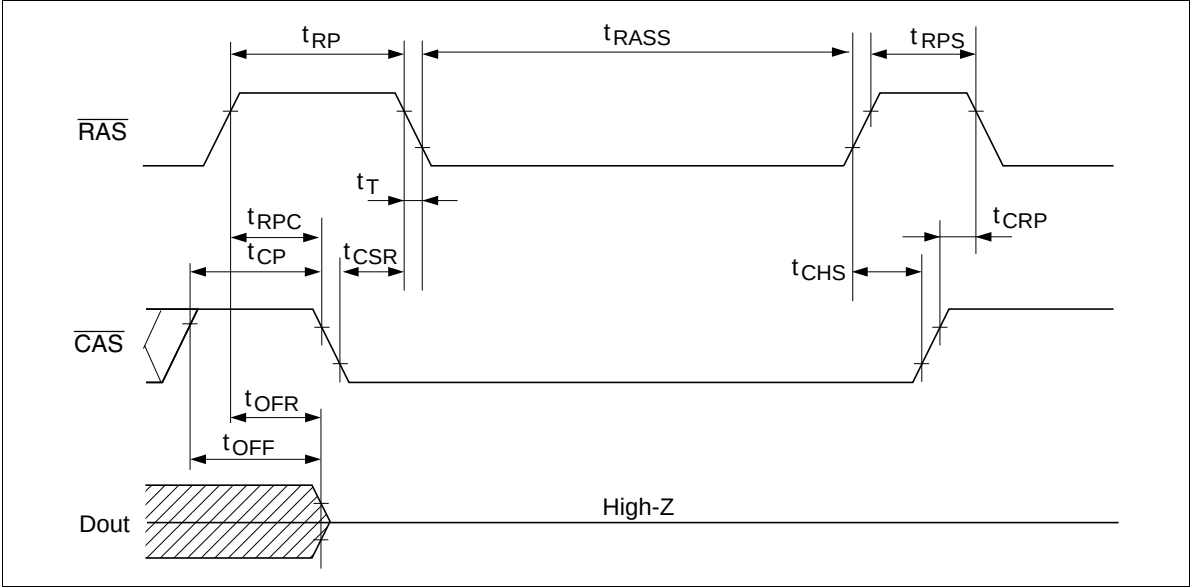
EDO Page Mode Mix Cycle (1)



EDO Page Mode Mix Cycle (2)

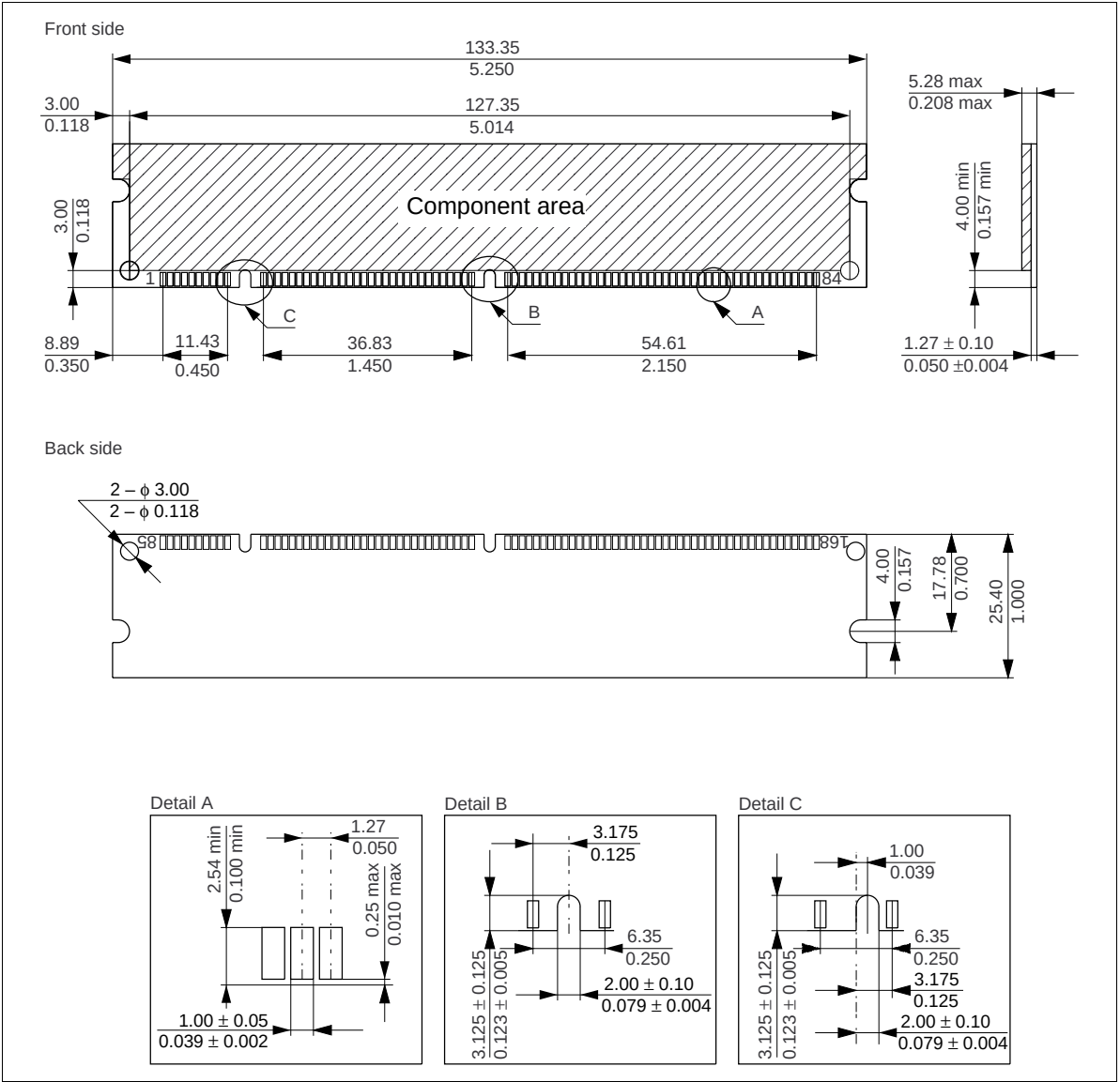


Self Refresh Cycle (L-version)* 23, 24, 25, 26



Physical Outline

Unit: mm/inch



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Dec. 27, 1996	Initial issue		
