HM5216808C Series
HM5216408C Series

1,048,576-word × 8-bit × 2-bank Synchronous Dynamic RAM (SSTL-3)
2,097,152-word × 4-bit × 2-bank Synchronous Dynamic RAM (SSTL-3)

HITACHI

ADE-203-617 (Z)
Preliminary
Rev. 0.0
Jul. 10, 1996

Description

All inputs and outputs are referred to the rising edge of the clock input. The HM5216808C Series, HM5216408C Series are compatible with SSTL-3 (Stub Serires-Terminated Transceiver Logic for 3.3 V) Class II.

Features

- 3.3V Power supply
- Clock frequency: 125 MHz/100 MHz/83 MHz (max)
- SSTL interface
- Single pulsed $\overline{RAS}$
- 2 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 2/4/8
- 2 variations of burst sequence
  - — Sequential (BL = 2/4/8)
  - — Interleave (BL = 2/4/8)
- Programmable $\overline{CAS}$ latency: 2/3
- Refresh cycles: 4096 refresh cycles/64 ms
- 2 variations of refresh
  - — Auto refresh
  - — Self refresh

Preliminary:The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

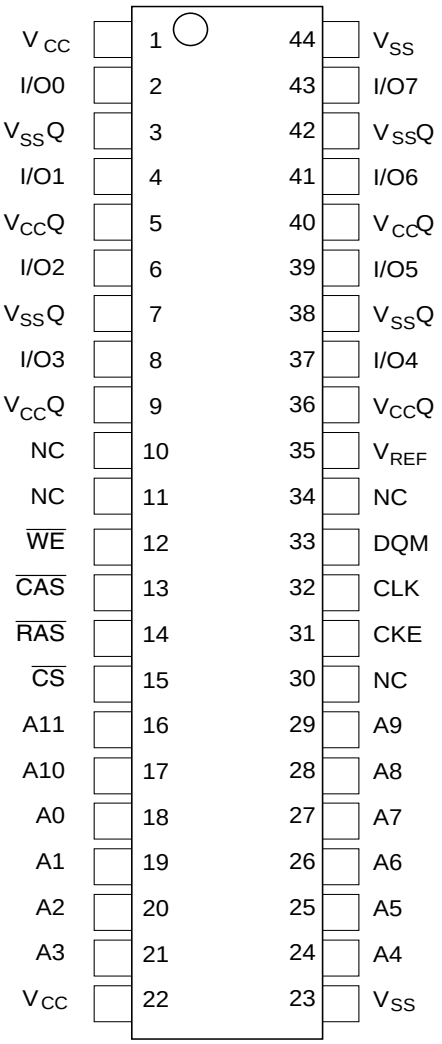
Hitachi semiconductor

Ordering Information

Type No.	Frequency	Package
HM5216808CTT-80 HM5216808CTT-10 HM5216808CTT-12	125 MHz 100 MHz 83 MHz	400-mil 44-pin plasticTSOP II (TTP-44DE)
HM5216408CTT-80 HM5216408CTT-10 HM5216408CTT-12	125 MHz 100 MHz 83 MHz	

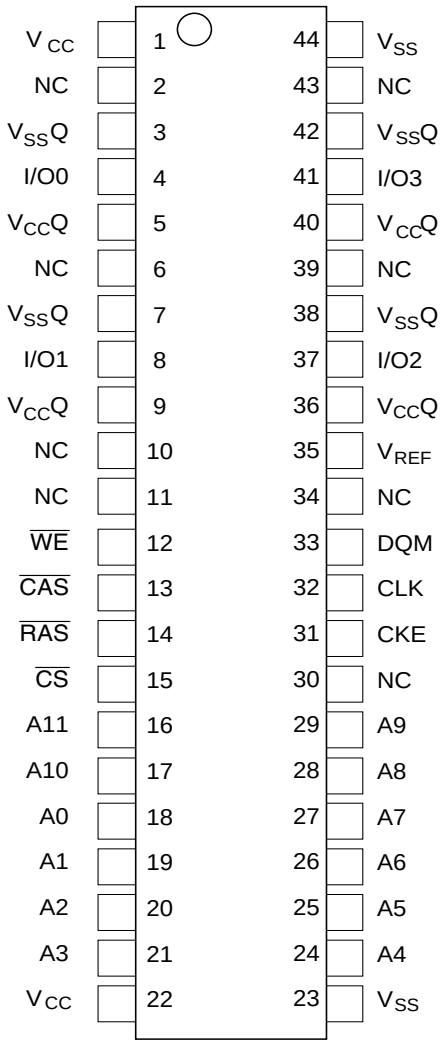
Pin Arrangement

HM5216808CTT Series



(Top view)

HM5216408CTT Series



(Top view)

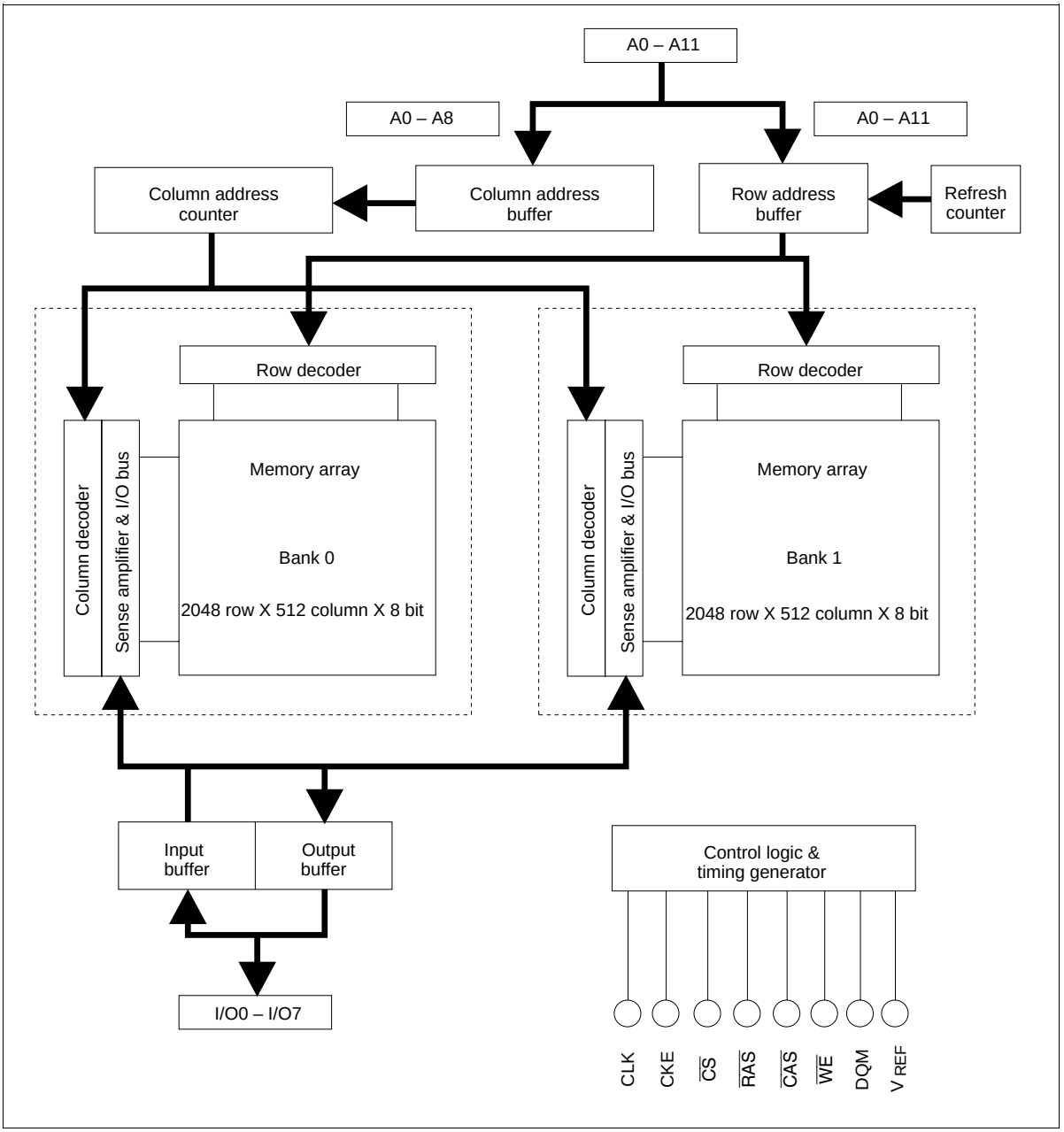
Pin Description (HM5216808C Series)

Pin name	Function
A0 to A11	Address input — Row address A0 to A10 — Column address A0 to A8 — Bank select address A11
I/O0 to I/O7	Data-input/output
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable command
DQM	Input/output mask
CLK	Clock input
CKE	Clock enable
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
$V_{CC}Q$	Power for I/O pin
$V_{SS}Q$	Ground for I/O pin
V_{REF}	Reference voltage
NC	No connection

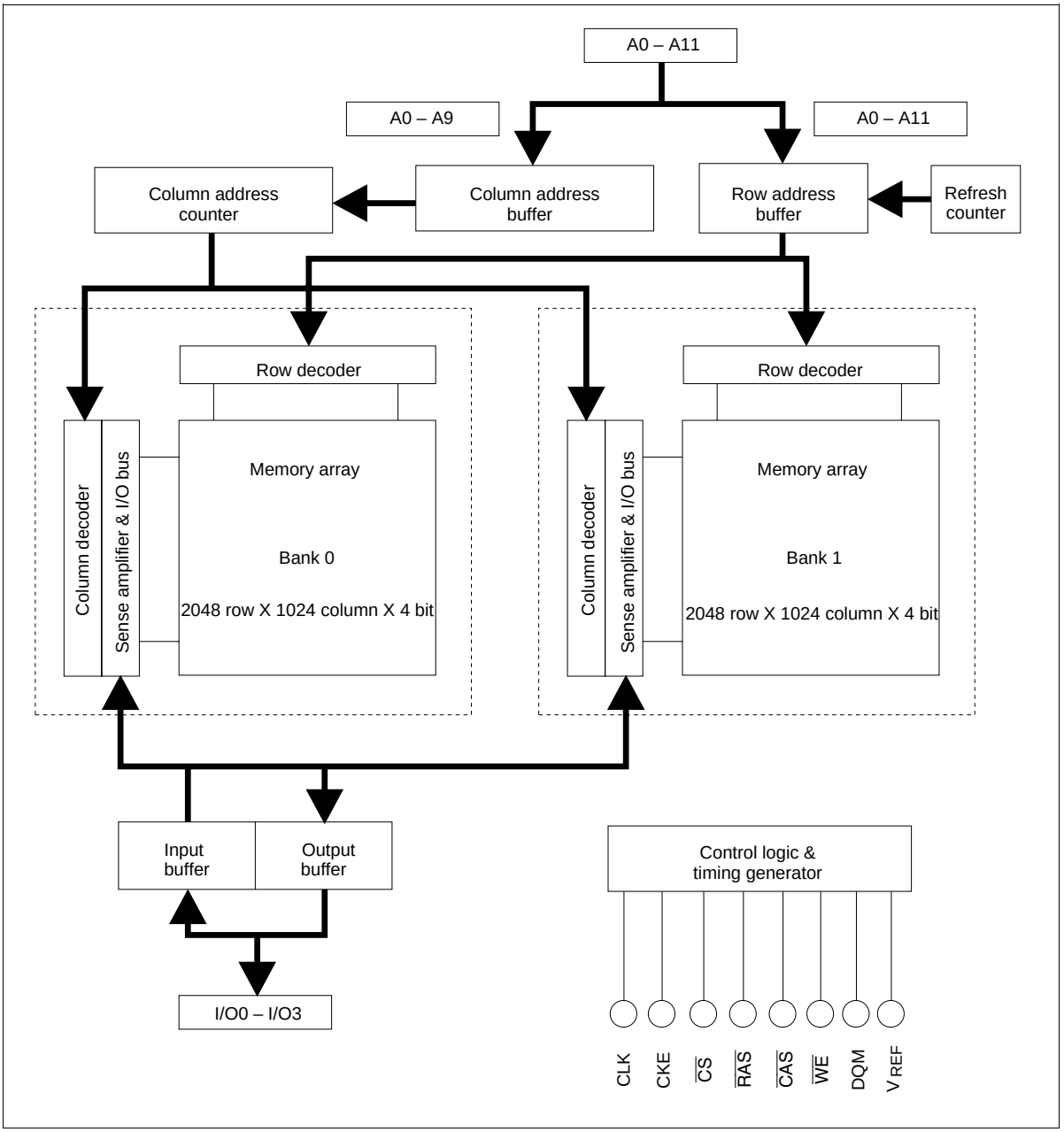
Pin Description (HM5216408C Series)

Pin name	Function
A0 to A11	Address input — Row address A0 to A10 — Column address A0 to A9 — Bank select address A11
I/O0 to I/O3	Data-input/output
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable command
DQM	Input/output mask
CLK	Clock input
CKE	Clock enable
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
$V_{CC}Q$	Power for I/O pin
$V_{SS}Q$	Ground for I/O pin
V_{REF}	Reference voltage
NC	No connection

Block Diagram (HM5216808C Series)



Block Diagram (HM5216408C Series)



Pin Functions

CLK (input pin): CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.

$\overline{CS}$ (input pin): When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A10 (input pins): Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address (AY0 to AY8; HM5216808C Series, AY0 to AY9; HM5216408C Series) is determined by A0 to A8 or A9 (A8; HM5216808C Series, A9; HM5216408C Series) level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11(BS) is precharged.

A11 (input pin): A11 is a bank select signal (BS). The memory array of the HM5216808C Series, the HM5216408C Series is divided into bank 0 and bank 1. HM5216808C Series contain 2048 row × 512 column × 8 bits. HM5216408C Series contain 2048 row × 1024 column × 4 bits. If A11 is Low, bank 0 is selected, and if A11 is High, bank 1 is selected.

CKE (input pin): This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQM (input pins): DQM controls input/output buffers.

Read operation: If DQM is High, the output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z.

Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.

I/O0 to I/O7 (I/O pins): Data is input to and output from these pins. These pins are the same as those of a conventional DRAM.

V_{CC} and $V_{CC}Q$ (power supply pins): 3.3 V is applied. (V_{CC} is for the internal circuit and $V_{CC}Q$ is for the output buffer.)

V_{SS} and $V_{SS}Q$ (power supply pins): Ground is connected. (V_{SS} is for the internal circuit and $V_{SS}Q$ is for the output buffer.)

V_{REF} (input pin): V_{REF} is reference voltage for input buffers.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

		CKE								
Function	**Symbol**	**n – 1**	**n**	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	**A11**	**A10**	**A0 to A9**
Ignore command	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Column address and read command	READ	H	×	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	×	L	H	L	H	V	H	V
Column address and write command	WRIT	H	×	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	×	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge all bank	PALL	H	×	L	L	H	L	×	H	×
Refresh	REF/SELF	H	V	L	L	L	H	×	×	×
Mode register set	MRS	H	×	L	L	L	L	V	V	V

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}. V: Valid address input

Ignore command [DESL]: When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignore command input at the clock. However, the internal status is held.

No operation [NOP]: This command is not an execution command. However, the internal operations continue.

Column address strobe and read command [READ]: This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY8; HM5216808C Series, AY0 to AY9; HM5216408C Series) and the bank select address (BS). After the read operation, the output buffer becomes High-Z.

Read with auto-precharge [READ A]: This command automatically performs a precharge operation after a burst read with a burst length of 2, 4, or 8.

Column address strobe and write command [WRIT]: This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY8; HM5216808C Series, AY0 to AY9; HM5216408C Series) and the bank select address (A11) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to

AY8; HM5216808C Series, AY0 to AY9; HM5216408C Series) and the bank select address (A11).

Write with auto-precharge [WRIT A]: This command automatically performs a precharge operation after a burst write with a length of 2, 4, or 8, or after a single write operation.

Row address strobe and bank activate [ACTV]: This command activates the bank that is selected by A11 (BS) and determines the row address (AX0 to AX10). When A11 is Low, bank 0 is activated. When A11 is High, bank 1 is activated.

Precharge selected bank [PRE]: This command starts precharge operation for the bank selected by A11. If A11 is Low, bank 0 is selected. If A11 is High, bank 1 is selected.

Precharge all banks [PALL]: This command starts a precharge operation for all banks.

R**efresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

Mode register set [MRS]: Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

		CKE		
Function	**Symbol**	**n – 1**	**n**	**DQM**
Write enable/output enable	ENB	H	×	L
Write inhibit/output disable	MASK	H	×	H

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.

The HM5216808C series, HM5216408C Series can mask input/output data by means of DQM. During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.
During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the HM5216808C Series, HM5216408C Series operating instructions.

CKE Truth Table

		CKE						
Current state	**Function**	**n – 1**	**n**	**$\overline{CS}$**	**$\overline{RAS}$**	**$\overline{CAS}$**	**$\overline{WE}$**	**Address**
Active	Clock suspend mode entry	H	L	H	×	×	×	×
Any	Clock suspend	L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit	L	H	×	×	×	×	×
Idle	Auto-refresh command REF	H	H	L	L	L	H	×
Idle	Self-refresh entry SELF	H	L	L	L	L	H	×
Idle	Power down entry	H	L	L	H	H	H	×
		H	L	H	×	×	×	×
Self refresh	Self refresh exit SELFX	L	H	L	H	H	H	×
		L	H	H	×	×	×	×
Power down	Power down exi	L	H	L	H	H	H	×
		L	H	H	×	×	×	×

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.

Clock suspend mode entry: The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

ACTIVE clock suspend: This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

READ suspend and READ A suspend: The data being output is held (and continues to be output).

WRITE suspend and WRIT A suspend: In this mode, external signals are not accepted. However, the internal state is held.

Clock suspend: During clock suspend mode, keep the CKL to Low.

Clock suspend mode exit: The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

IDLE: In this state, all banks are not selected, and completed precharge operation.

Self-refresh entry [SELF]: When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

Power down mode entry: When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

Self-refresh exit: When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

Power down exit: When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	×	×	×	×	DESL	Enter IDLE after t_{RP}
	L	H	H	H	×	NOP	Enter IDLE after t_{RP}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*[3]
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*[3]
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*[3]
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*[3]
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and Precharge*[2]
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh (auto-refresh)	H	×	×	×	×	DESL	Enter IDLE after t_{RC}
	L	H	H	H	×	NOP	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of t_{RWL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOP]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge.

From [IDLE]

To [DESL], [NOP], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

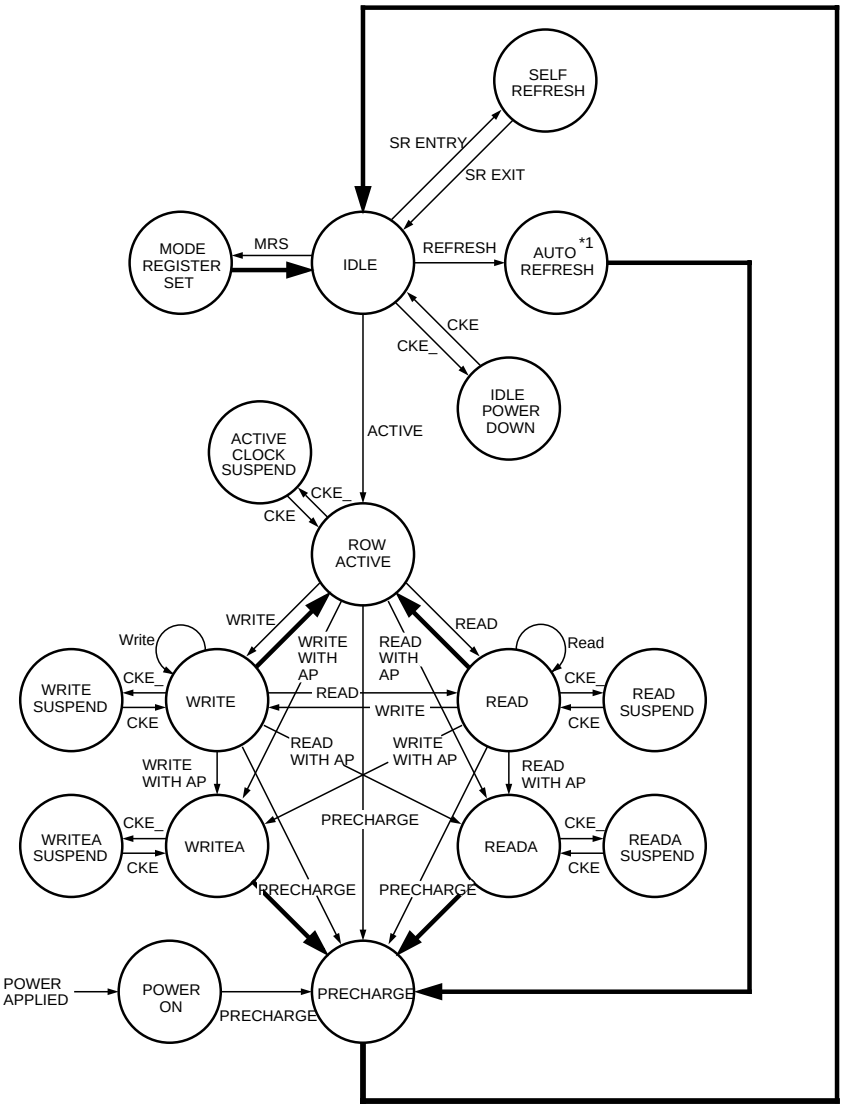
To [DESL], [NOP]: These commands continue write operations until the burst is completed, and the synchronous DRAM enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the IDLE state.

Simplified State Diagram



Automatic transition after completion of command.
Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operaaation is performed automatically and enter the IDLE state.

Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A11) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

A11, A10, A9, A8 (OPCODE): The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

Burst read and BURST WRITE: Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

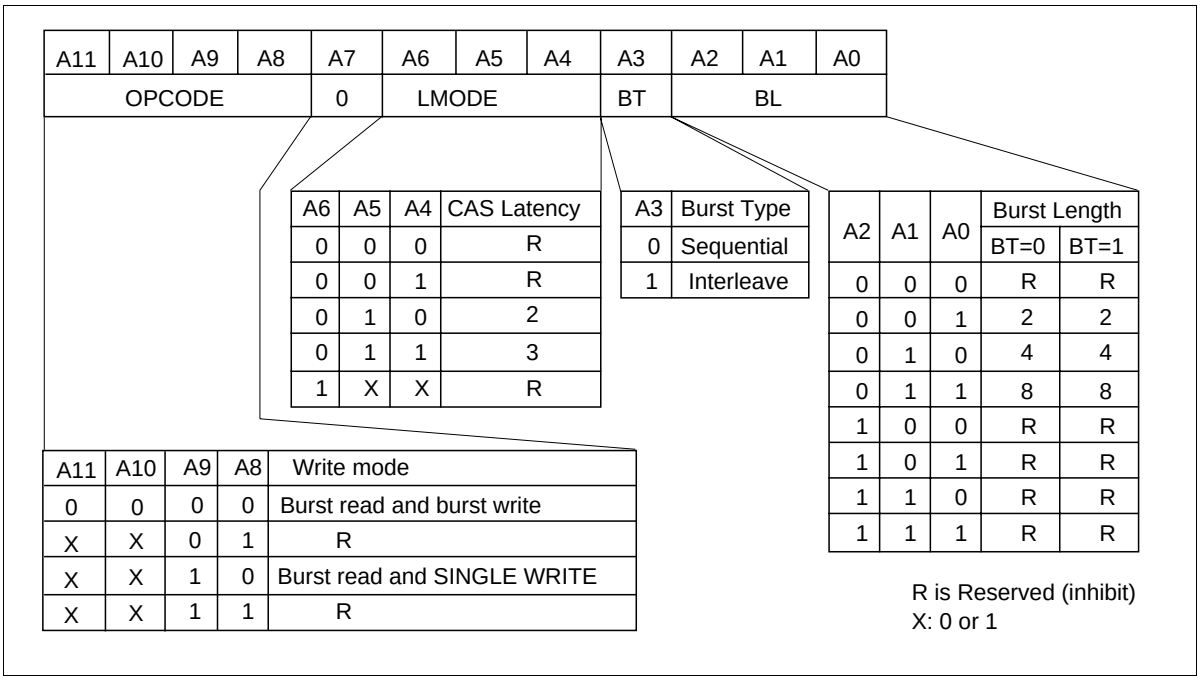
Burst read and SINGLE WRITE: Data is only written to the column address specified during the write cycle, regardless of the burst length.

A7: Keep this bit Low at the mode register set cycle.

A6, A5, A4 (LMODE): These pins specify the $\overline{\text{CAS}}$ latency.

A3 (BT): A burst type is specified.

A2, A1, A0 (BL): These pins specify the burst length.



A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE				0	LMODE			BT	BL		

A6	A5	A4	CAS Latency
0	0	0	R
0	0	1	R
0	1	0	2
0	1	1	3
1	X	X	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	0	R	R
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	R	R

A11	A10	A9	A8	Write mode
0	0	0	0	Burst read and burst write
X	X	0	1	R
X	X	1	0	Burst read and SINGLE WRITE
X	X	1	1	R

R is Reserved (inhibit)
X: 0 or 1

Burst Sequence

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

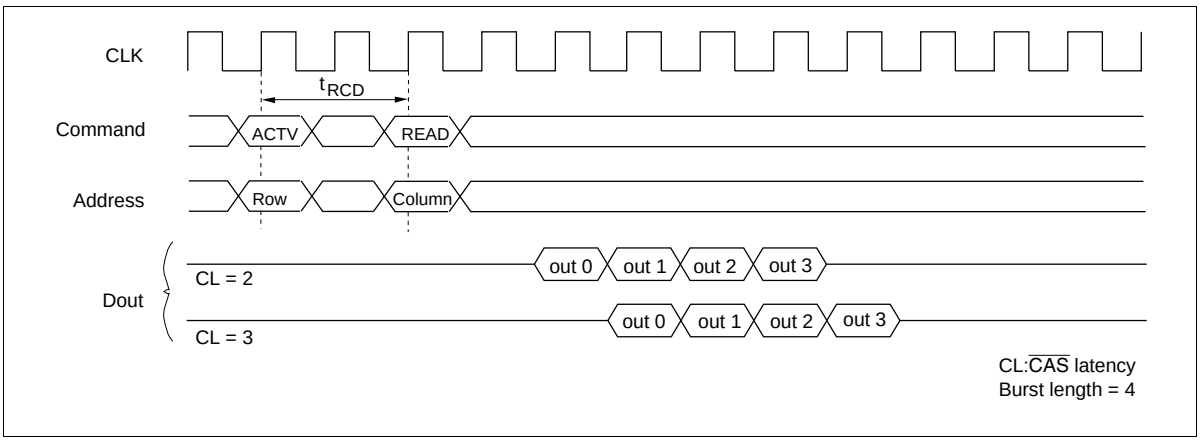
Operation of HM5216808C Series, HM5216408C Series

Read/Write Operations

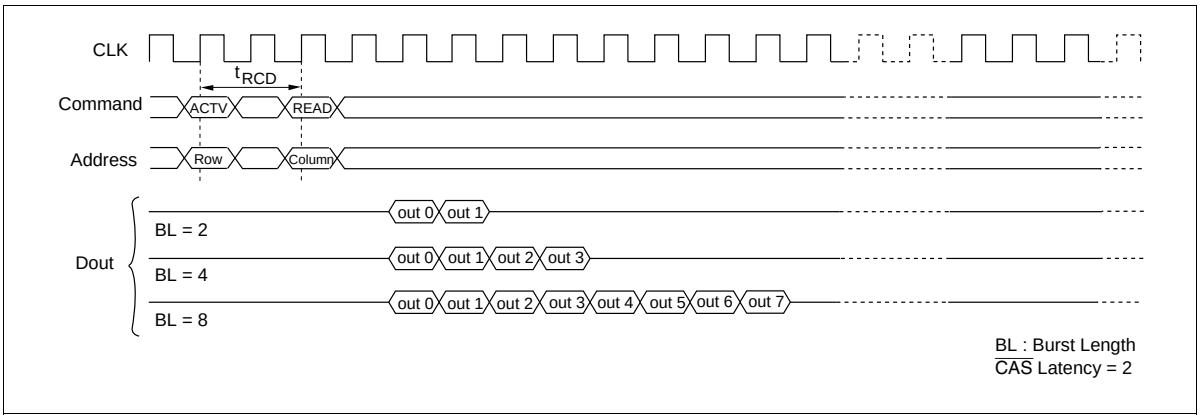
Bank active: Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Either bank 0 or bank 1 is activated according to the status of the A11 pin, and the row address (AX0 to AX10) is activated by the A0 to A10 pins at the bank active command cycle. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

Read operation: A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CAS}$ Latency - 1) cycle after read command set. HM5216808C series, HM5216408C series can perform a burst read operation. The burst length can be set to 2, 4 or 8. The start address for a burst read is specified by the column address (AY0 to AY8; HM5216808C Series, AY0 to AY9; HM5216408C Series) and the bank select address (A11) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the $\overline{CAS}$ Latency. The $\overline{CAS}$ Latency can be set to 2 or 3. When the burst length is 2, 4, or 8, the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output. The $\overline{CAS}$ latency and burst length must be specified at the mode register.

$\overline{CAS}$ Latency

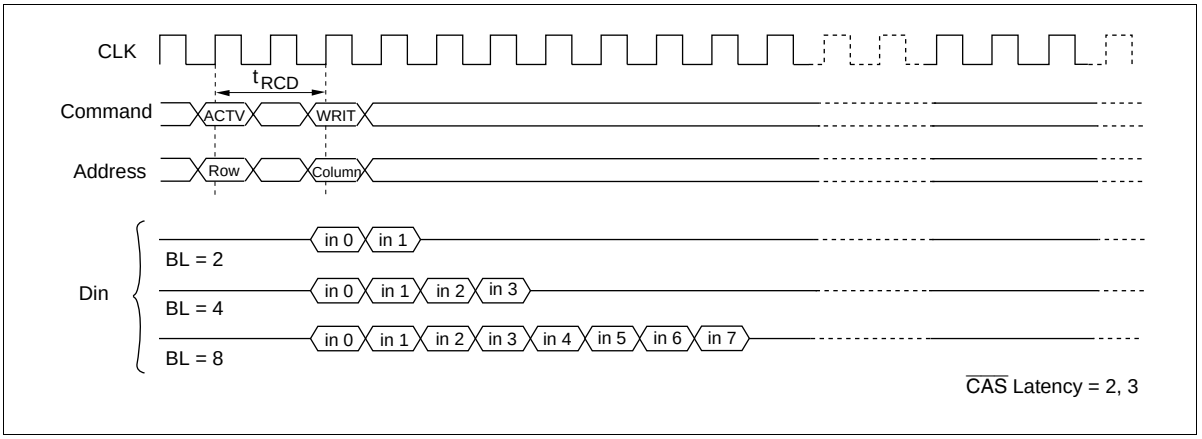


Burst Length

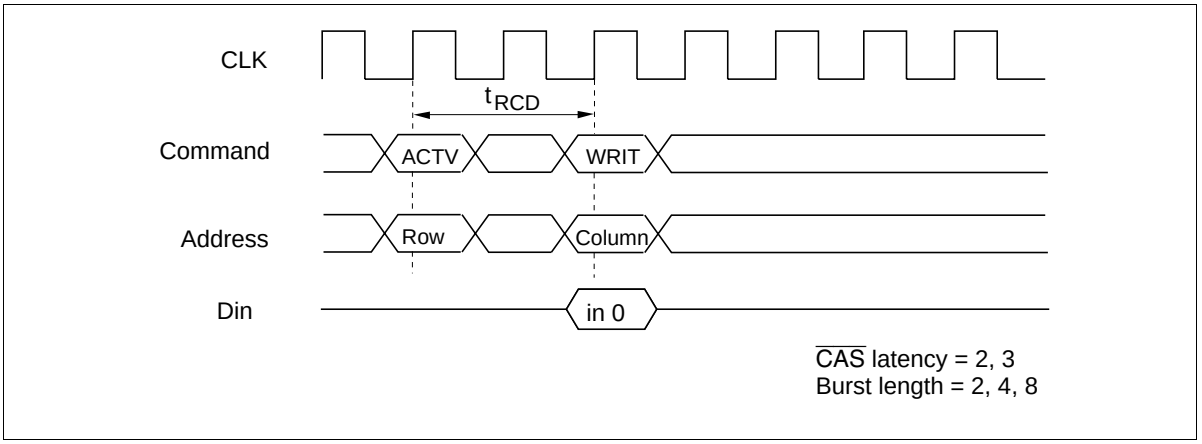


Write operation: Burst write or single write mode is selected by the OPCODE (A11, A10, A9, A8) of the mode register.

Burst write: A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 2, 4 or 8, like burst read operations. The write start address is specified by the column address (AY0 to AY8; HM5216808C Series, AY0 to AY9; HM5216408C Series) and the bank select address (A9) at the write command set cycle.



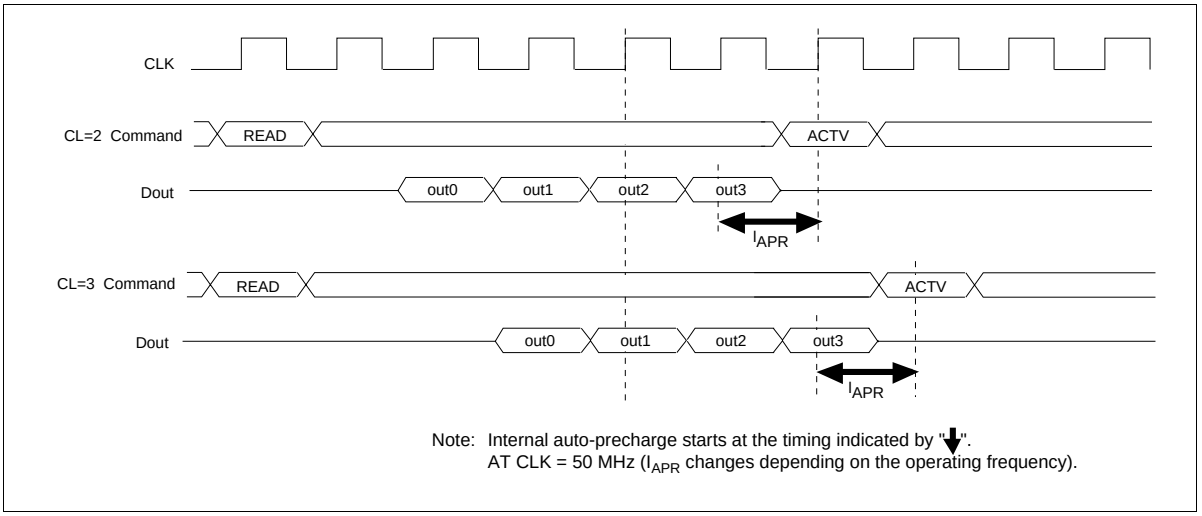
Single write: A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address (AY0 to AY8; HM5216808C Series, AY0 to AY9; HM5216408C Series) and the bank select address (A11) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0).



Auto-precharge

Read with auto-precharge: In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by l_{APR} is required before execution of the next command.

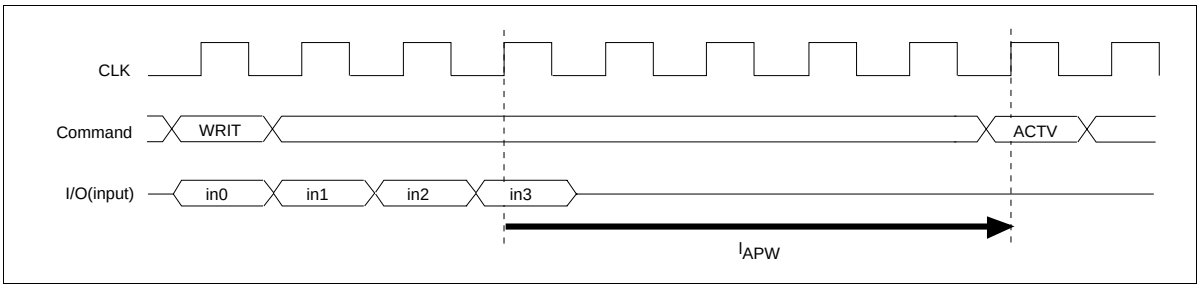
CAS latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output



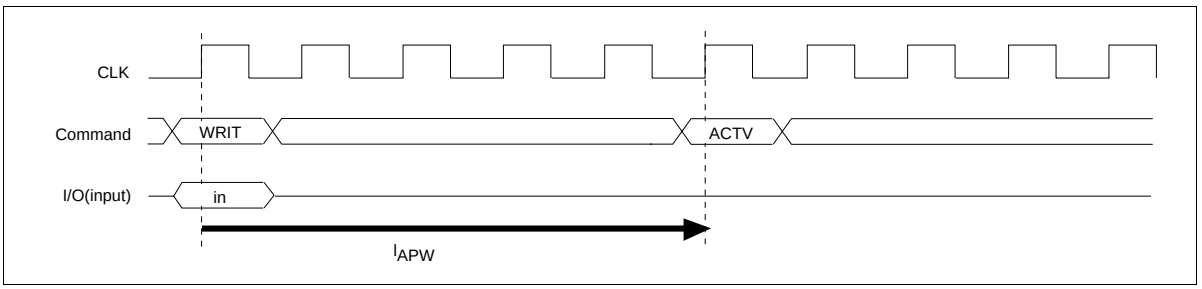
Note: Internal auto-precharge starts at the timing indicated by "↓".
AT CLK = 50 MHz (I_{APR} changes depending on the operating frequency).

Write with auto-precharge: In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of l_{APW} is required between the final valid data input and input of the next command.

Burst Write (Burst Length = 4)



Single Write

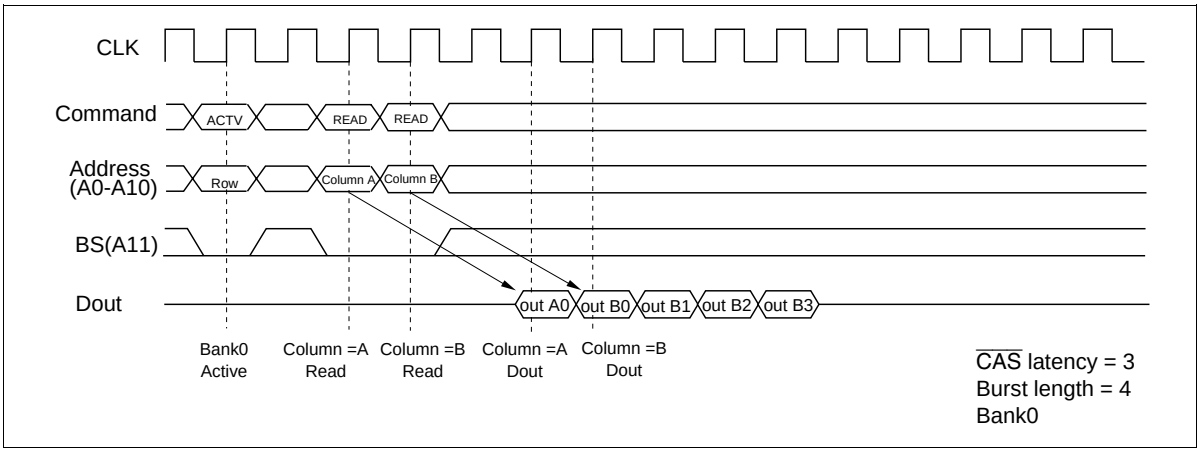


Command Intervals

Read command to Read command interval

Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

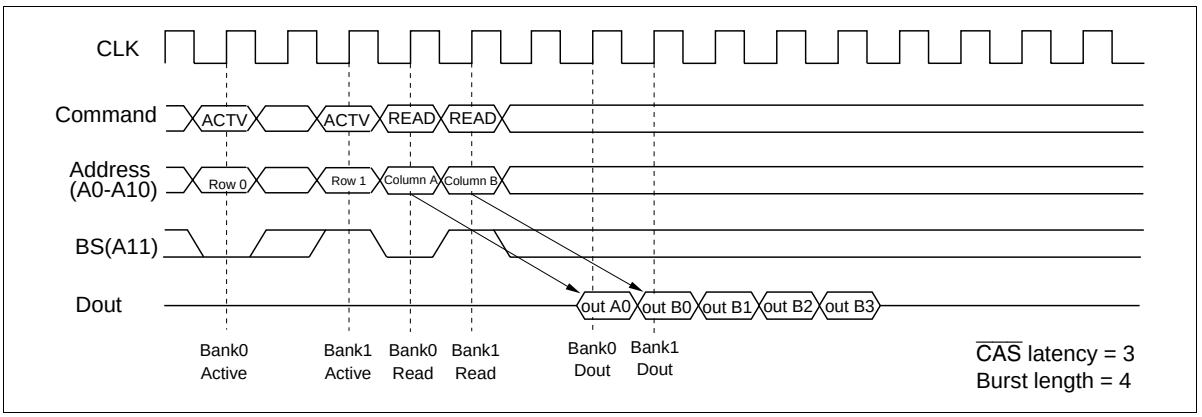
READ to READ Command Interval (same ROW address in same bank)



Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

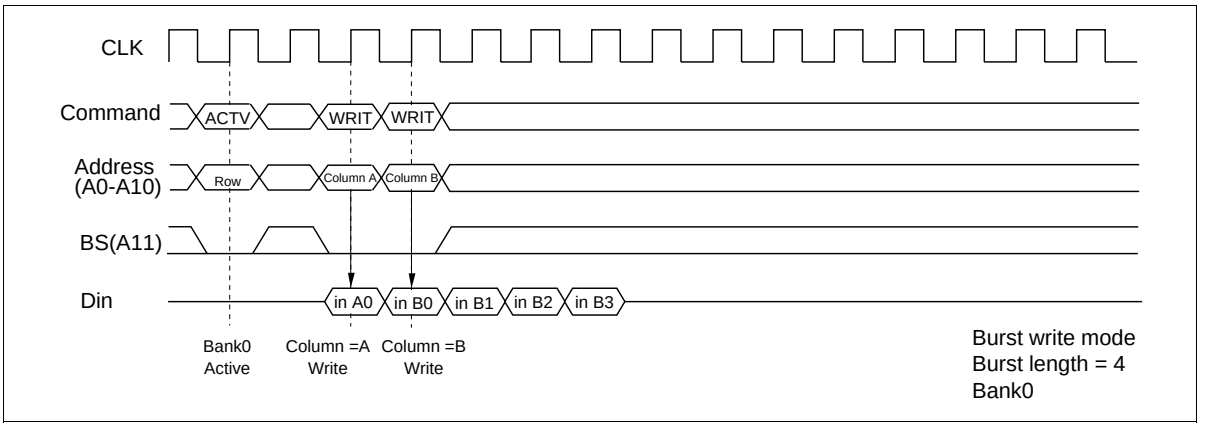
READ to READ Command Interval (different bank)



Write command to Write command interval

Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle. In the case of burst writes, the second write command has priority.

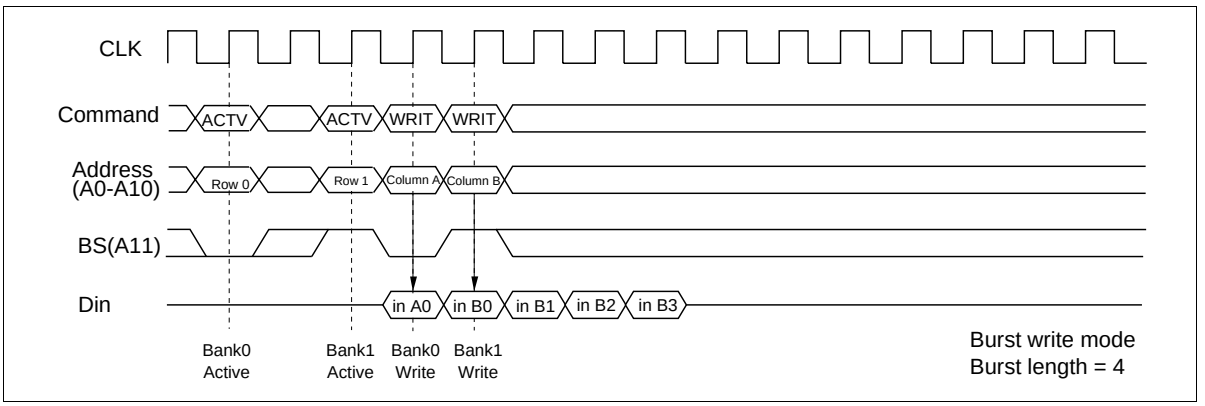
WRITE to WRITE Command Interval (same ROW address in same bank)



Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

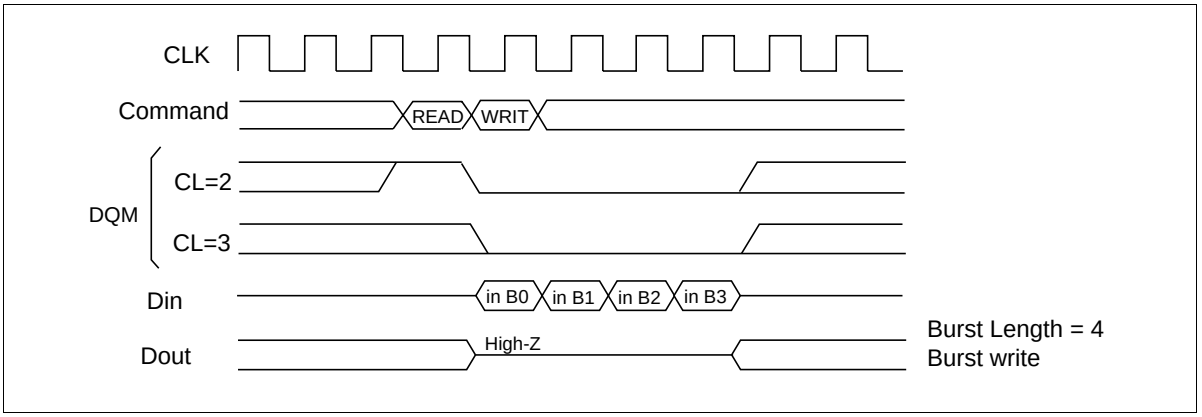
WRITE to WRITE Command Interval (different bank)



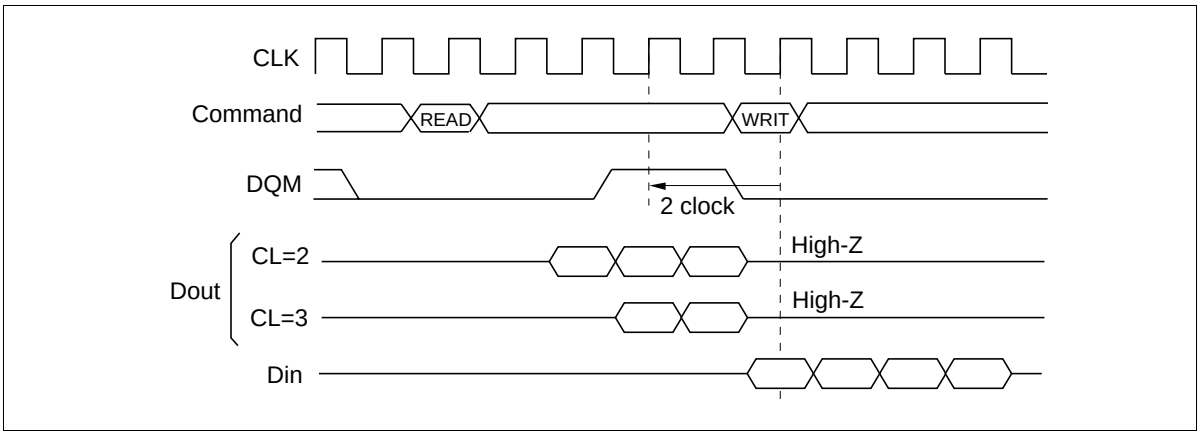
Read command to Write command interval

Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 cycle. However, DQM must be set High so that the output buffer becomes High-Z before data input.

READ to WRITE Command Interval-1



READ to WRITE Command Interval-2



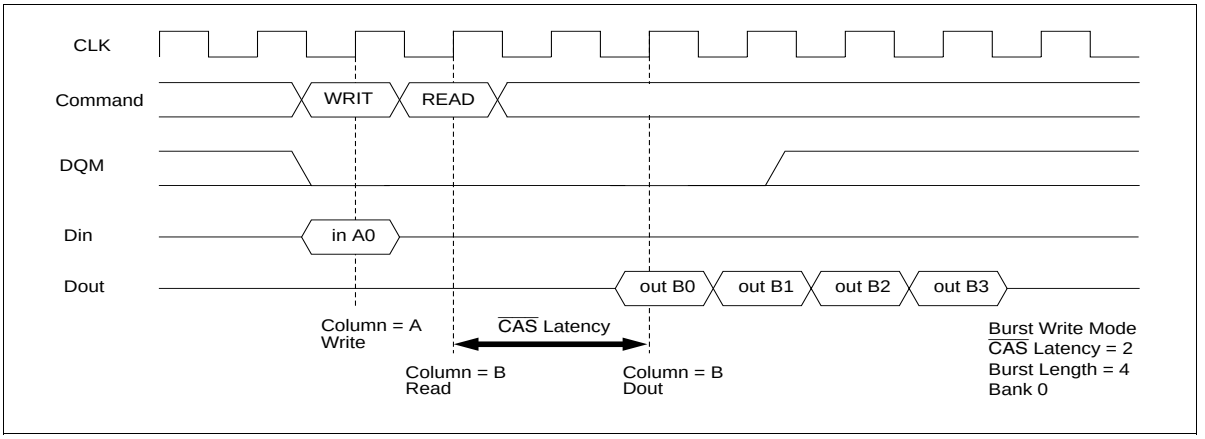
Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command or a bank-active command.

Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQM must be set High so that the output buffer becomes High-Z before data input.

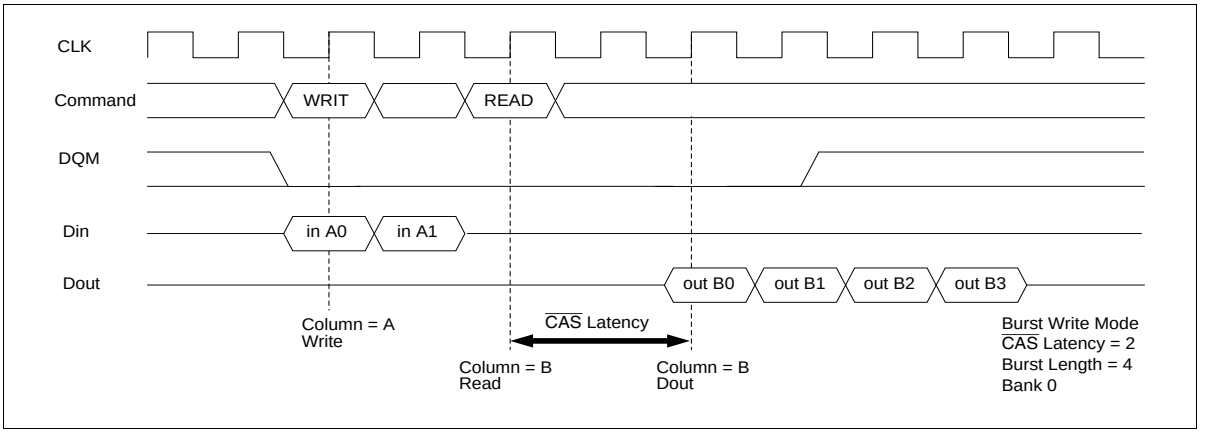
Write command to Read command interval

Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 cycle. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval-1



WRITE to READ Command Interval-2



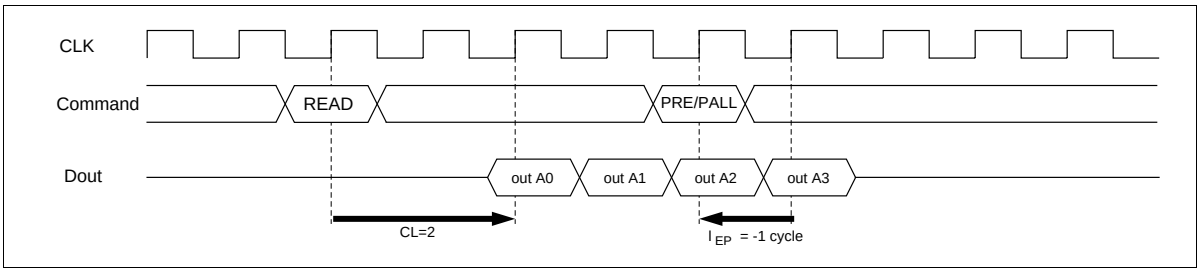
Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed (as in the case of the same bank and the same address). Read command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z

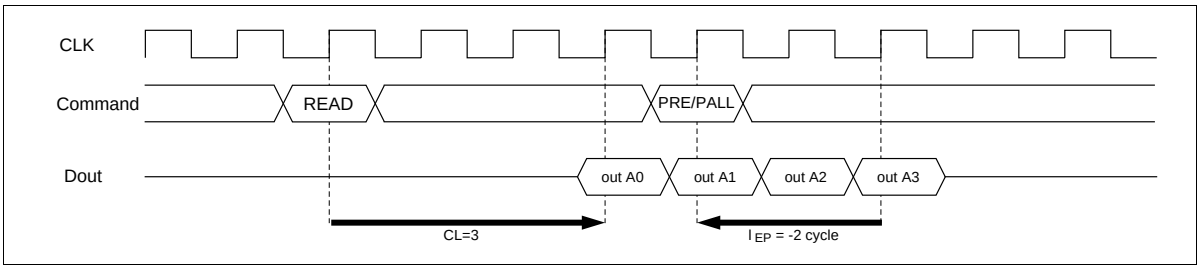
after the cycles defined by l_{HZP}, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the cycles defined by l_{EP} must be assured as an interval from the final data output to precharge command execution.

READ to PRECHARGE Command Interval (same bank): To output all data

$\overline{CAS}$ Latency = 2, Burst Length = 4

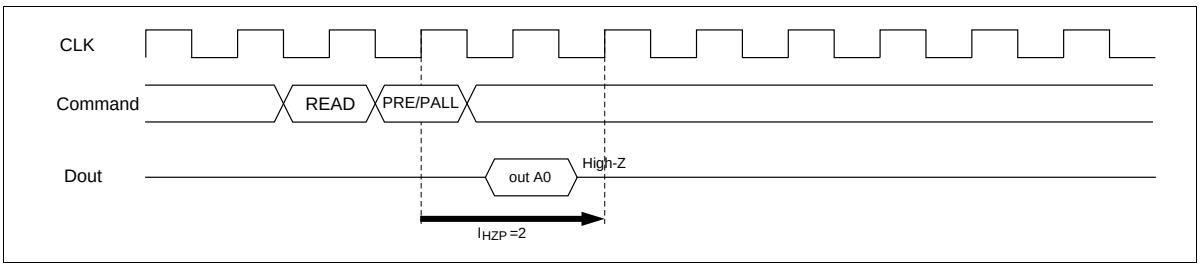


$\overline{CAS}$ Latency = 3, Burst Length = 4

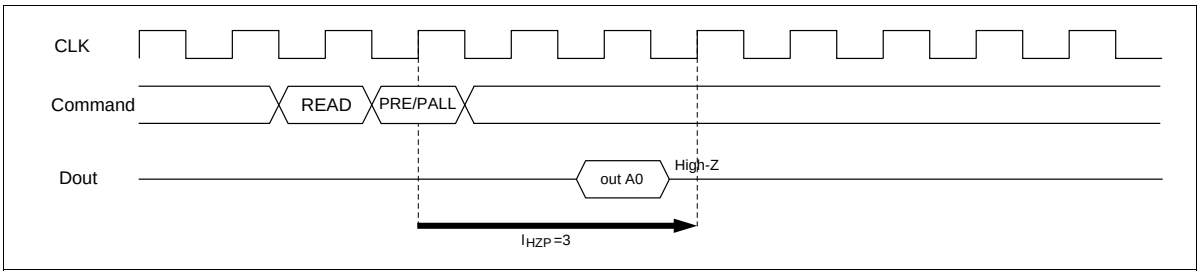


READ to PRECHARGE Command Interval (same bank): To stop output data

$\overline{CAS}$ Latency = 2, Burst Length = 2, 4, 8



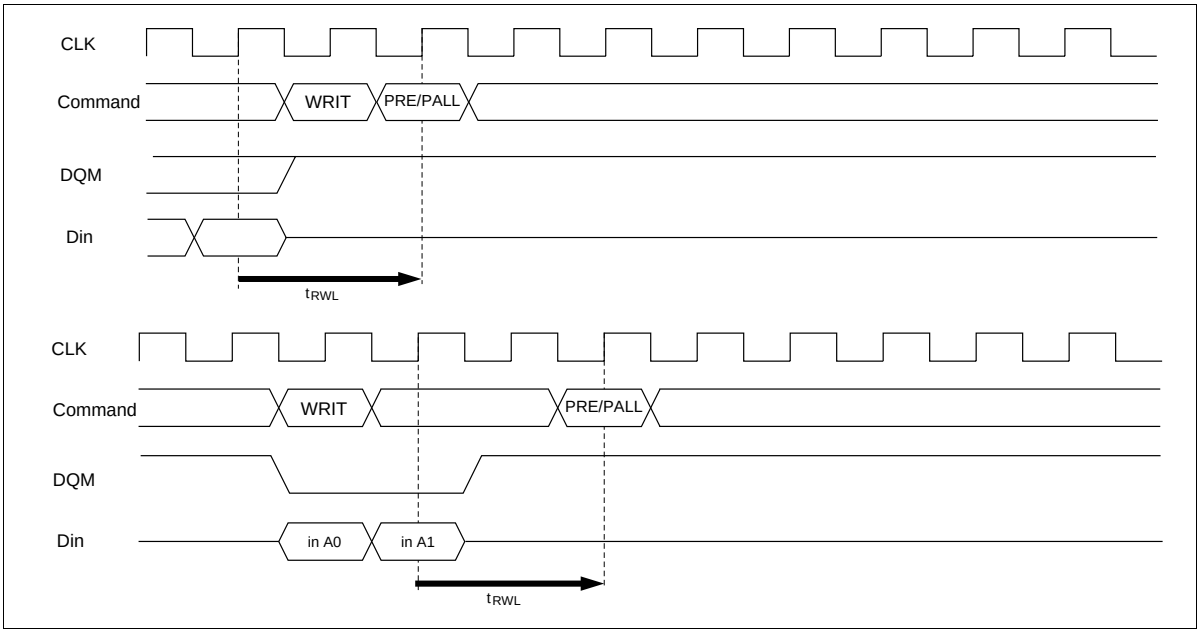
$\overline{\text{CAS}}$ Latency = 3, Burst Length = 2, 4, 8



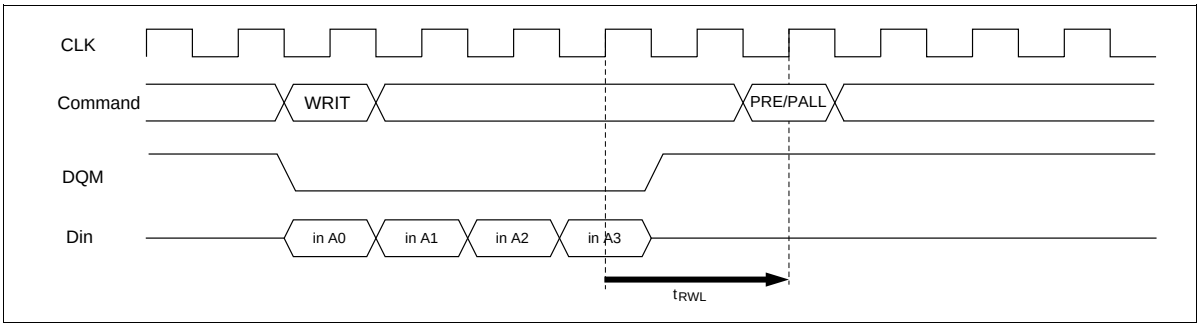
Write command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle. However, if the burst write operation is unfinished, the input data must be masked by means of DQM for assurance of the cycle defined by t_{RWL}.

WRITE to PRECHARGE Command Interval (same bank)

Burst Length = 4 (To stop write operation)



Burst Length = 4 (To write all data)

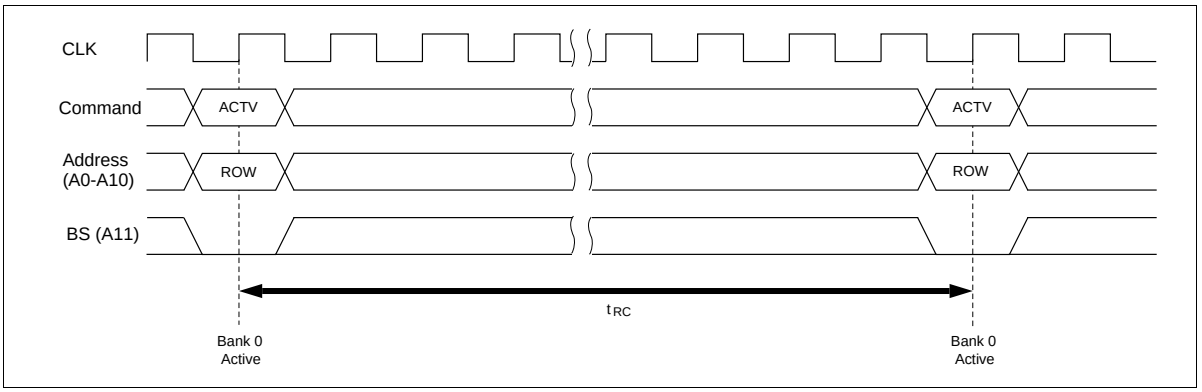


Bank active command interval

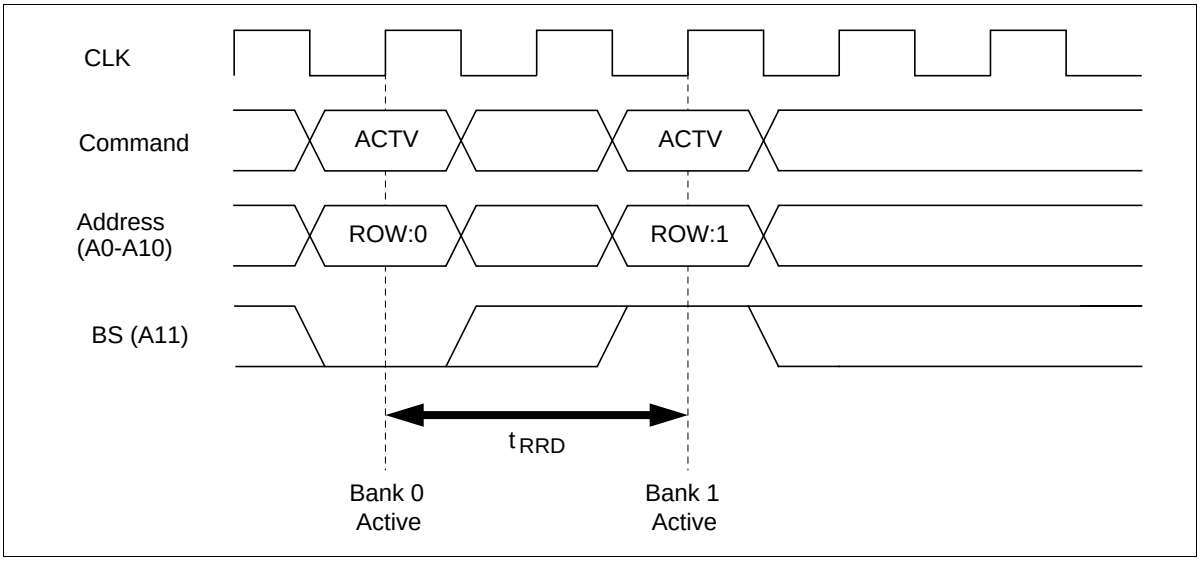
Same bank: The interval between the two bank-active commands must be no less than t_{RC}.

In the case of different bank-active commands: The interval between the two bank-active commands must be no less than t_{RRD}.

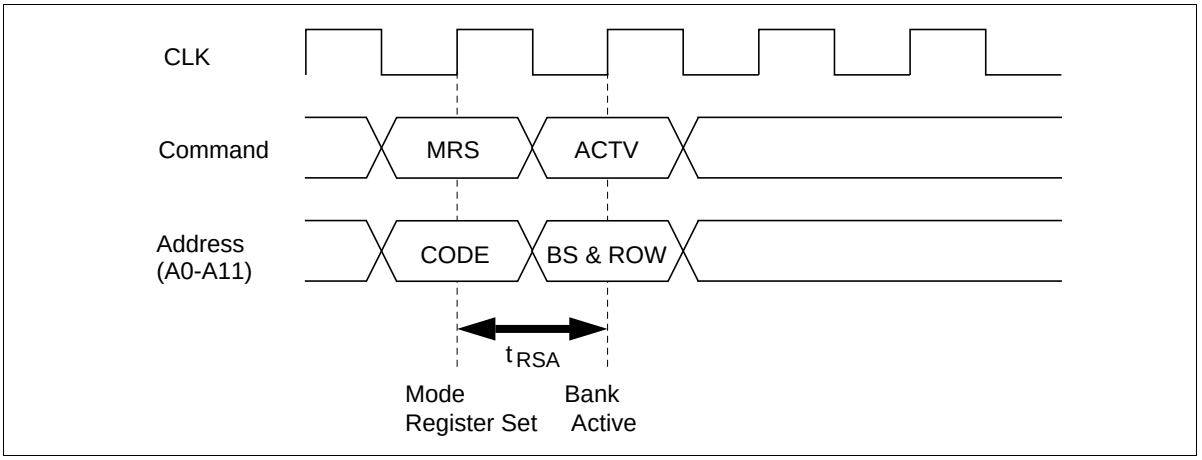
Bank active to bank active for same bank



Bank active to bank active for different bank



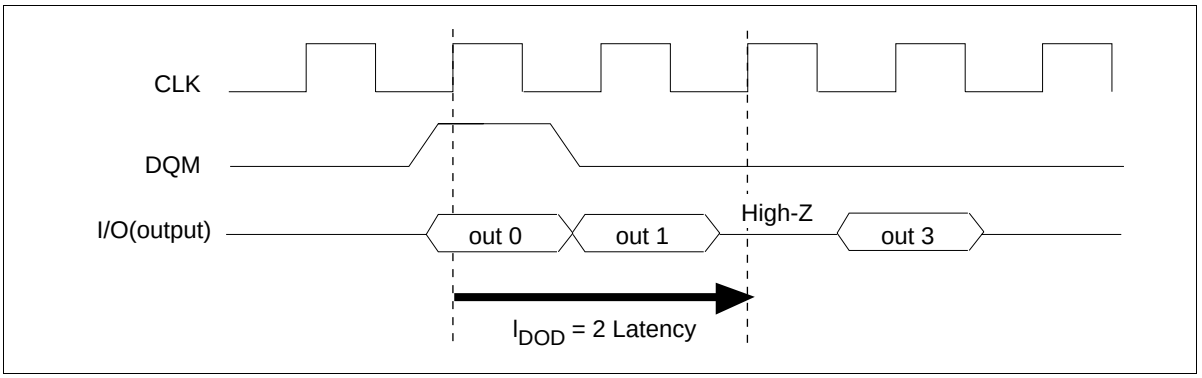
Mode register set to Bank-active command interval: The interval between setting the mode register and executing a bank-active command must be no less than t_{RSA}.



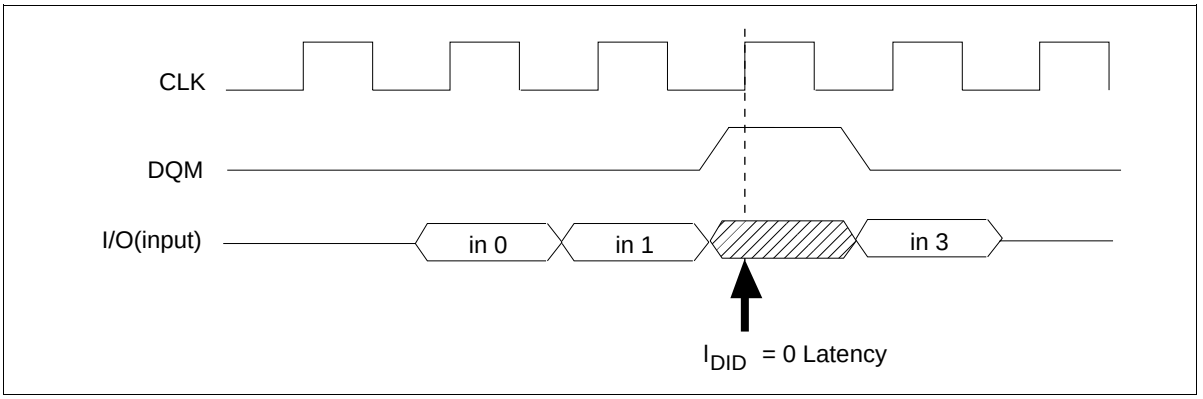
DQM Control

The DQM mask the lower and upper bytes of the I/O data, respectively. The timing of DQM is different during reading and writing.

Reading: When data is read, the output buffer can be controlled by DQM.
By setting DQM to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQM during reading is 2.



Writing: Input data can be masked by DQM. By setting DQM to Low, data can be written. In addition, when DQM is set to High, the corresponding data is not written, and the previous data is held. The latency of DQM during writing is 0.



Refresh

Auto-refresh: All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the interval counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 4,096 cycles/64 ms. (4,096 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh: After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. After the self-refresh, since it is impossible to determine the address of the last ROW to be refreshed, an auto-refresh should immediately be performed for all addresses (4,096 cycles).

Others

Power-down mode: The synchronous DRAM enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the synchronous DRAM exits from the power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

Clock suspend mode: By driving CKE to Low during a bank-active or read/write operation, the synchronous DRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the synchronous DRAM terminates clock suspend mode, and command input is enabled from the next cycle. For details, refer to the "CKE Truth Table".

Power-up sequence: During power-up sequence, the DQM and the CKE must be set to High. When 200 µs has past after power on, all banks must be precharged using the precharge command. After t_{RP} delay, set 8 or more auto refresh commands. And set the mode register set command to initialize the mode register.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}, $V_{CC}Q$	3.0	3.3	3.6	V	1
	V_{SS}, $V_{SS}Q$	0	0	0	V	
Input reference voltage	V_{REF}	1.3	1.5	1.7	V	
Termination voltage	V_{TT}	V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V	
DC input high voltage	V_{IH} (dc)	V_{REF} + 0.2	—	4.6	V	1, 2
DC input low voltage	V_{IL} (dc)	–0.3	—	V_{REF} – 0.2	V	1, 3

Notes: 1. All voltage referred to V_{SS}
2. V_{IH} (max) = 5.5 V for pulse width ≤ 5 ns
3. V_{IL} (min) = –1.5 V for pulse width ≤ 5 ns

DC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

		HM5216808C/HM5216408C								
		-80		-10		-12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	150	—	130	—	115	mA	t_{RC} = min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	—	8	—	8	—	8	mA	CKE = V_{IL}, t_{CK} = min	5
		—	4	—	4	—	4	mA	CKE = V_{IL} CLK = V_{IL} or V_{IH} Fixed	6
		—	75	—	70	—	65	mA	CKE = V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	10	—	10	—	10	mA	CKE = V_{IL}, t_{CK} = min, I/O = High-Z	1, 2
		—	80	—	75	—	70	mA	CKE = V_{IH}, NOP command t_{CK} = min, I/O = High-Z	1, 2, 3
Burst operating current ($\overline{CAS}$ latency=2)	I_{CC4}	—	140	—	130	—	115	mA	t_{CK} = min BL = 4	1, 2, 4
($\overline{CAS}$ latency=3)	I_{CC4}	—	190	—	180	—	155	mA		
Refresh current	I_{CC5}	—	120	—	115	—	100	mA	t_{RC} = min	
Self refresh current	I_{CC6}	—	4	—	4	—	4	mA	$V_{IH} \geq V_{CC} - 0.2$ $V_{IL} \leq 0.2$ V	7
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	$0 \leq Vout \leq V_{CC}$ I/O = disable	
Output high voltage	V_{OH}	V_{TT}+0.8	—	V_{TT}+0.8	—	V_{TT}+0.8	—	V	I_{OH} = –16 mA	
Output low voltage	V_{OL}	—	V_{TT}–0.8	—	V_{TT}–0.8	—	V_{TT}–0.8	V	I_{OL} = 16 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per one CLK cycle.
5. After power down mode set, CLK operating current.
6. After power down mode set, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	2	—	4	pF	1, 3
Input capacitance (Signals)	C_{I2}	2	—	4	pF	1, 3
Output capacitance (I/O)	C_O	4	—	6	pF	1, 2, 3

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

		HM5216808C/HM5216408C							
		-80		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
System clock cycle time ($\overline{CAS}$ latency = 2)	t_{CK}	12	—	15	—	18	—	ns	1
($\overline{CAS}$ latency = 3)	t_{CK}	8	—	10	—	12	—		
CLK high pulse width	t_{CKH}	2.5	—	3	—	4	—	ns	1
CLK low pulse width	t_{CKL}	2.5	—	3	—	4	—	ns	1
Access time from CLK ($\overline{CAS}$ latency = 2)	t_{AC}	—	10	—	9	—	10	ns	1, 2
($\overline{CAS}$ latency = 3)	t_{AC}	—	6	—	7	—	9		
Data-out hold time	t_{OH}	2	—	2	—	2	—	ns	1, 2
CLK to Data-out low impedance	t_{LZ}	2	—	2	—	2	—	ns	1, 2, 3
CLK to Data-out high impedance	t_{HZ}	—	6	—	7	—	9	ns	1, 4
Data-in setup time	t_{DS}	2	—	2	—	3	—	ns	1
Data in hold time	t_{DH}	1	—	1	—	1	—	ns	1
Address setup time	t_{AS}	2	—	2	—	3	—	ns	1
Address hold time	t_{AH}	1	—	1	—	1	—	ns	1
CKE setup time	t_{CES}	2	—	2	—	3	—	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	—	2	—	3	—	ns	1
CKE hold time	t_{CEH}	1	—	1	—	1	—	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	—	2	—	3	—	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	—	1	—	1	—	ns	1

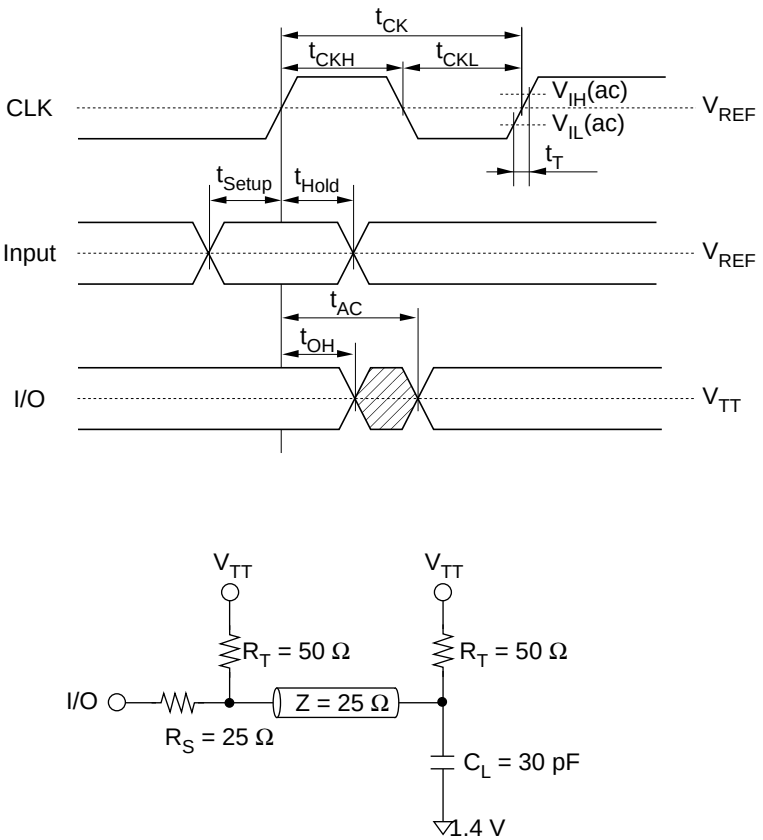
AC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V) (cont)

		HM5216808C/HM5216408C							
		-80		-10		-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Ref/Active to Ref/Active command period	t_{RC}	80	—	90	—	100	—	ns	1
Active to Precharge command period	t_{RAS}	56	120000	60	120000	70	120000	ns	1
Active to precharge on full page mode	t_{RASC}	—	120000	—	120000	—	120000	ns	1
Active command to column command (same bank)	t_{RCD}	24	—	30	—	30	—	ns	1
Precharge to active command period	t_{RP}	24	—	30	—	30	—	ns	1
The last data-in to Precharge lead time	t_{RWL}	12	—	15	—	15	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	16	—	20	—	20	—	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	—	64	—	64	—	64	ms	

Notes: 1. AC measurement assumes $t_T = [V_{IH} (ac) – V_{IL} (ac)]/SLEW$ ns. Reference level for timing of input signals is V_{REF}.
2. Access time is measured at V_{TT}. Load condition is C_L = 30 pF with terminated output load.
3. t_{LZ} (max) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} defines CKE setup time to CKE rising edge except power down exit command.

Test Conditions

Parameter	Symbol	Value	Unit
Input reference voltage	V_{REF}	$V_{CC}Q \times 0.45$	V
Termination voltage	V_{TT}	V_{REF}	V
AC input high voltage	V_{IH} (ac)	V_{REF} + 0.4	V
AC input low voltage	V_{IL} (ac)	V_{REF} – 0.4	V
Input signal siew rate	SLEW	1.0	V/ns



Relationship Between Frequency and Minimum Latency

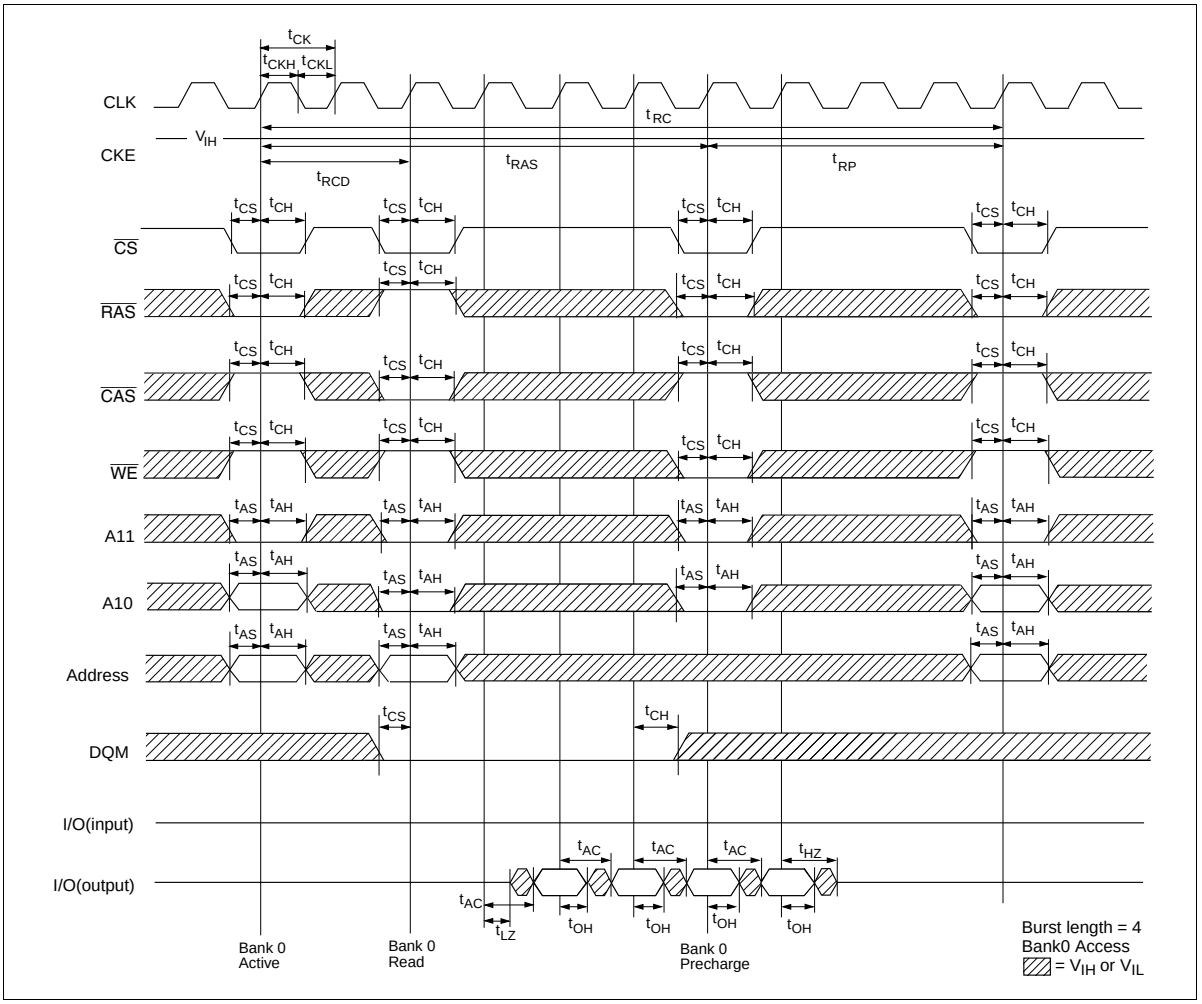
		HM5216808C/HM5216408C						
Parameter		**-80**		**-10**		**-12**		
Frequency (MHz)		**125**	**83**	**100**	**66**	**83**	**55**	
t_{CK} (ns)	**Symbol**	**8**	**12**	**10**	**15**	**12**	**18**	**Notes**
Active command to column command (same bank)	t_{RCD}	3	2	3	2	3	2	1
Active command to active command (same bank)	t_{RC}	10	7	9	6	9	6	= [t_{RAS} + t_{RP}] 1
Active command to precharge command (same bank)	t_{RAS}	7	5	6	4	6	4	1
Precharge command to active command (same bank)	t_{RP}	3	2	3	2	3	2	1
Last data input to precharge command (same bank)	t_{RWL}	2	1	2	1	2	1	1
Active command to active command (different bank)	t_{RRD}	2	2	2	2	2	2	1
Self refresh exit time	l_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)	l_{APW}	5	3	5	3	5	3	= [t_{RWL} + t_{RP}]
Self refresh exit to command input	l_{SEC}	9	6	9	6	9	6	= [t_{RC}]
Precharge command to high impedance ($\overline{CAS}$ latency = 2)	l_{HZP}	—	2	—	2	—	2	
($\overline{CAS}$ latency = 3)	l_{HZP}	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)	l_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge) ($\overline{CAS}$ latency = 2)	l_{EP}	—	–1	—	–1	—	–1	
($\overline{CAS}$ latency = 3)	l_{EP}	–2	–2	–2	–2	–2	–2	
Column command to column command	l_{CCD}	1	1	1	1	1	1	
Write command to data in latency	l_{WCD}	0	0	0	0	0	0	
DQM to data in	l_{DID}	0	0	0	0	0	0	
DQM to data out	l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable	l_{CLE}	1	1	1	1	1	1	
Register set to active command	l_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable	l_{CDD}	0	0	0	0	0	0	
Power down exit to command input	l_{PEC}	1	1	1	1	1	1	

Notes: 1. t_{RCD} to t_{RRD} are recommended value.

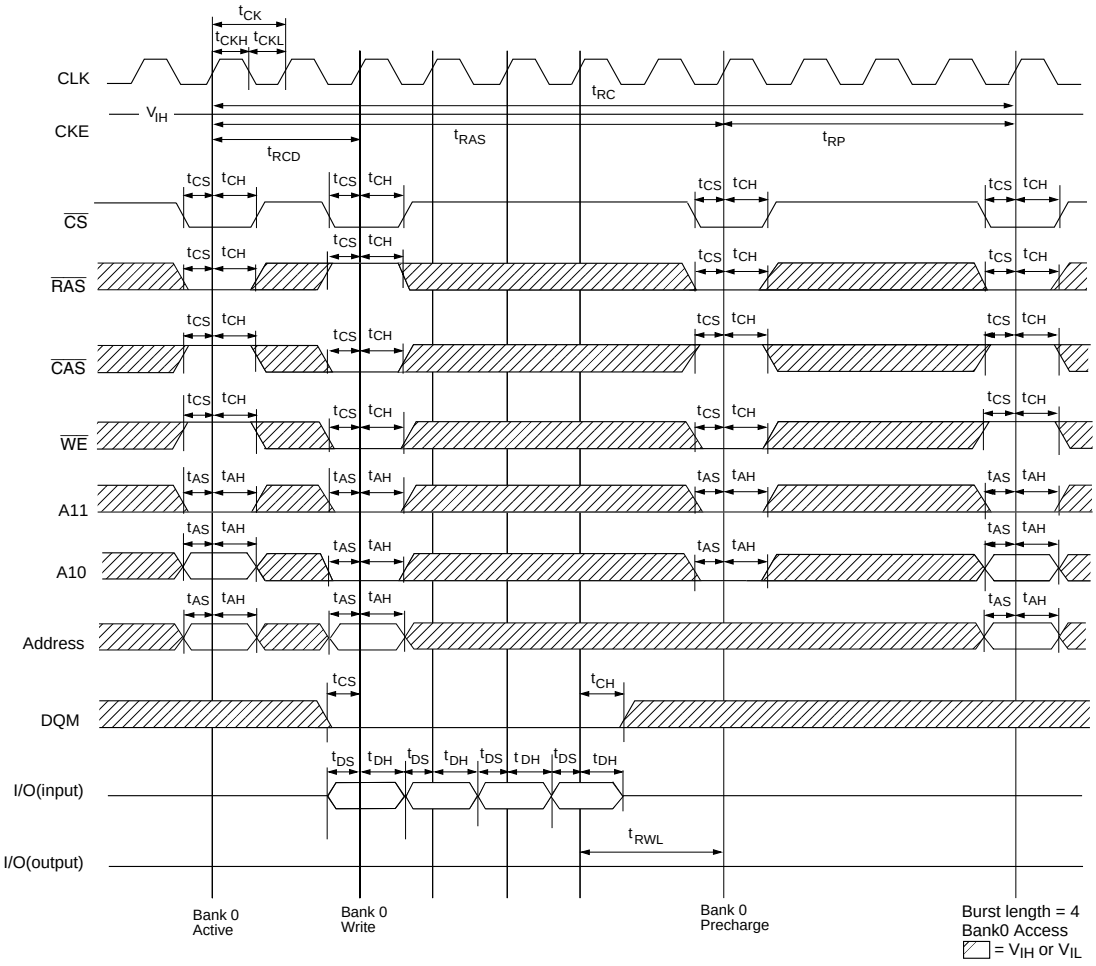
2. When self refresh exit is executed, CKE should be kept „H“ longer than l_{SREX} from exit cycle.

Timing Waveforms

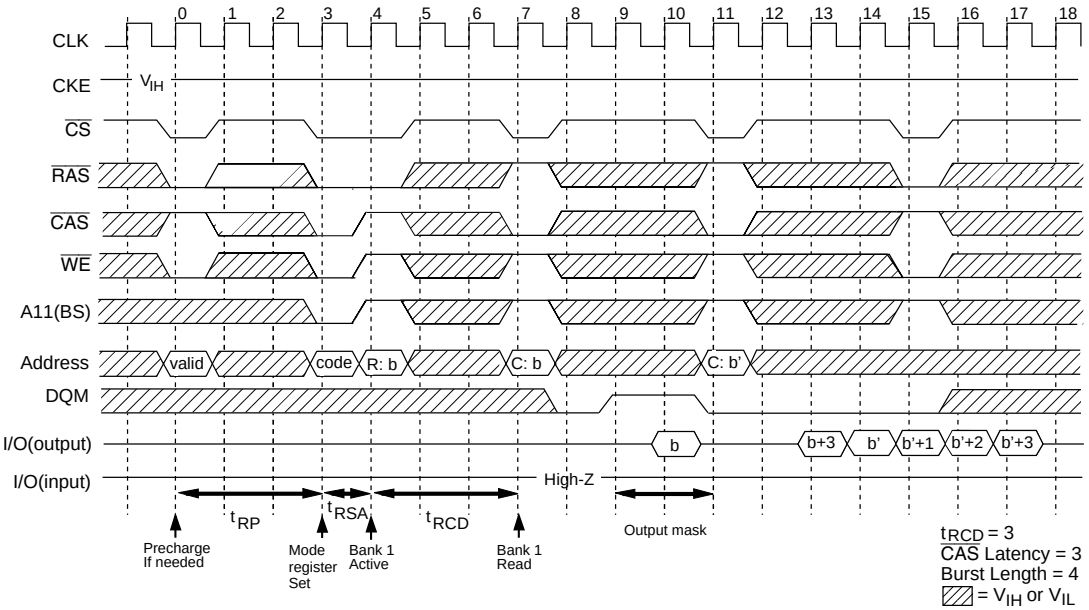
Read Cycle



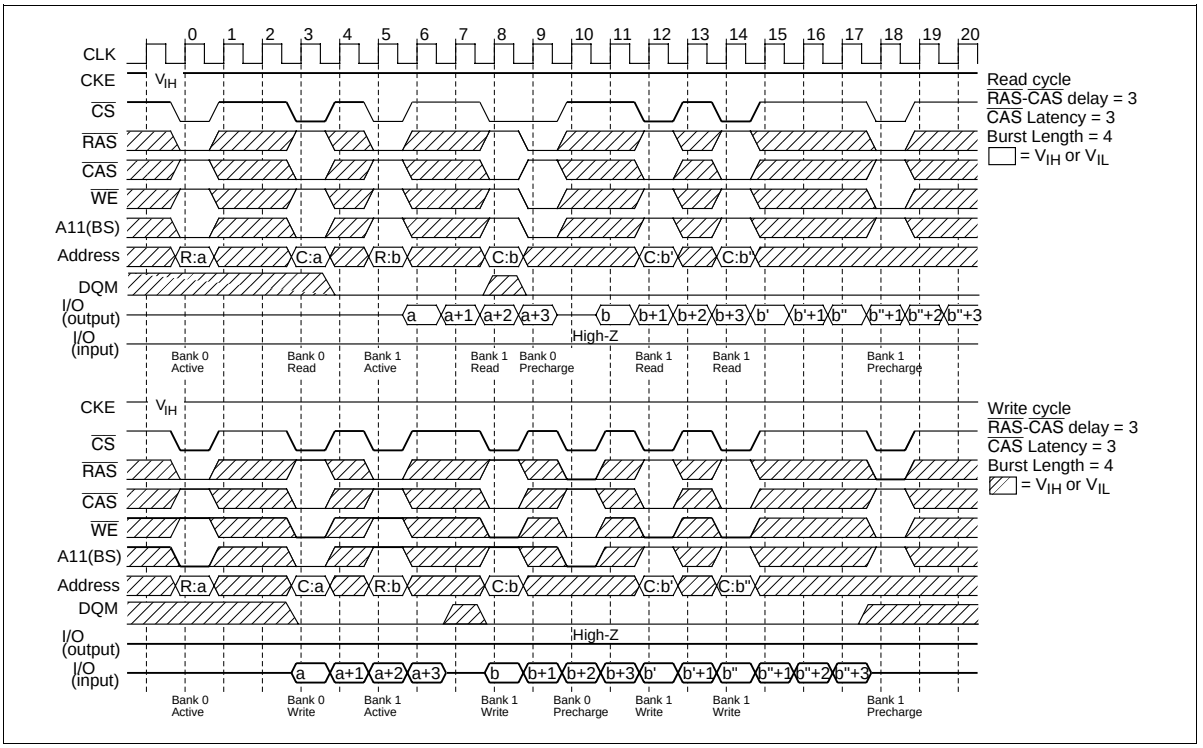
Write Cycle


tCK
tCKH tCKL
CLK
VIH
CKE
tRC
tRAS
tRP
tRCD
CS
RAS
CAS
WE
A11
A10
Address
DQM
I/O(input)
I/O(output)
tCS tCH
tAS tAH
tDS tDH
tRWL
Bank 0 Active
Bank 0 Write
Bank 0 Precharge
Burst length = 4
Bank0 Access
= VIH or VIL

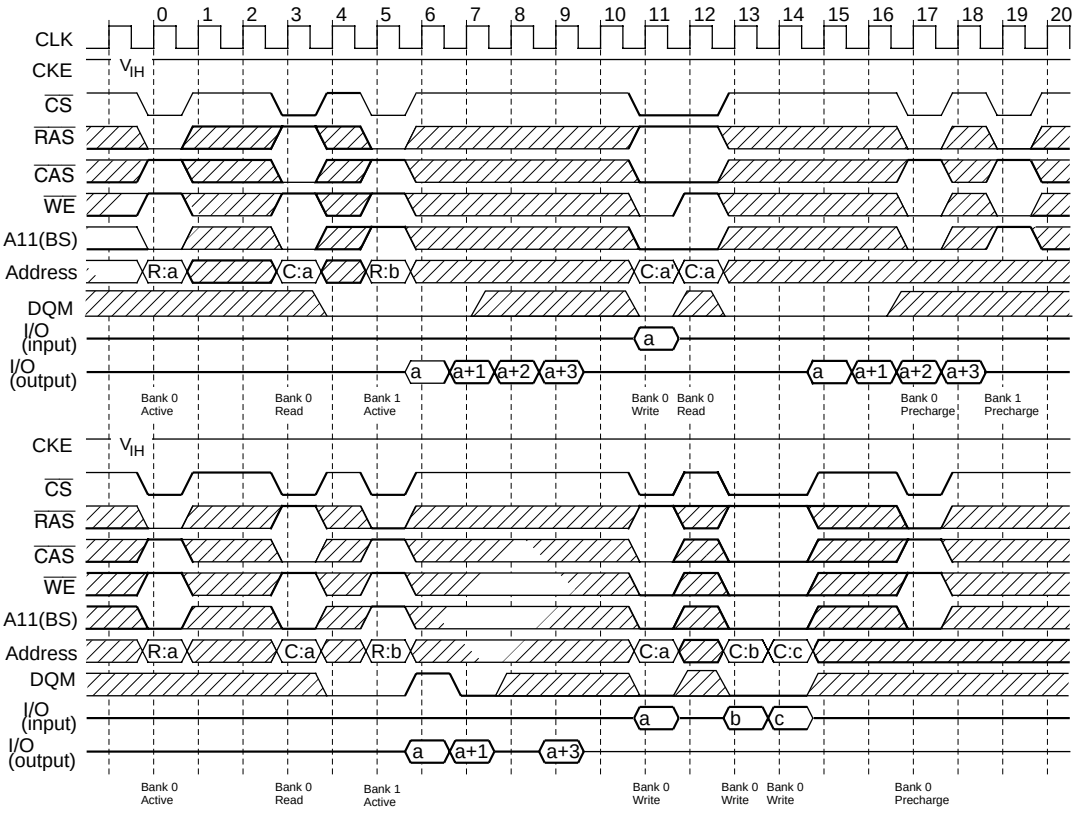
Mode Register Set Cycle



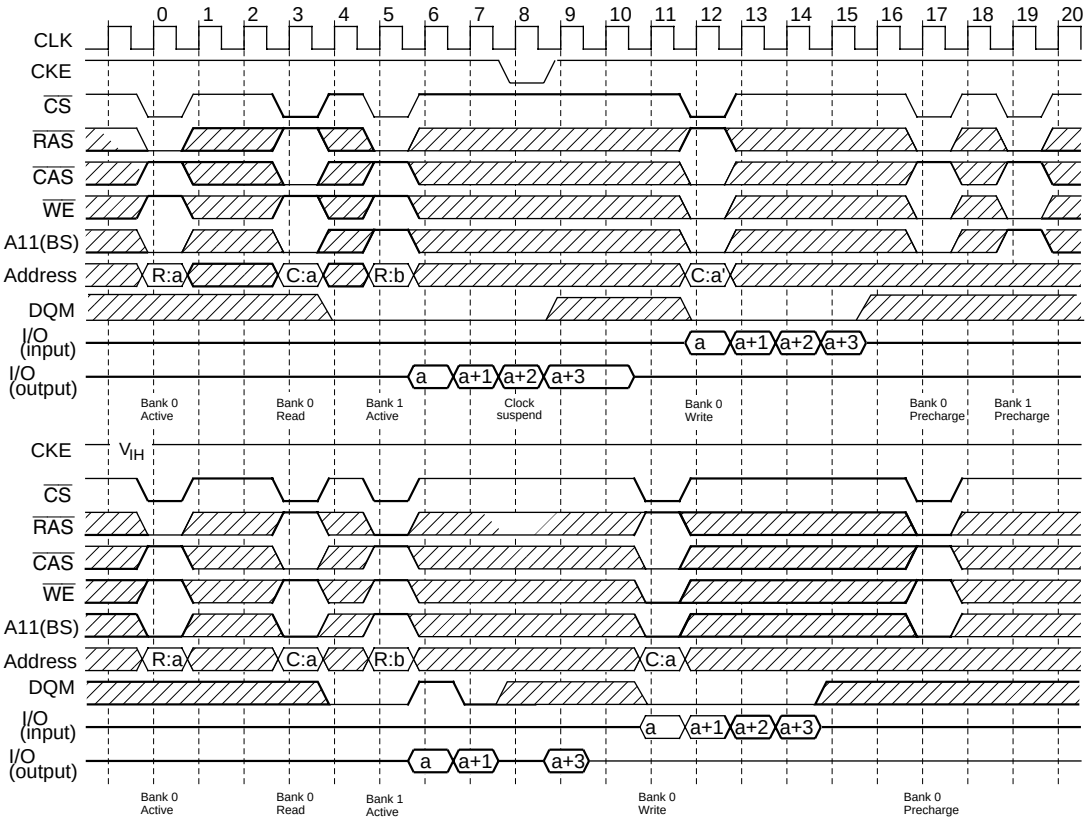
Read Cycle/Write Cycle



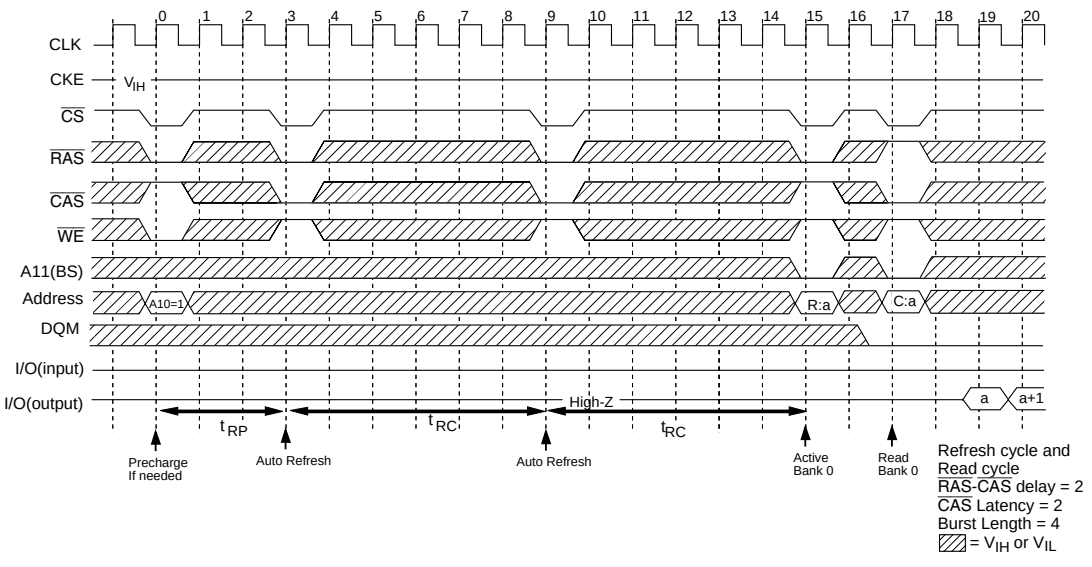
Read/Single Write Cycle



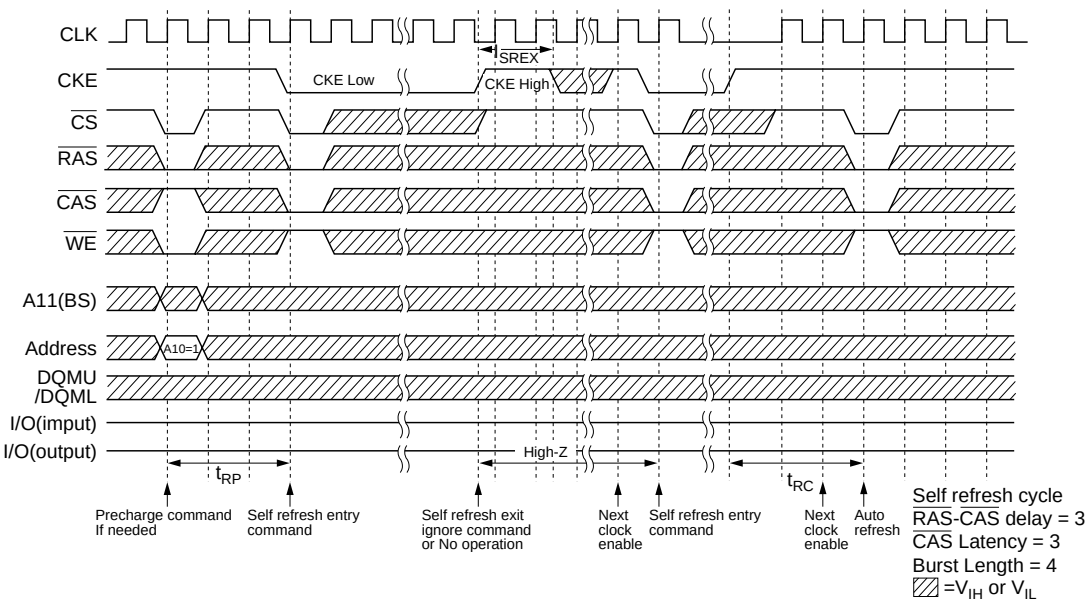
Read/Burst Write Cycle



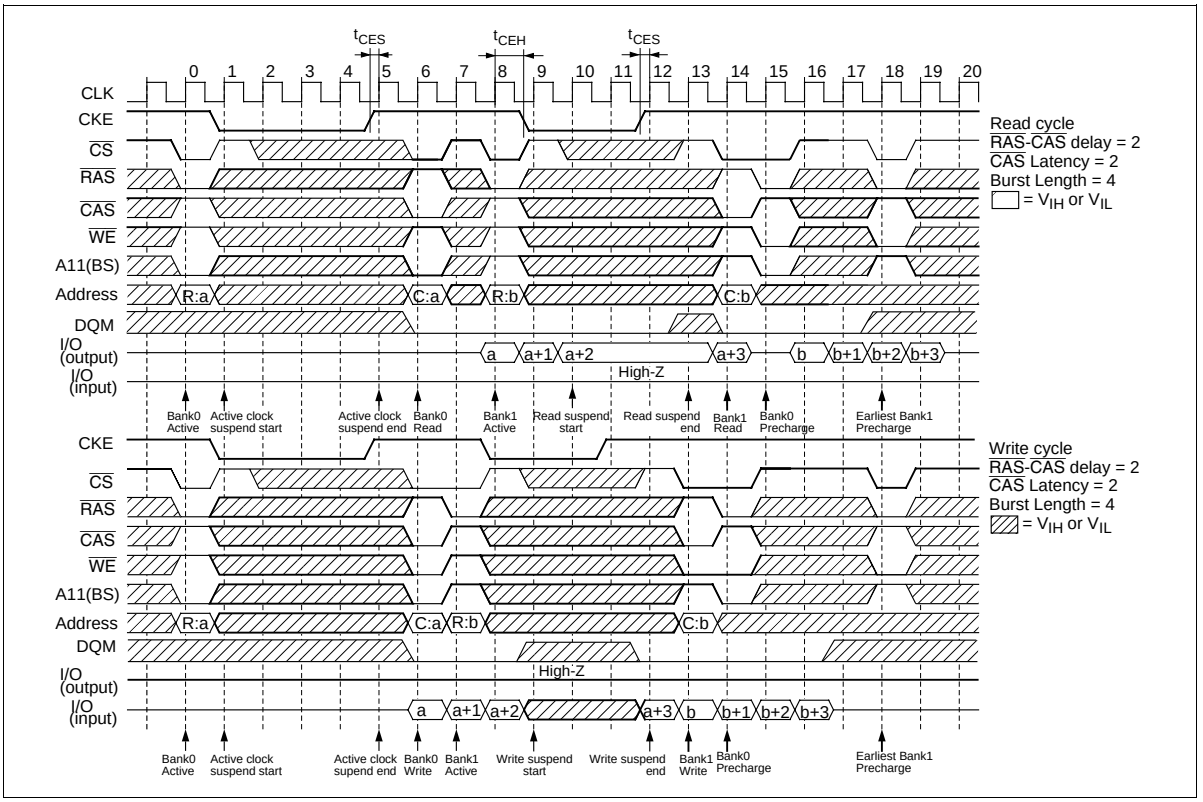
Auto Refresh Cycle



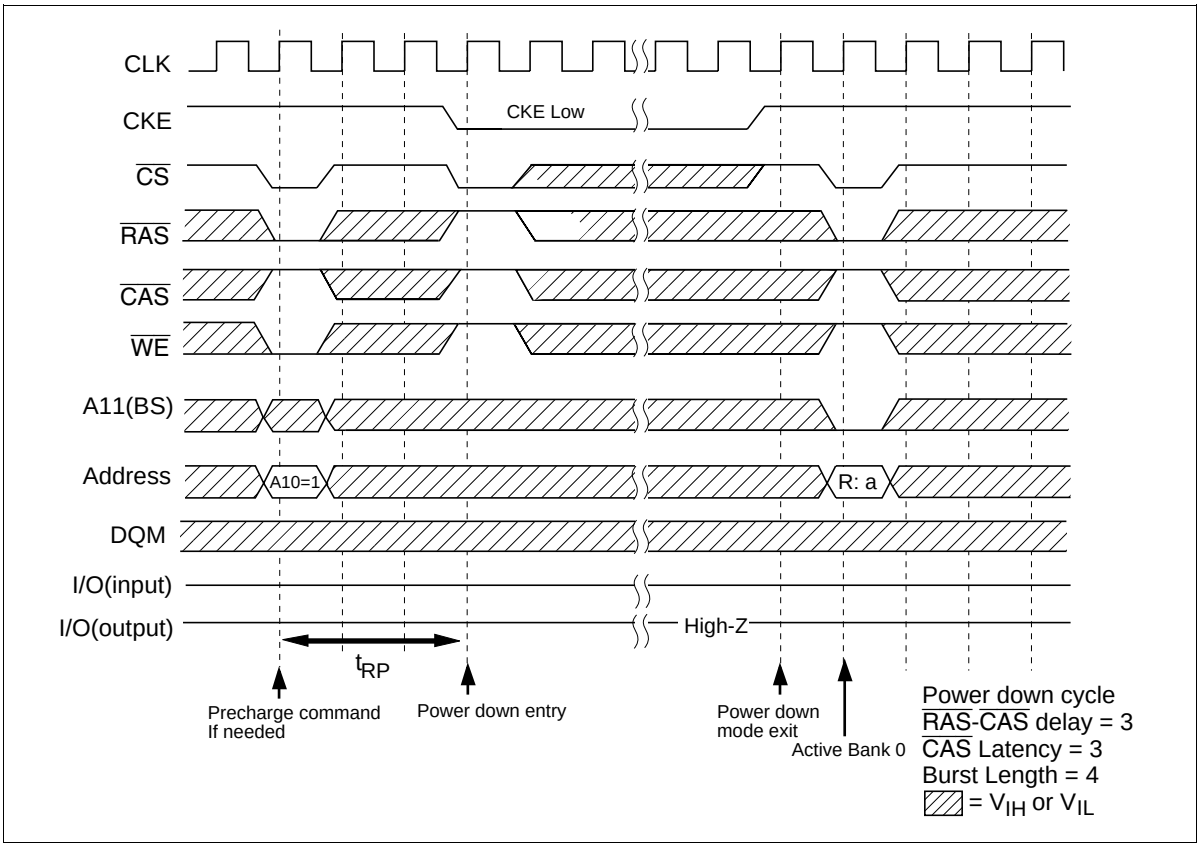
Self Refresh Cycle



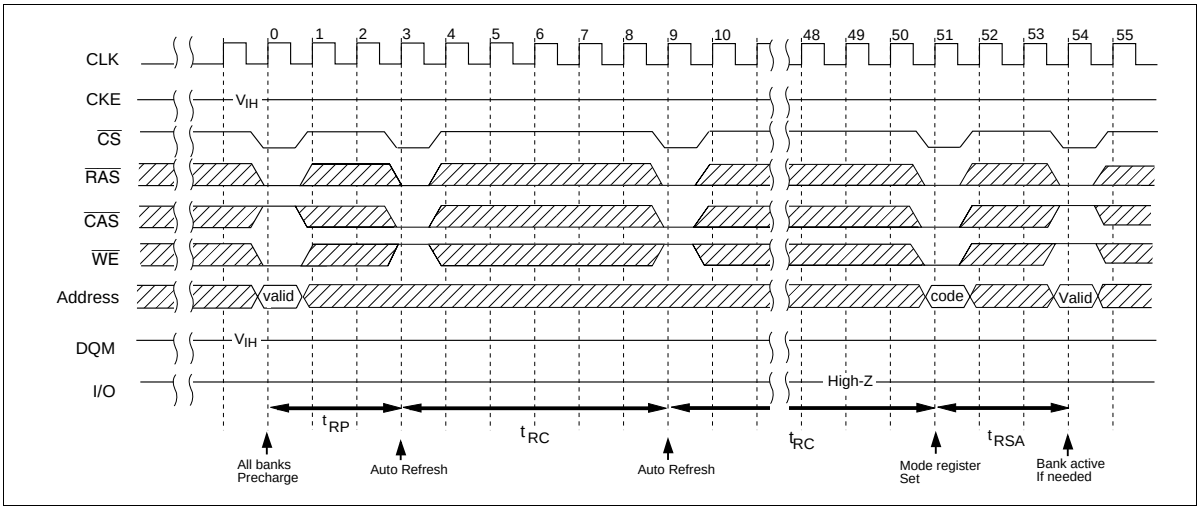
Clock Suspend Mode



Power Down Mode

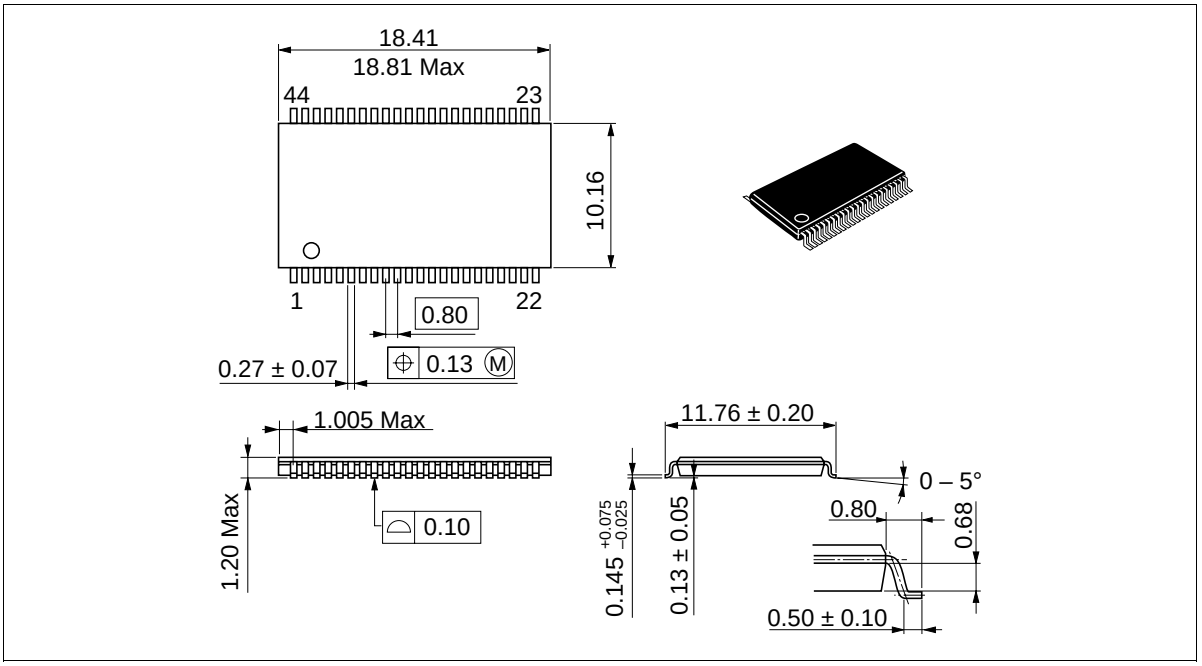


Power Up Sequence



Package Dimensions

HM5216808CTT/HM5216408CTT Series (TTP-44DE) Unit: mm



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0.0	Jul. 10, 1996	Initial issue		