
HM514405C Series

1,048,576-word $\times$ 4-bit Dynamic Random Access Memory

HITACHI

Description

The Hitachi HM514405C is a CMOS dynamic RAM organized 1,048,576-word $\times$ 4-bit. HM514405C has realized higher density, higher performance and various functions by employing 0.8 μ m CMOS process technology and some new CMOS circuit design technologies. The HM514405C offers Extended Data Out (EDO) Page Mode as a high speed access mode. Multiplexed address input permits the HM514405C to be packaged in standard 300-mil 26-pin plastic SOJ and standard 300-mil 26-pin plastic TSOP II.

Features

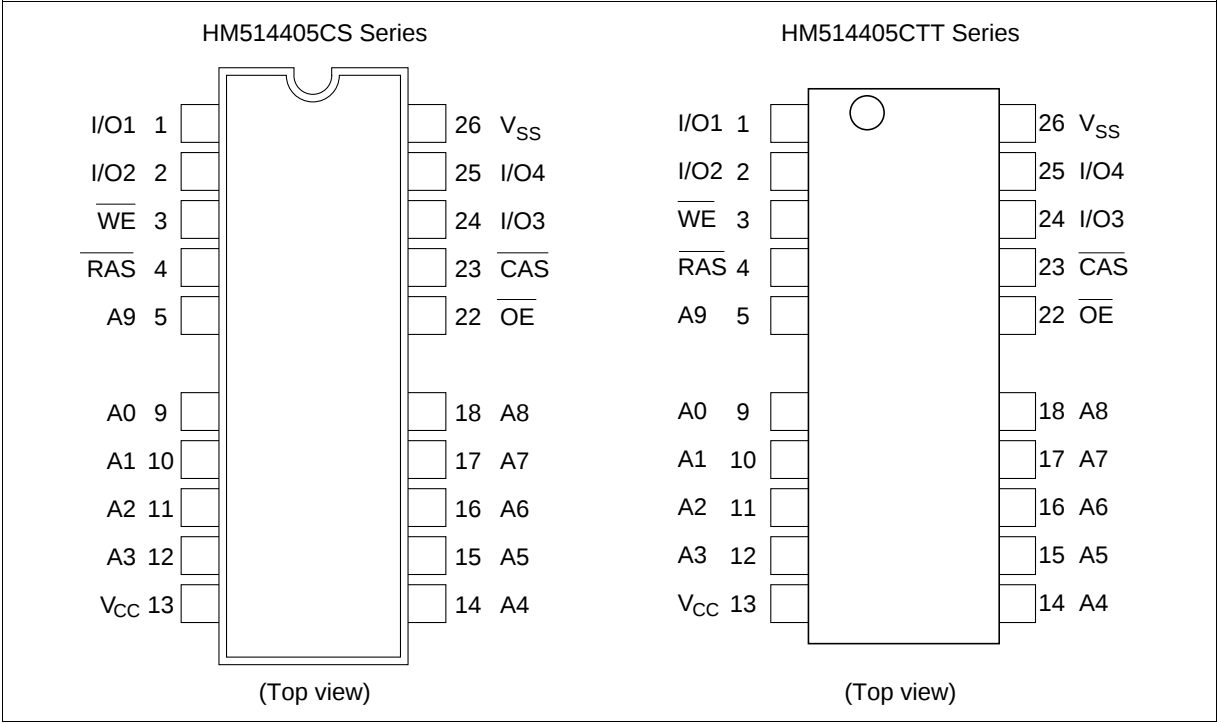
- Single 5 V ($\pm 10\%$)
- High speed
 - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode: 605 mW/550 mW/495 mW (max)
 - Standby mode: 11 mW (max)
- EDO page mode capability
- 1024 refresh cycles : 16 ms
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- Test function

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Ordering Information

Type No.	Access Time	Package
HM514405CS-6	60 ns	300-mil 26-pin plastic SOJ (CP-26/20D)
HM514405CS-7	70 ns	
HM514405CS-8	80 ns	
HM514405CTT-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/20D)
HM514405CTT-7	70 ns	
HM514405CTT-8	80 ns	

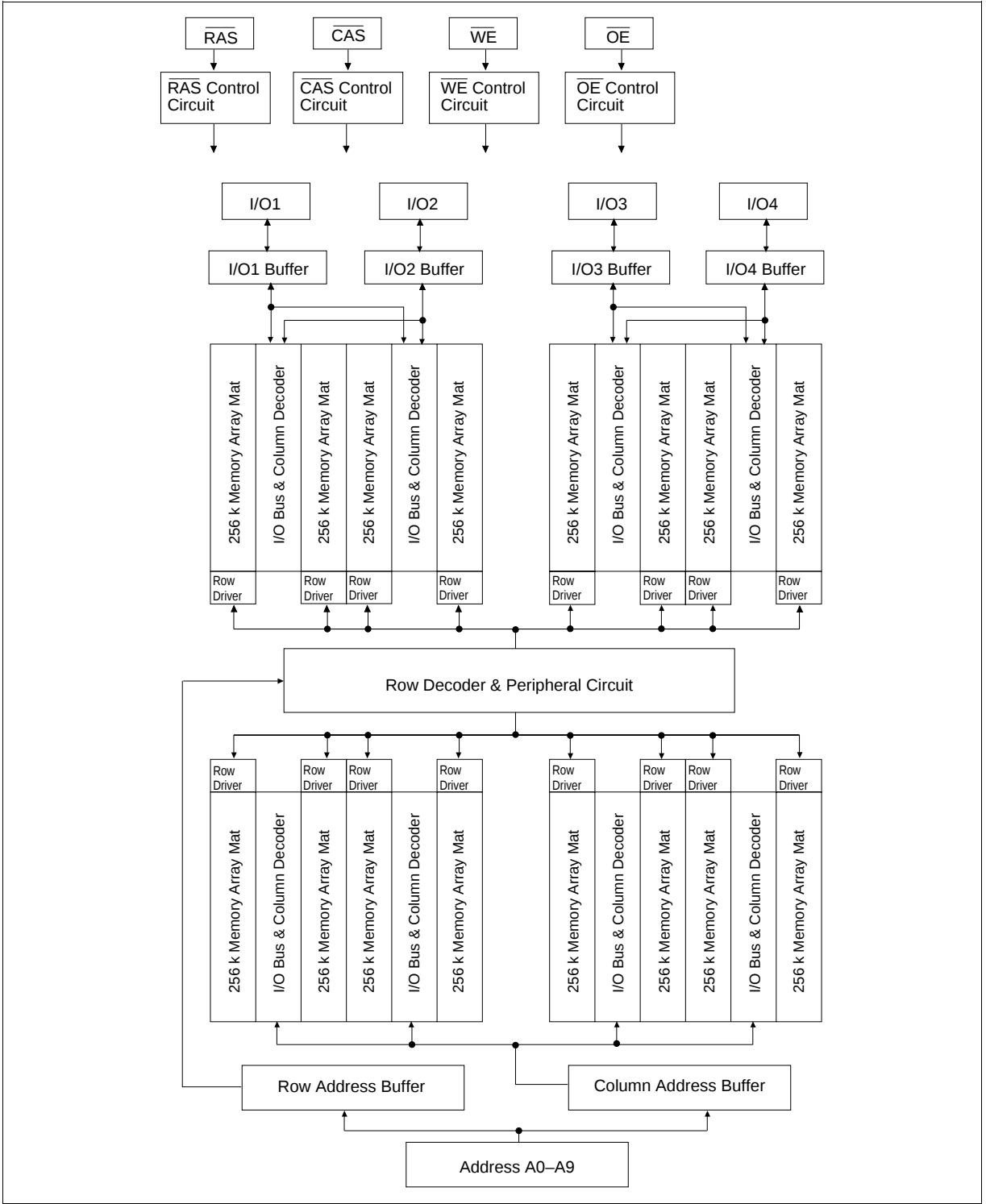
Pin Arrangement



Pin Description

Pin Name	Function
A0 to A9	Address input
A0 to A9	Refresh address input
I/O1 to I/O4	Data-in/Data-out
RAS	Row address strobe
CAS	Column address strobe
WE	Read/Write enable
OE	Output enable
VCC	Power (+5 V)
VSS	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514405C								
		-6		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions	Notes
Operating current	I _{CC1}	—	110	—	100	—	90	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling t _{RC} = min	1, 2
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{\text{IH}}$ Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Dout = High-Z	
$\overline{\text{RAS}}$ -only refresh current	I _{CC3}	—	110	—	100	—	90	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	5	—	5	—	5	mA	$\overline{\text{RAS}} = V_{\text{IH}},$ $\overline{\text{CAS}} = V_{\text{IL}}$ Dout = enable	1
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	I _{CC6}	—	110	—	100	—	90	mA	t _{RC} = min	
EDO page mode current	I _{CC4}	—	130	—	120	—	110	mA	t _{HPC} = min	1, 3
Input leakage current	I _{LI}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I _{LO}	−10	10	−10	10	−10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed twice or less while RAS = V_{IL}.
3. Address can be changed once or less while CAS = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	5	pF	1
Input capacitance (Clocks)	C _{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	C _{I/O}	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. RAS and CAS = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)^{*1, *14, *15, *16}

Test Conditions

- Input rise and fall time : 2 ns
- Input level : V_{IL} = 0 V, V_{IH} = 3.0 V
- Input timing reference levels : 0.8 V, 2.4 V
- Output timing reference levels : 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM514405C							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	104	—	124	—	144	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	10000	70	10000	80	10000	ns	19
$\overline{\text{CAS}}$ pulse width	t _{CAS}	10	10000	13	10000	15	10000	ns	20
Row address setup time	t _{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	10	—	13	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	45	20	52	20	60	ns	8
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	30	15	35	15	40	ns	9
$\overline{\text{RAS}}$ hold time	t _{RSH}	15	—	18	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	48	—	58	—	68	—	ns	23
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ to Din delay time	t _{ODD}	15	—	18	—	20	—	ns	
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ setup time from Din	t _{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	7
Refresh period	t _{REF}	—	16	—	16	—	16	ms	

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Read Cycle

Parameter	Symbol	HM514405C						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3, 17
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	—	20	ns	3, 4, 13, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	3, 5, 13, 17
Access time from $\overline{\text{OE}}$	t_{OAC}	—	15	—	18	—	20	ns	3, 17
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	18
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	18
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	28	—	ns	
Output buffer turn-off time	t_{OFF1}	—	15	—	15	—	15	ns	6, 21
Output buffer turn-off time to $\overline{\text{OE}}$	t_{OFF2}	—	15	—	15	—	15	ns	6
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	20	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	20	—	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WDD}	15	—	18	—	20	—	ns	
$\overline{\text{OE}}$ pulse width	t_{OEP}	15	—	18	—	20	—	ns	
Turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	—	15	ns	6, 21
Turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	—	15	ns	6
Output data hold time	t_{OH}	5	—	5	—	5	—	ns	
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	80	—	ns	
Read command hold time from $\overline{\text{CAS}}$	t_{RCHC}	15	—	18	—	20	—	ns	
Read command hold time from column address	t_{RCHA}	30	—	35	—	40	—	ns	

Write Cycle

		HM514405C							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	10	—	13	—	15	—	ns	
Write command pulse width	t_{Wp}	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	10	—	13	—	15	—	ns	11

Read-Modify-Write Cycle

		HM514405C							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	133	—	159	—	183	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	—	90	—	102	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	—	38	—	42	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	47	—	55	—	62	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEh}	15	—	18	—	20	—	ns	

Refresh Cycle

		HM514405C							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	13	—	15	—	ns	

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EDO Page Mode Cycle

		HM514405C							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t _{HPC}	25	—	30	—	35	—	ns	22
EDO page mode $\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	13	—	15	—	ns	
EDO page mode $\overline{\text{RAS}}$ pulse width	t _{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	35	—	40	—	45	ns	3, 13, 17
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	35	—	40	—	45	—	ns	
Output data hold time from $\overline{\text{CAS}}$ low	t _{DOH}	3	—	3	—	3	—	ns	
$\overline{\text{CAS}}$ hold time referred $\overline{\text{OE}}$	t _{COL}	10	—	13	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ setup time	t _{COP}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{\text{CAS}}$ precharge	t _{RCHP}	35	—	40	—	45	—	ns	

EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514405C						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	t _{HPCM}	66	—	77	—	86	—	ns	
EDO page mode read-modify-write cycle $\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t _{CPW}	52	—	60	—	67	—	ns	10

Test Mode Cycle

		HM514405C							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{\text{WE}}$ setup time	t _{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{\text{WE}}$ hold time	t _{WH}	10	—	10	—	10	—	ns	

Counter Test Cycle

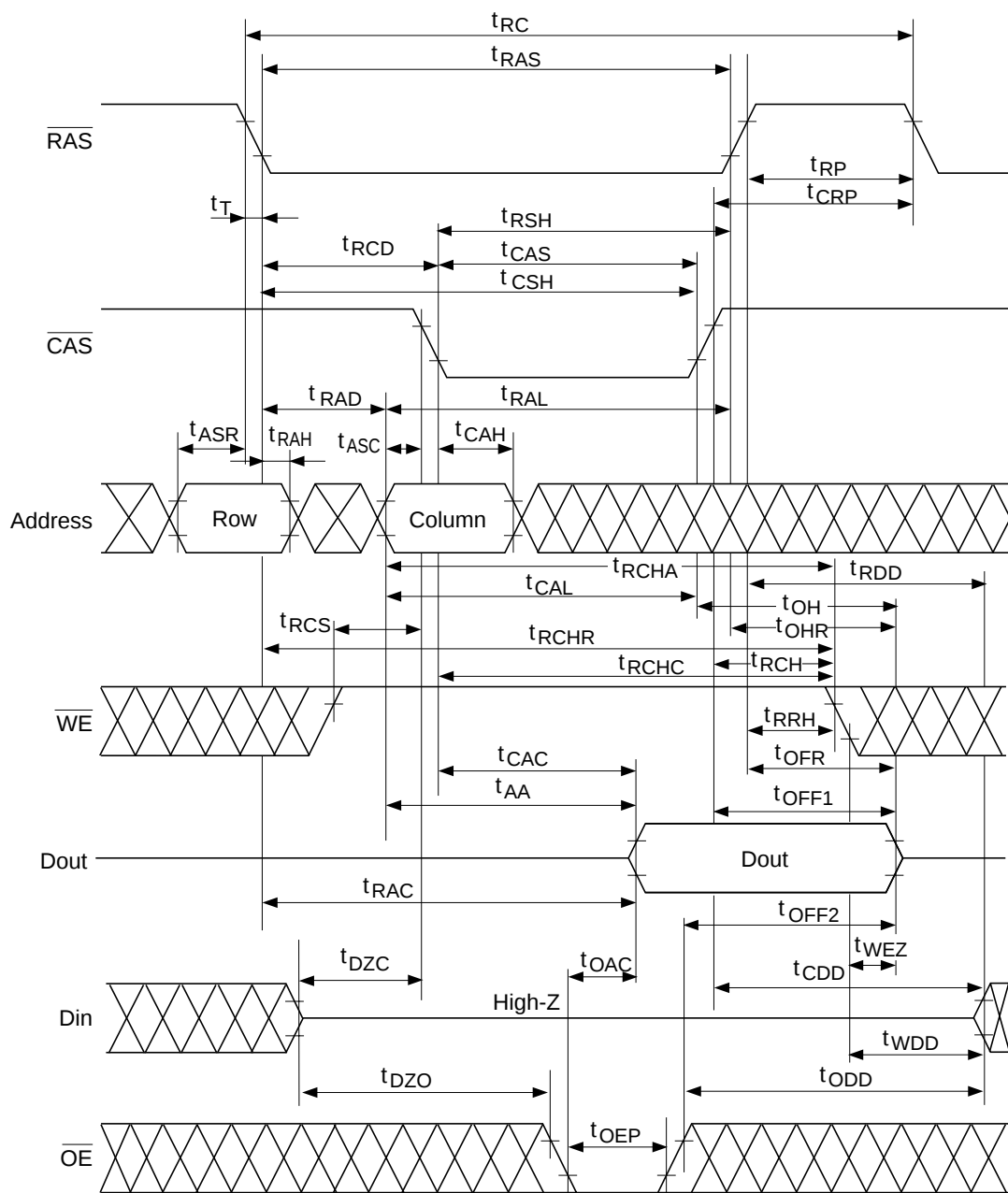
		HM514405C							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{\text{CAS}}$ precharge time in counter test cycle	t_{CPT}	40	—	40	—	40	—	ns	

- Notes:
1. AC measurements assume $t_T = 2$ ns.
 2. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 4. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$.
 5. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.
 6. $t_{\text{OFF1}}(\text{max})$, $t_{\text{OFF2}}(\text{max})$, $t_{\text{OFR}}(\text{max})$ and $t_{\text{WEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
 7. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} , t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referred to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or read-modify-write cycle.
 12. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 13. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{ACP} .
 14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
 15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits - - - CA0. This test mode operation can be performed by $\overline{\text{WE}}$ -and- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle.
 17. In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} , t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
 18. Either t_{RCH} or t_{RRH} must be satisfied

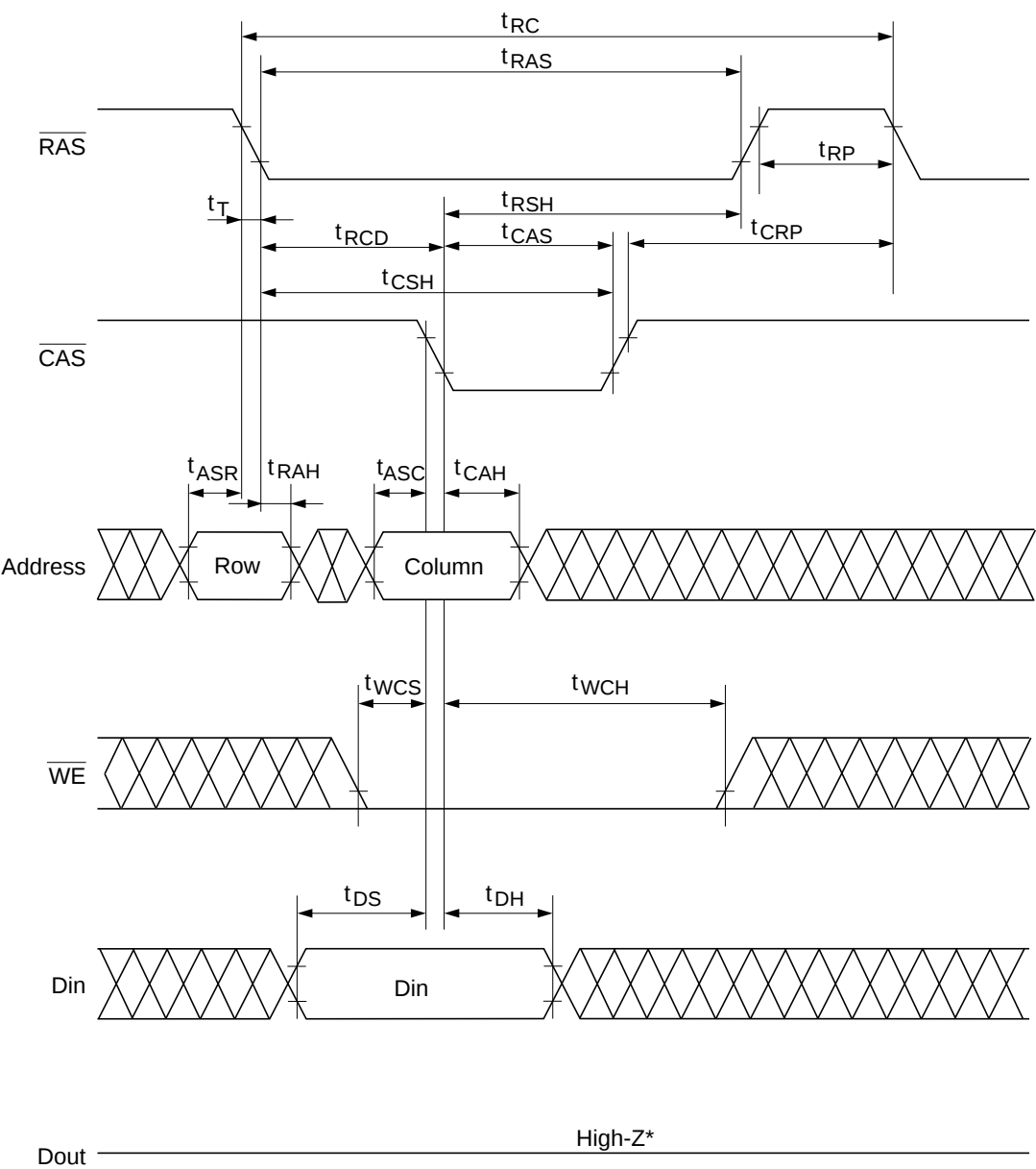
19. $t_{RAS}(\text{min}) = t_{RWD}(\text{min}) + t_{RWL}(\text{min}) + t_T$ in read-modify-write cycle.
20. $t_{CAS}(\text{min}) = t_{CWD}(\text{min}) + t_{CWL}(\text{min}) + t_T$ in read-modify-write cycle.
21. t_{OFF1} and t_{OFR} are determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.
22. $t_{HPC}(\text{min})$ can be achieved during a series of EDO page mode early write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle $t_{HPC}(t_{CAS} + t_{CP} + 2t_T)$ becomes greater than the specified $t_{HPC}(\text{min})$ value.
23. $t_{CSH}(\text{min})$ can be achieved when $t_{RCD} \leq t_{CSH}(\text{min}) - t_{CAS}(\text{min})$.
24. XXXX H or L (H: $V_{IH}(\text{min}) \leq V_{IN} \leq V_{IH}(\text{max})$, L: $V_{IL}(\text{min}) \leq V_{IN} \leq V_{IL}(\text{max})$)
///// Invalid Dout

Timing Waveforms^{*24}

Read Cycle

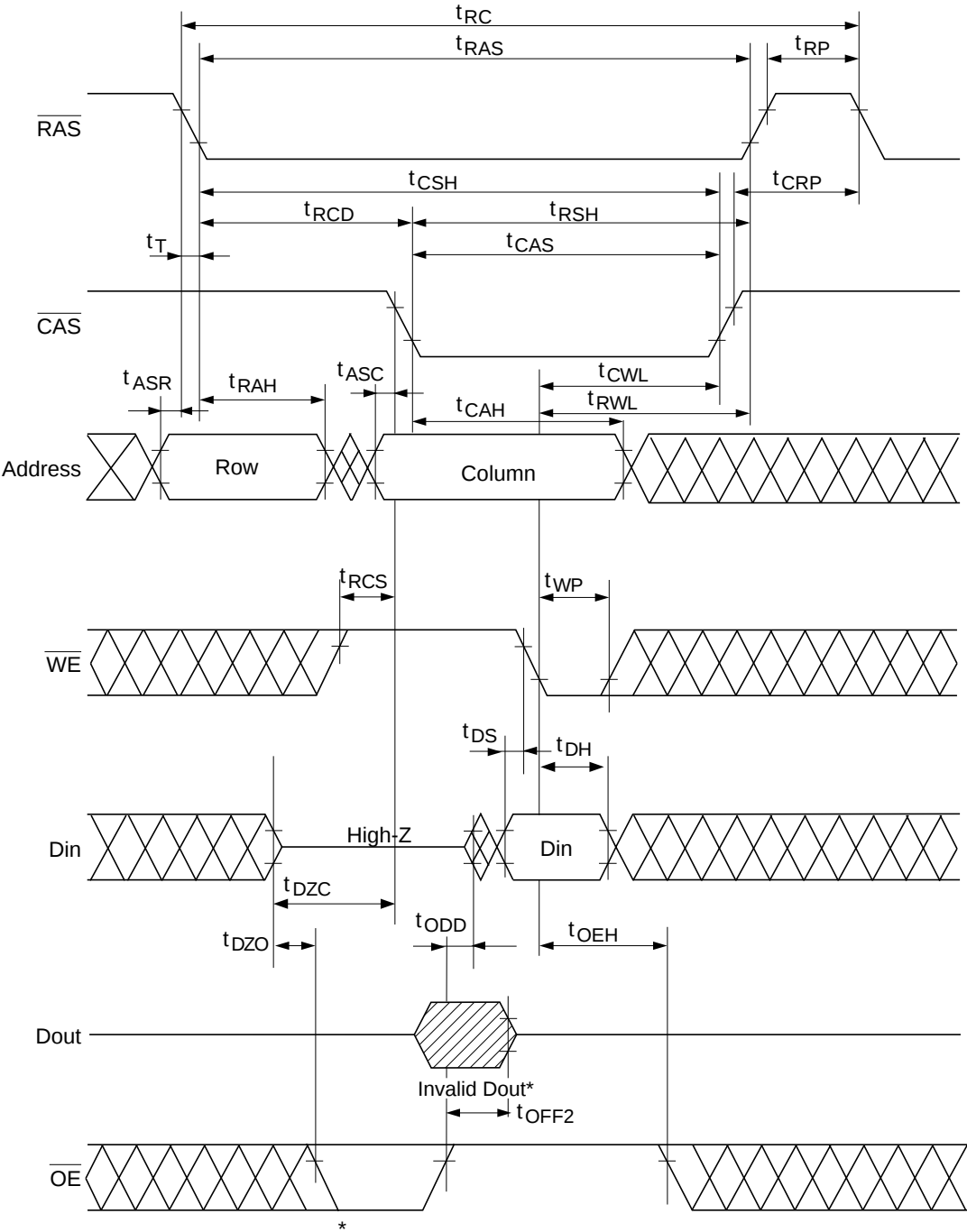


Early Write Cycle



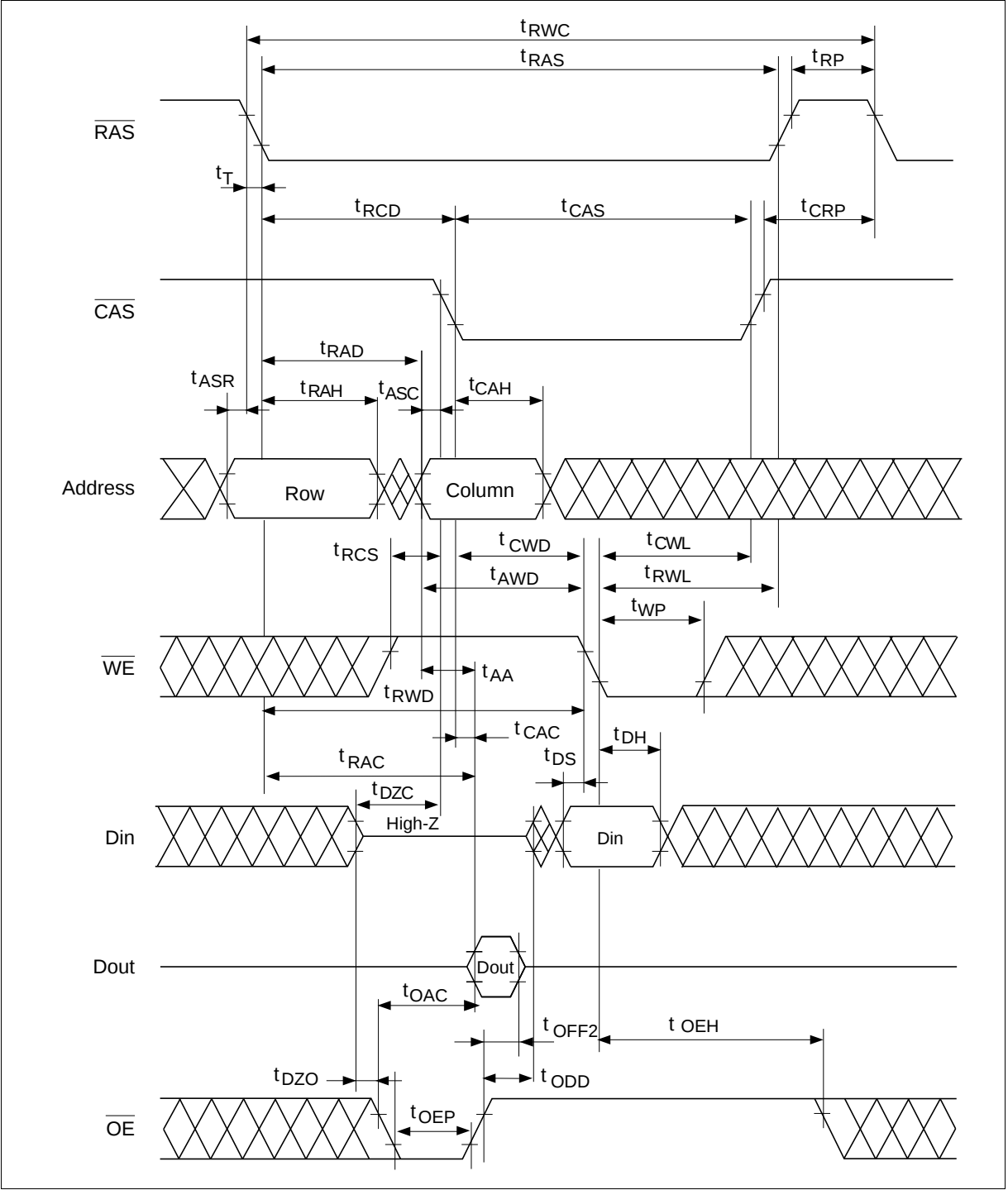
* $t_{WCS} \geq t_{WCS}(\min)$
** $\overline{OE}$: H or L

Delayed Write Cycle

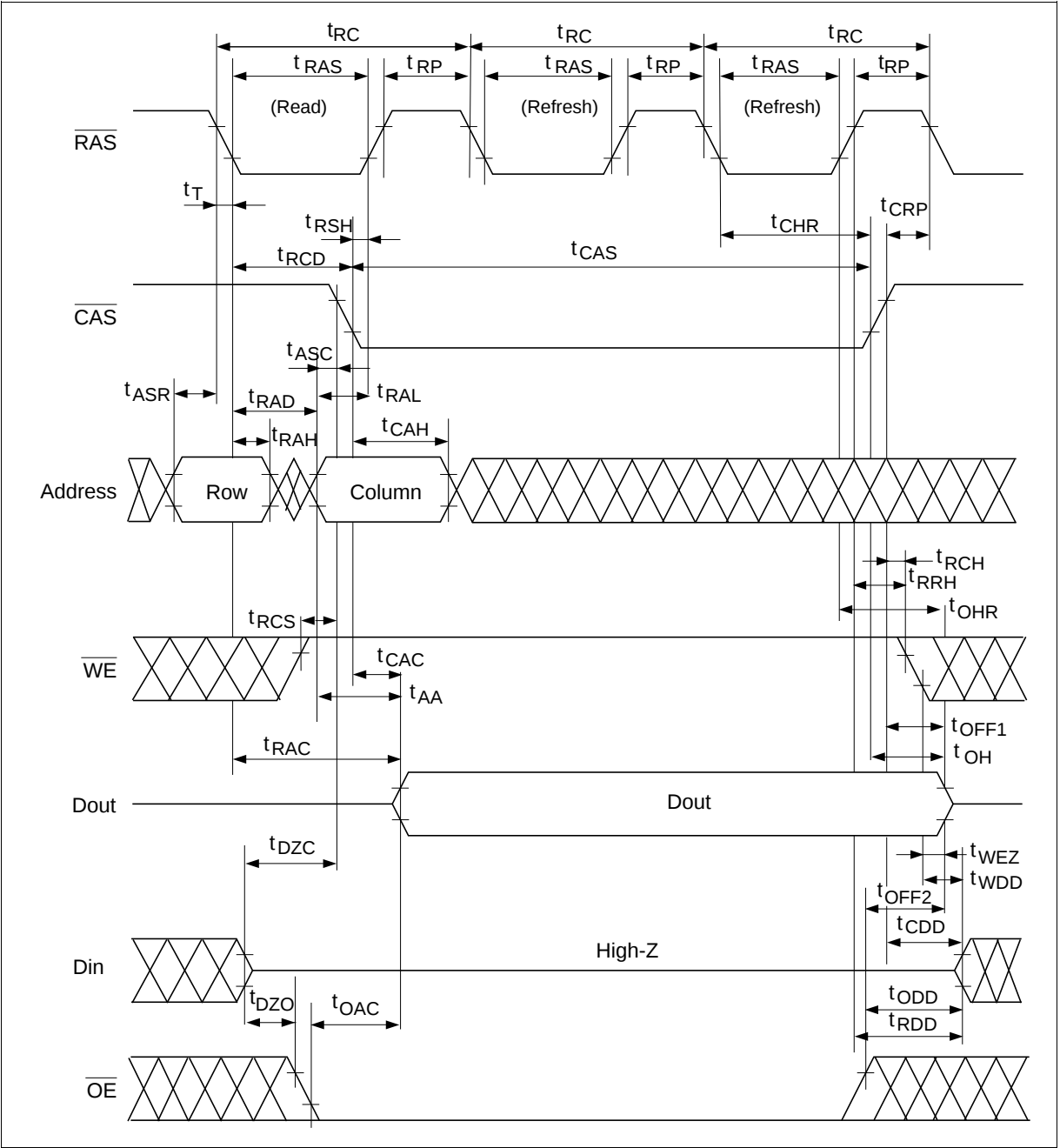


* Invalid Dout comes out, when $\overline{OE}$ is low level.

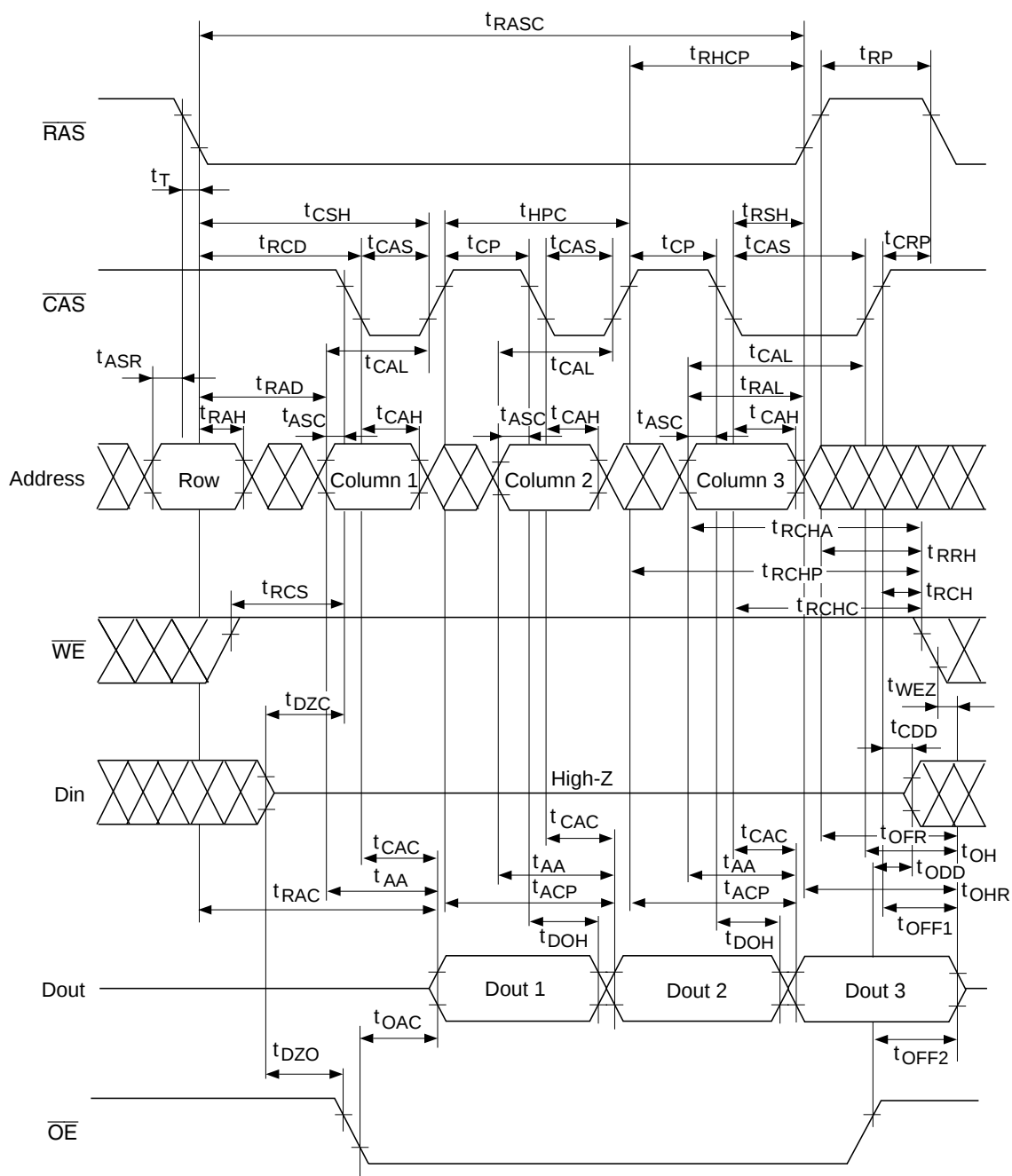
Read-Modify-Write Cycle



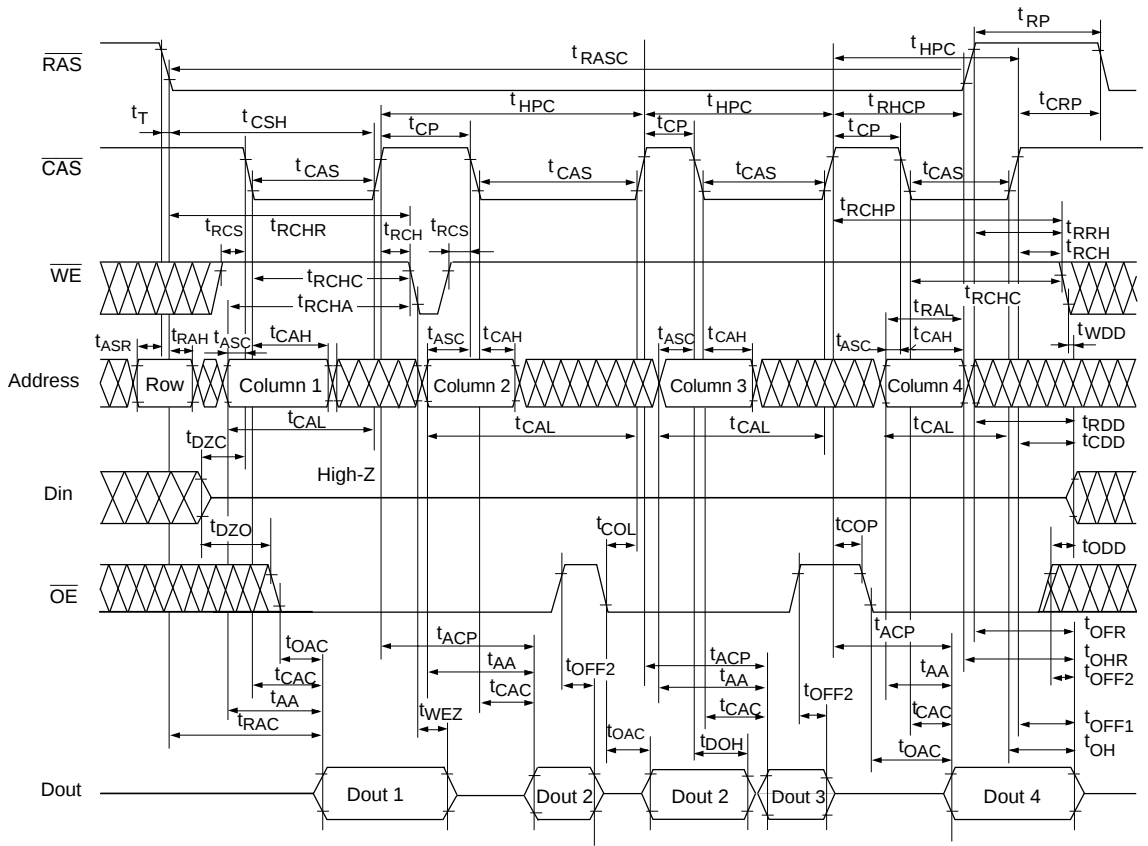
Hidden Refresh Cycle



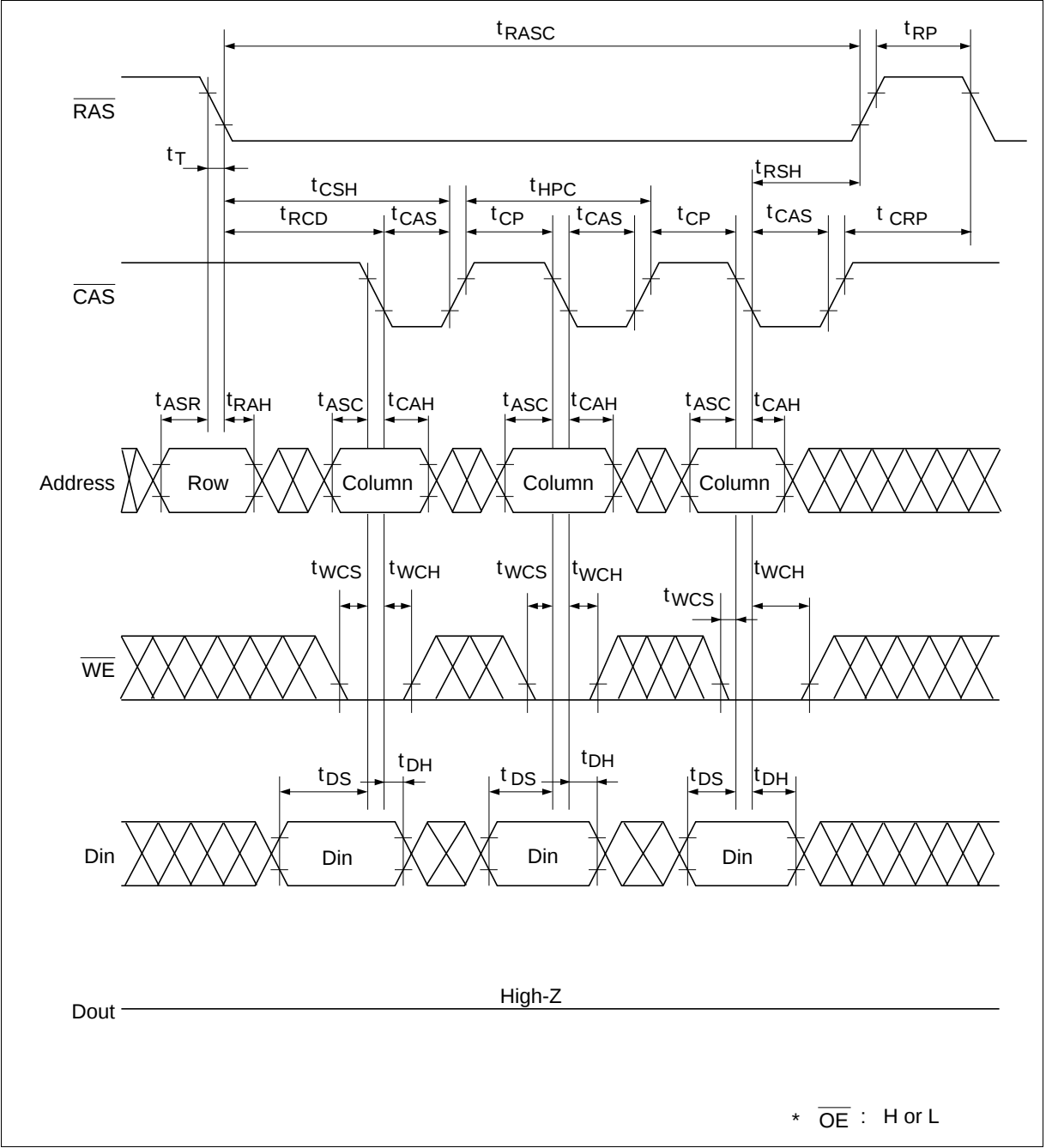
EDO Page Mode Read Cycle (t_{HPC} minimum cycle operation)



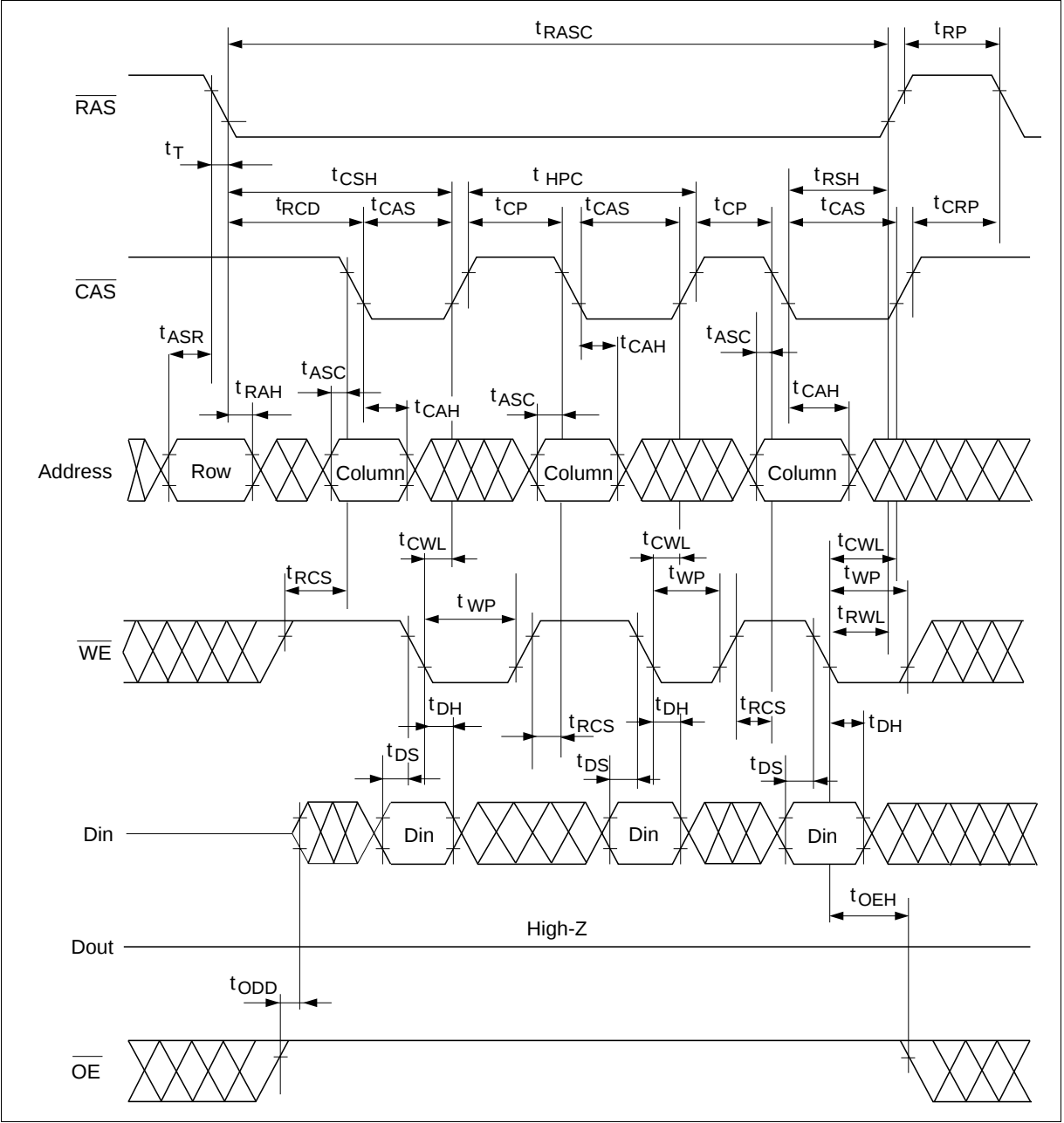
EDO Page Mode Read Cycle (High-Z control by $\overline{\text{WE}}$ and $\overline{\text{OE}}$)

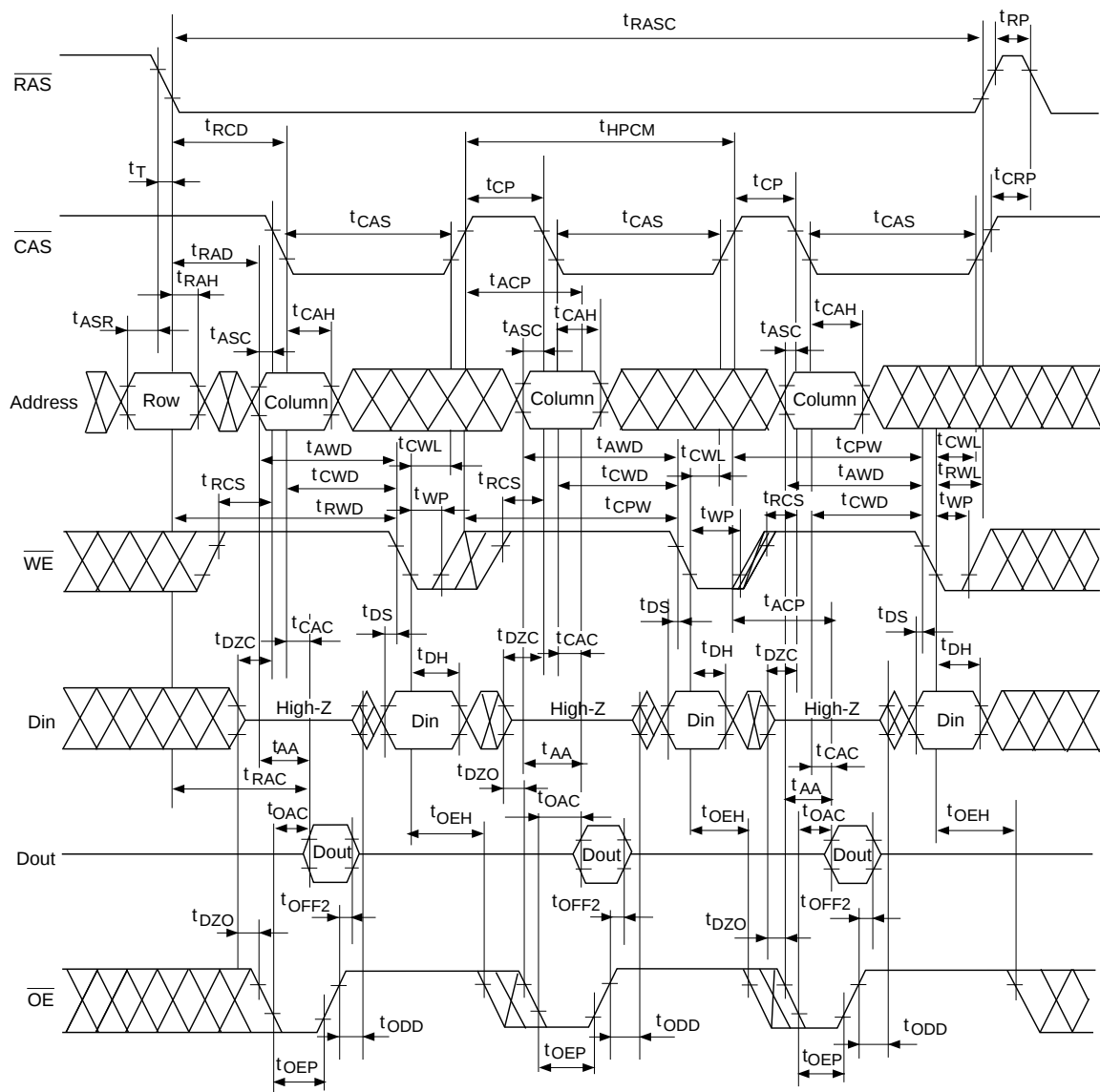


EDO Page Mode Early Write Cycle (t_{HPC} minimum cycle operation)

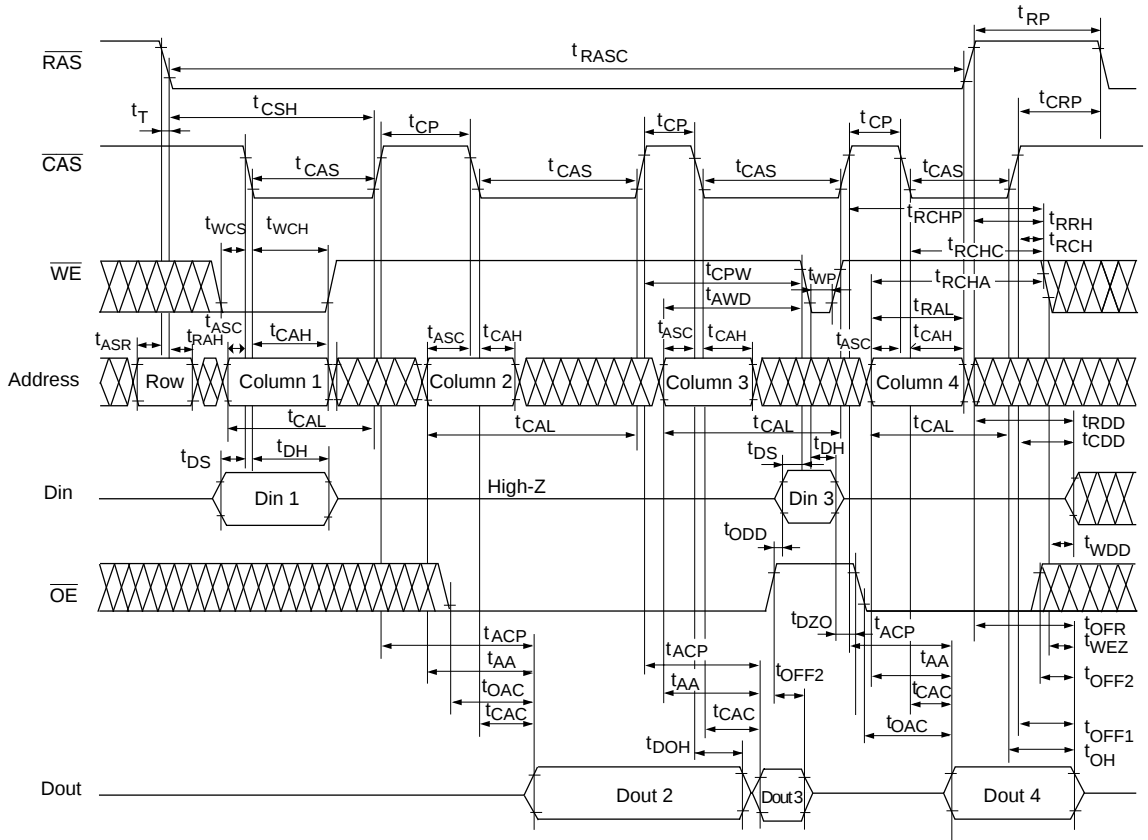


EDO Page Mode Delayed Write Cycle

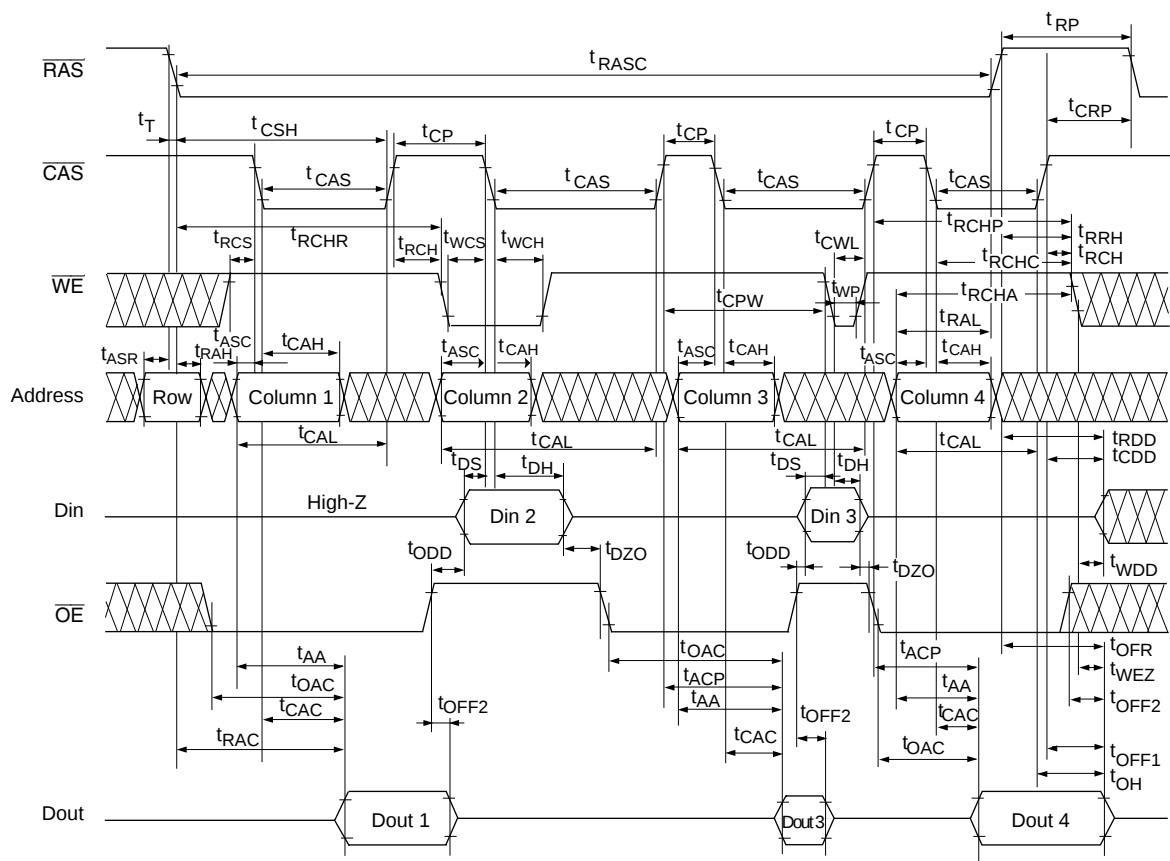




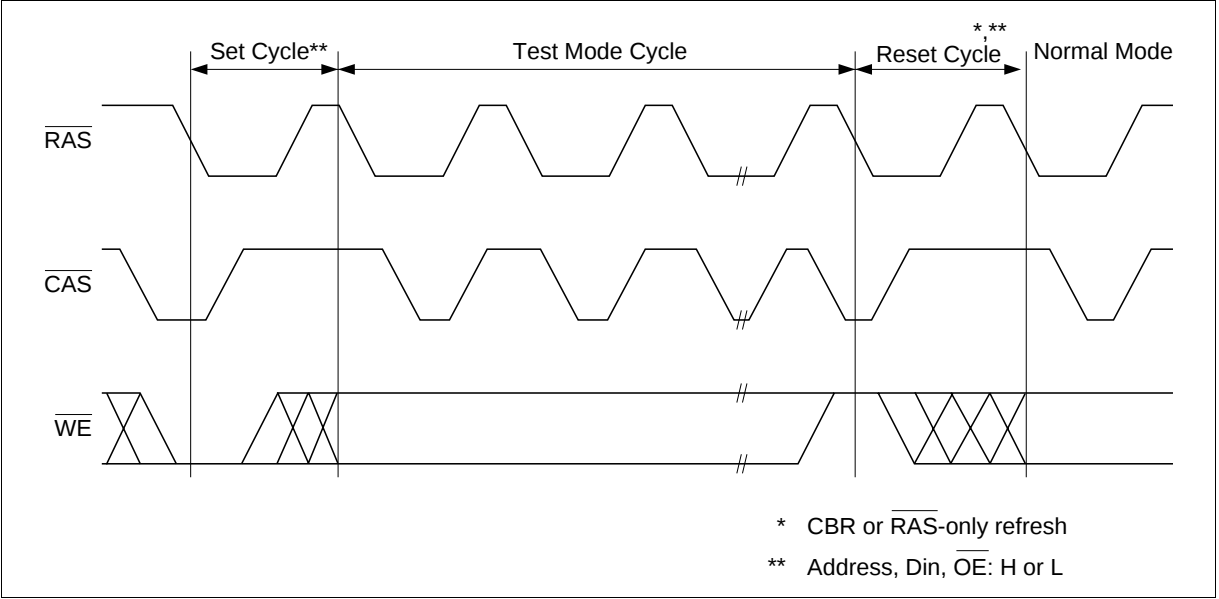
EDO Page Mode Mix Cycle (1)^{*22}



EDO Page Mode Mix Cycle (2) ^{*22}

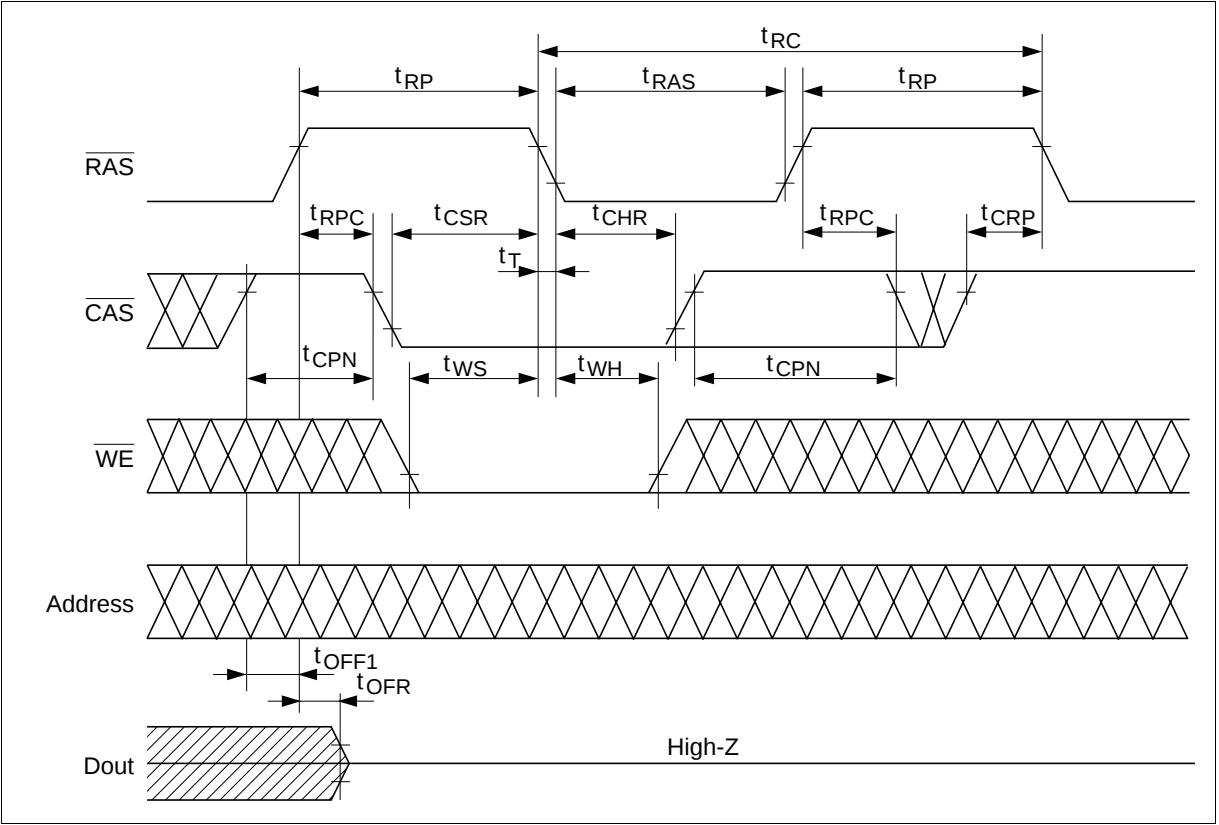


Test Mode Cycle

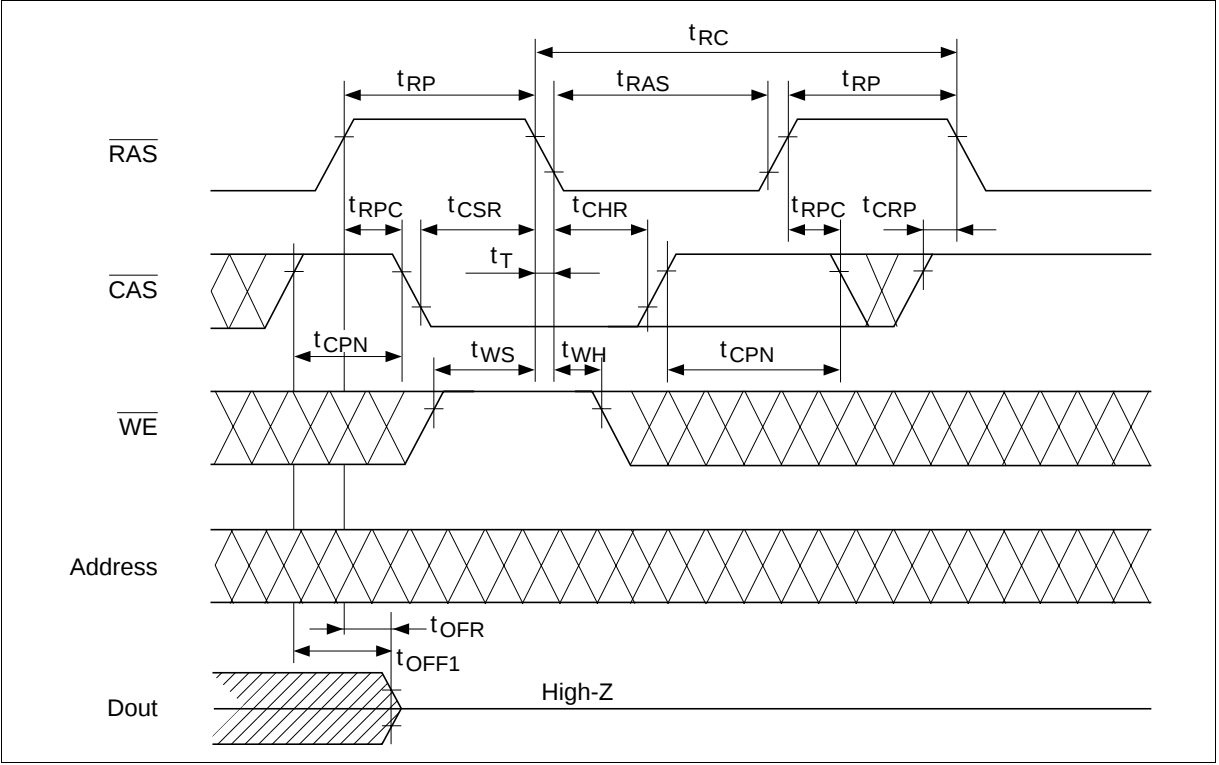


Test Mode Set Cycle

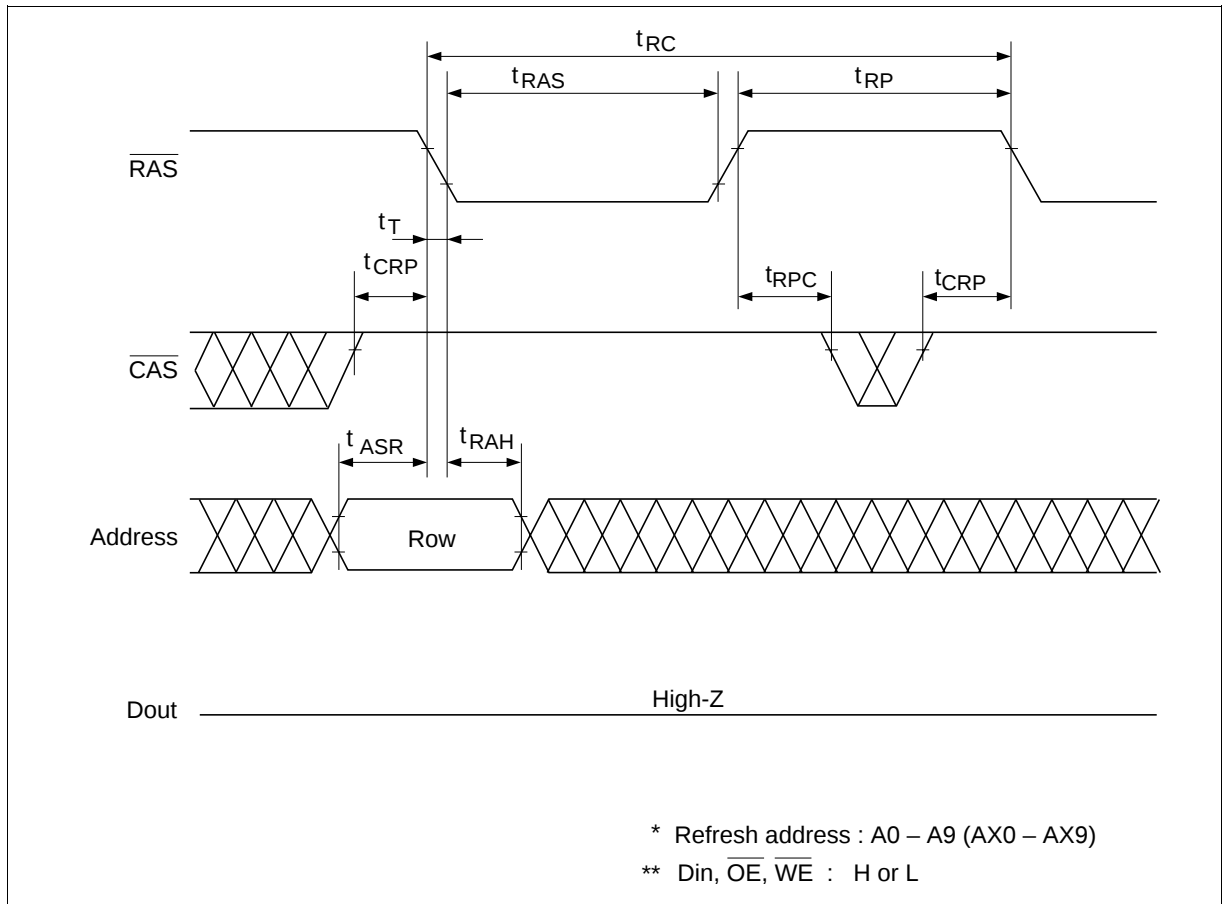
$\overline{\text{WE}}$ -and- $\overline{\text{CAS}}$ -Before $\overline{\text{RAS}}$ -Refresh Cycle



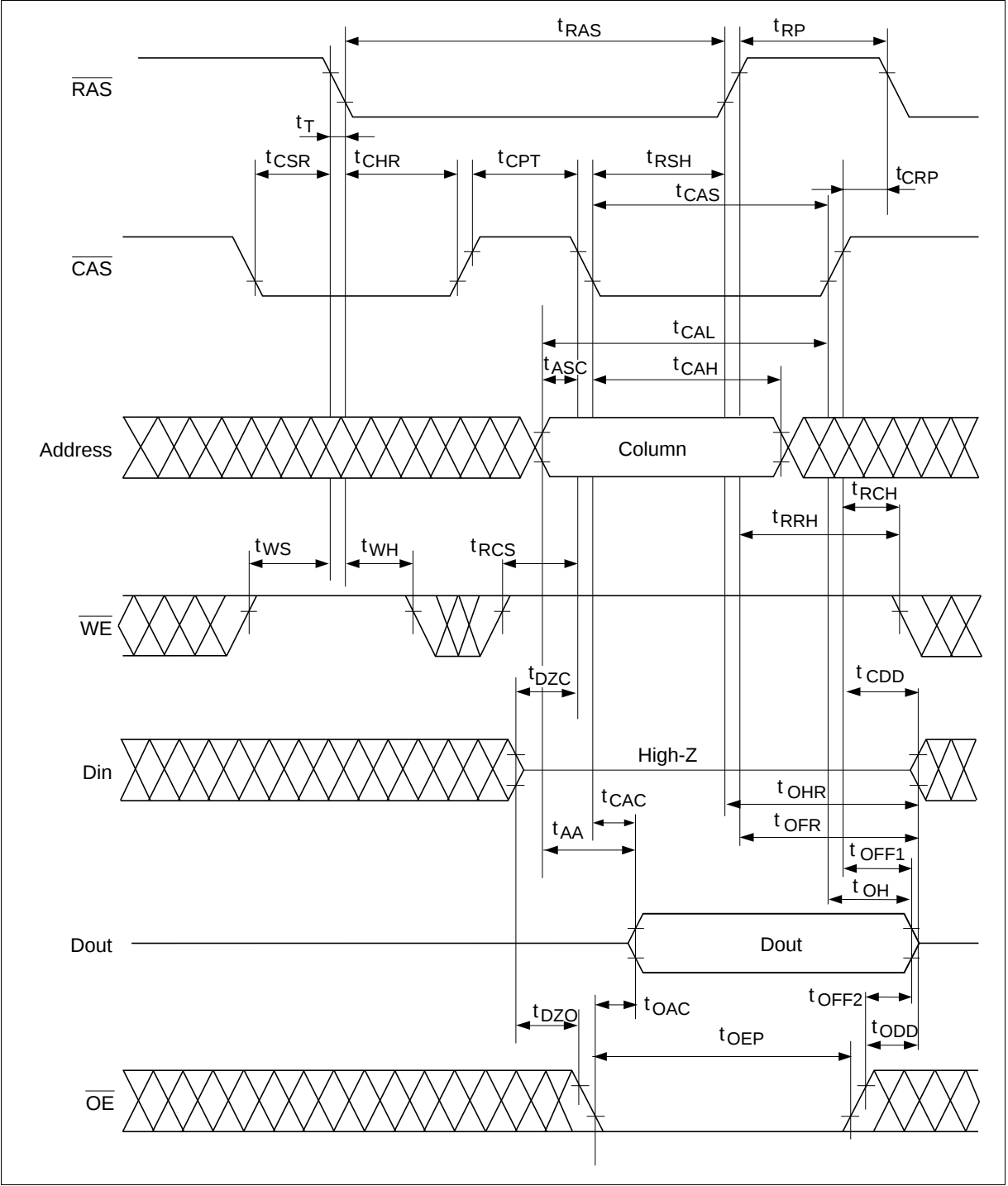
CAS-Before-RAS Refresh Cycle



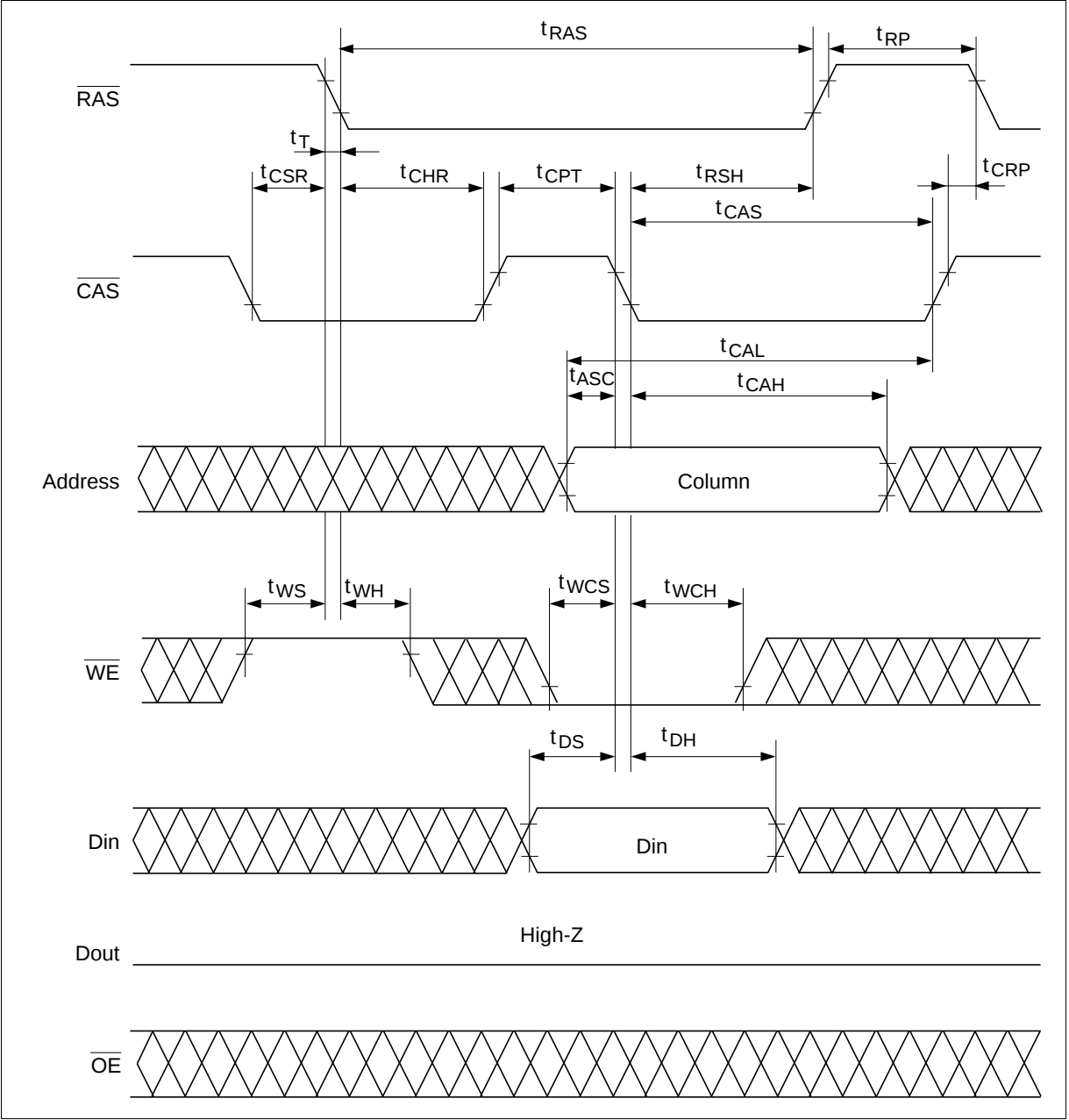
RAS-Only Refresh Cycle



CAS-Before-RAS Refresh Counter Check Cycle (Read)



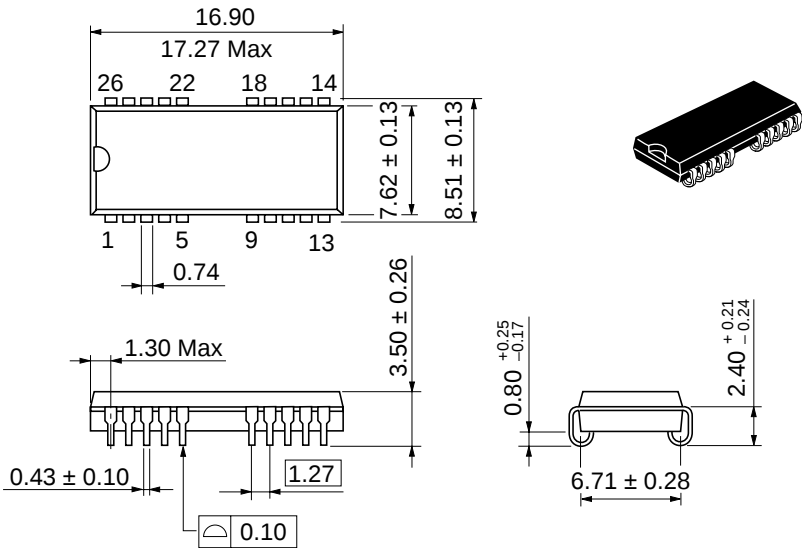
CAS-Before-RAS Refresh Counter Check Cycle (Write)



Package Dimensions

HM514405CS Series (CP-26/20D)

Unit: mm



HM514405CTT Series (TTP-26/20D)

Unit: mm

