

Fast Transient Response, Low Input Voltage, Very Low Dropout Linear Regulator Controller

FEATURES

- Fast Transient Response Optimized with Ceramic Output Capacitors
- FET $R_{DS(ON)}$ Defines Dropout Voltage
- $\pm 1\%$ Reference Tolerance Over Temperature
- Multifunction LDO Shutdown Pin with Latchoff
- Fixed Frequency 1.4MHz Boost Converter Generates MOSFET Gate Drive
- Internally Compensated Current Mode PWM
- Boost Converter Uses Tiny Capacitors and Inductor
- Independent Boost Converter Shutdown Control Permits LDO Output Voltage Supply Sequencing
- 16-Lead SSOP Package

APPLICATIONS

- Microprocessor, ASIC and I/O Supplies
- Very Low Dropout Input-to-Output Conversion
- Logic Termination Supplies

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DESCRIPTION

August 2002

The LT[®]3150 drives a low cost external N-channel MOSFET as a source follower to produce a fast transient response, very low dropout voltage linear regulator. Selection of the N-channel MOSFET $R_{DS(ON)}$ allows dropout voltages below 300mV for low V_{IN} to low V_{OUT} applications.

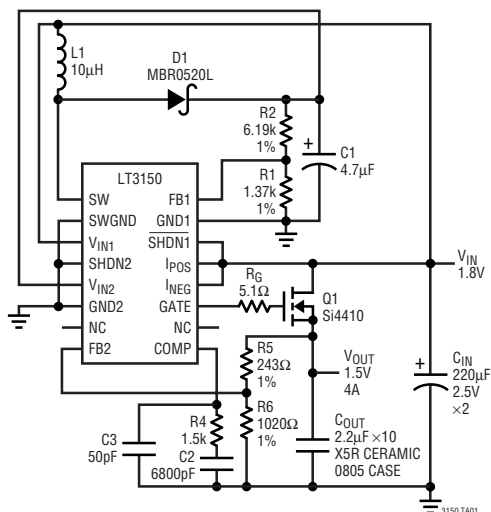
The LT3150 includes a fixed frequency boost regulator that generates gate drive for the N-channel MOSFET. The internally compensated current mode PWM architecture combined with the 1.4MHz switching frequency permits the use of tiny, low cost capacitors and inductors.

The LT3150's transient load performance is optimized with ceramic output capacitors. A precision 1.21V reference accommodates low voltage supplies.

Protection includes a high side current limit amplifier that activates a fault timer circuit. A multifunction shutdown pin provides either current limit time-out with latchoff, overvoltage protection or thermal shutdown. Independent shutdown control of the boost converter provides on/off and sequencing control of the LDO output voltage.

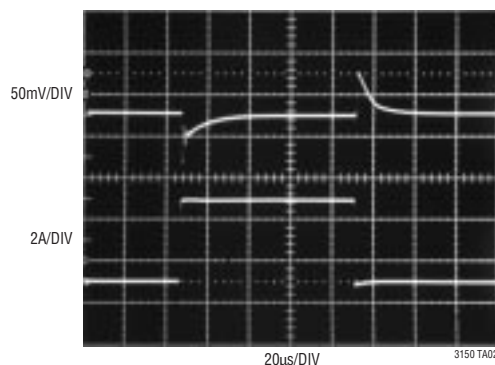
TYPICAL APPLICATION

1.8V to 1.5V, 4A Very Low Dropout Linear Regulator
(Typical Dropout Voltage = 65mV at $I_{OUT} = 4A$)



C_{IN}: PANASONIC SP SERIES EEFUE0E221R 20%
C1: AVX TAJA475M020R 20V 20%
L1: MURATA LQH32CN100K11 OR SUMIDA CDRH3D16100

**Transient Response for
0.1A to 4A Output Load Step**



ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1} , $\overline{SHDN1}$ Voltage	10V
SW Voltage	-0.4V to 36V
FB1 Voltage	$V_{IN1} + 0.3V$
Current into FB1, FB2 Pin	$\pm 1mA$
V_{IN2} , I_{POS} , I_{NEG}	22V
$\overline{SHDN2}$	V_{IN2}
Operating Ambient Temperature Range	0°C to 70°C
Junction Temperature (Note 2)	125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

		ORDER PART NUMBER
		LT3150CGN
		GN PART MARKING
		3150

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{IN1} = 1.5V$, $V_{\overline{SHDN1}} = V_{IN1}$, $V_{IN2} = 12V$, $GATE = 6V$, $I_{POS} = I_{NEG} = 5V$, $V_{\overline{SHDN2}} = 0.75V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Boost Switching Regulator						
	V_{IN1} Minimum Operating Voltage			0.9	1.1	V
	V_{IN1} Maximum Operating Voltage				10	V
V_{FB1}	FB1 Reference Voltage		● 1.20	1.23	1.255	V
	FB1 Input Bias Current	Current Flows into Pin	●	27	80	nA
I_{Q1}	V_{IN1} Quiescent Current	$V_{\overline{SHDN1}} = 1.5V$		3	4.5	mA
	V_{IN1} Quiescent Current in Shutdown	$V_{\overline{SHDN1}} = 0V$, $V_{IN1} = 2V$ $V_{\overline{SHDN1}} = 0V$, $V_{IN1} = 5V$		0.01 0.01	0.5 1.0	μA μA
	FB1 Reference Line Regulation	$1.5V \leq V_{IN1} \leq 10V$		0.02	0.2	%/V
	Switching Frequency		● 1	1.4	1.9	MHz
	Maximum Duty Cycle		● 82	86		%
	Switch Current Limit	(Note 3)		550	800	mA
	Switch V_{CESAT}	$I_{SW} = 300mA$		300	350	mV
	Switch Leakage Current	$V_{SW} = 5V$		0.01	1	μA
	$\overline{SHDN1}$ Input Voltage High		1			V
	$\overline{SHDN1}$ Input Voltage Low				0.3	V
	$\overline{SHDN1}$ Input Bias Current	$V_{\overline{SHDN1}} = 3V$, Current Flows into Pin $V_{\overline{SHDN1}} = 0V$, Current Flows into Pin		25 0.01	50 0.1	μA μA
Linear Regulator Controller						
I_{Q2}	V_{IN2} Quiescent Current		● 5	12	19	mA
V_{FB2}	FB2 Reference Voltage		● 1.203 1.198	1.210 1.210	1.217 1.222	V V
	FB2 Line Regulation	$10V \leq V_{IN2} \leq 20V$	●	0.01	0.03	%/V
	FB2 Input Bias Current	$FB2 = V_{FB2}$, Current Flows out of Pin	●	-0.6	-4	μA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.
 $V_{IN1} = 1.5\text{V}$, $V_{SHDN1} = V_{IN1}$, $V_{IN2} = 12\text{V}$, $GATE = 6\text{V}$, $I_{POS} = I_{NEG} = 5\text{mA}$, $V_{SHDN2} = 0.75\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{GATE} = 3\text{V to } 10\text{V}$	●	69	84		dB
V_{OL}	GATE Output Swing Low (Note 4)	$I_{GATE} = 0\text{mA}$	●		2.5	3	V
V_{OH}	GATE Output Swing High	$I_{GATE} = 0\text{mA}$	●	$V_{IN2} - 1.6$	$V_{IN2} - 1$		V
	$I_{POS} + I_{NEG}$ Supply Current	$3\text{V} \leq I_{POS} \leq 20\text{V}$	●	0.3	0.625	1	mA
	Current Limit Threshold Voltage		●	42	50	58	mV
			●	37	50	63	mV
	Current Limit Threshold Voltage Line Regulation	$3\text{V} \leq I_{POS} \leq 20\text{V}$	●		-0.20	-0.50	%/V
	SHDN2 Sink Current	Current Flows Into Pin	●	2.5	5.0	8.0	μA
	SHDN2 Source Current	Current Flows Out of Pin	●	-8	-15	-23	μA
	SHDN2 Low Clamp Voltage		●		0.1	0.25	V
	SHDN2 High Clamp Voltage		●	1.50	1.85	2.20	V
	SHDN2 Threshold Voltage		●	1.18	1.21	1.240	V
	SHDN2 Threshold Hysteresis		●	50	100	150	mV

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \cdot 130^\circ\text{C/W})$$

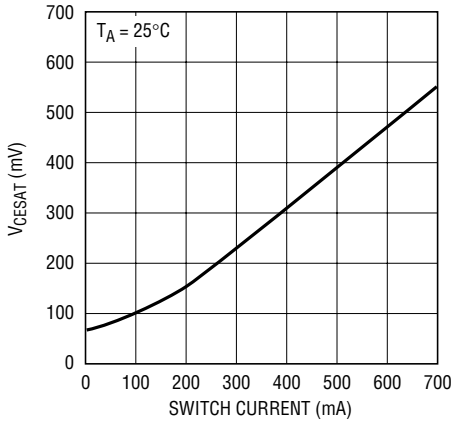
Note 3: Switch current limit is guaranteed by design and/or correlation to static test.

Note 4: The $V_{GS(th)}$ of the external MOSFET must be greater than $3\text{V} - V_{OUT}$.

TYPICAL PERFORMANCE CHARACTERISTICS

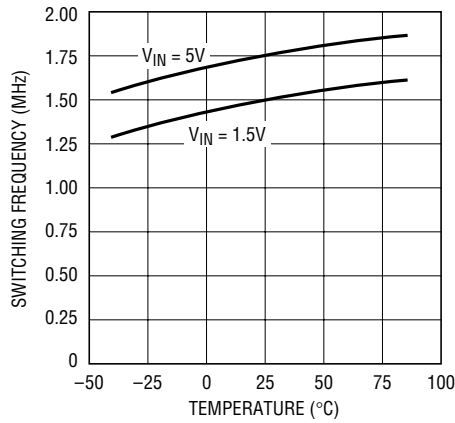
Boost Switching Regulator

Switch V_{CESAT} vs Switch Current



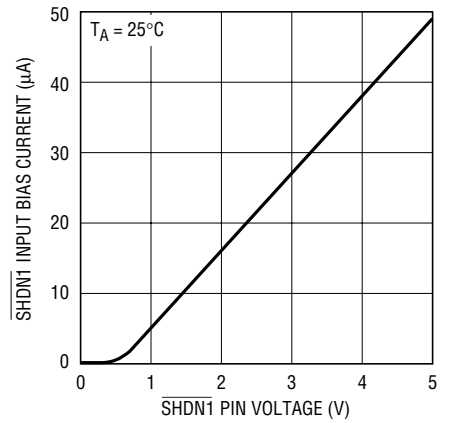
3150 G01

Oscillator Frequency vs Temperature



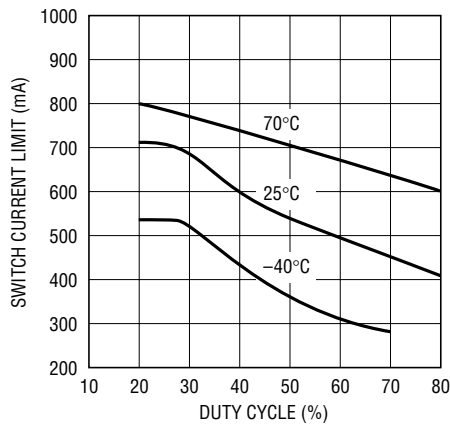
3150 G02

SHDN1 Input Bias Current vs V_{SHDN1}



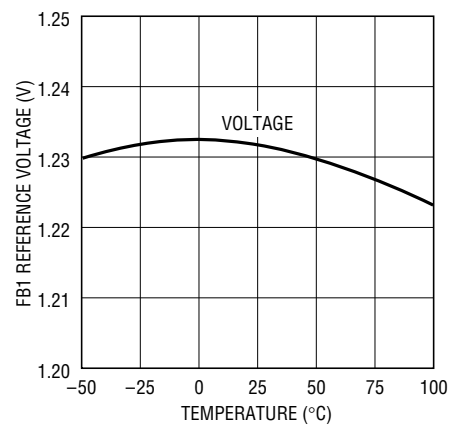
3150 G03

Switch Current Limit vs Duty Cycle



3150 G04

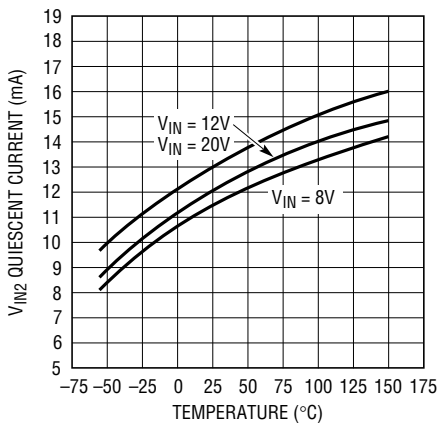
FB1 Reference Voltage vs Temperature



3150 G05

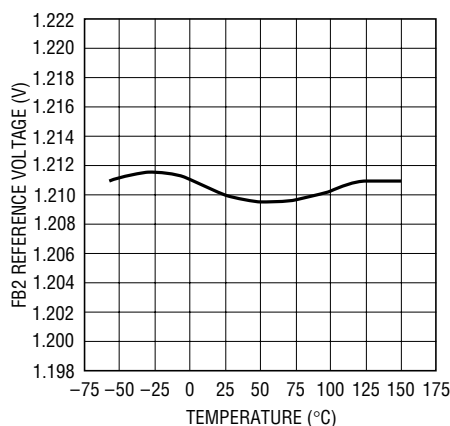
Linear Regulator Controller

V_{IN2} Quiescent Current vs Temperature



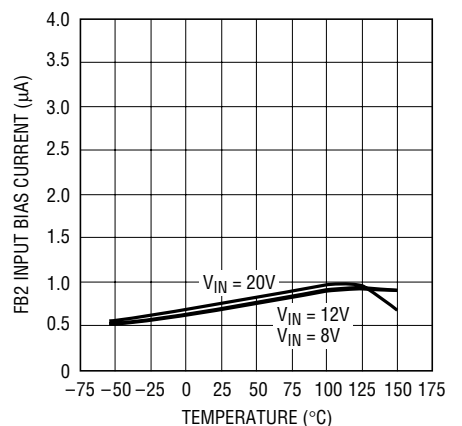
3150 G06

FB2 Reference Voltage vs Temperature



3150 G07

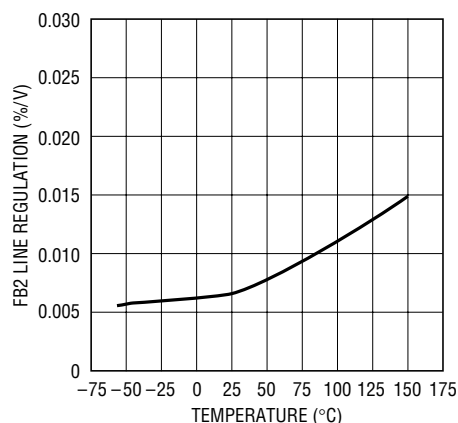
FB2 Input Bias Current vs Temperature



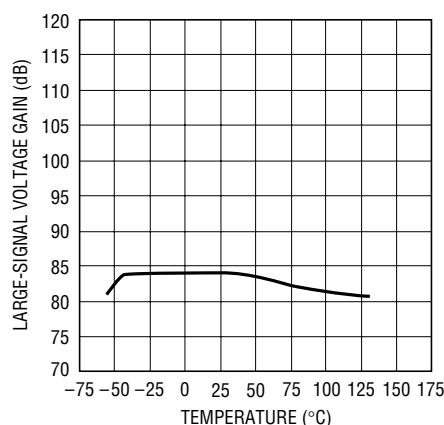
3150 G08

3150i

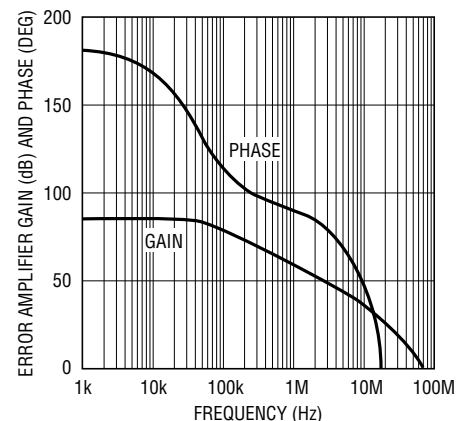
TYPICAL PERFORMANCE CHARACTERISTICS Linear Regulator Controller

FB2 Line Regulation vs Temperature


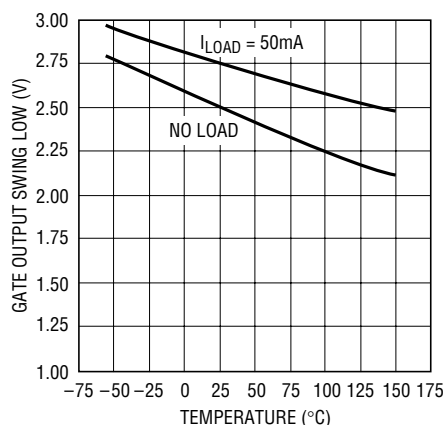
3150 G09

Error Amplifier Large-Signal Voltage Gain vs Temperature


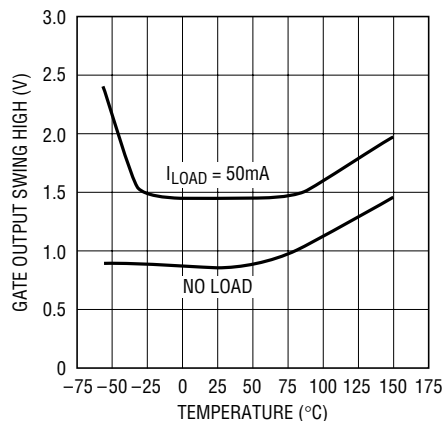
3150 G10

Gain and Phase vs Frequency


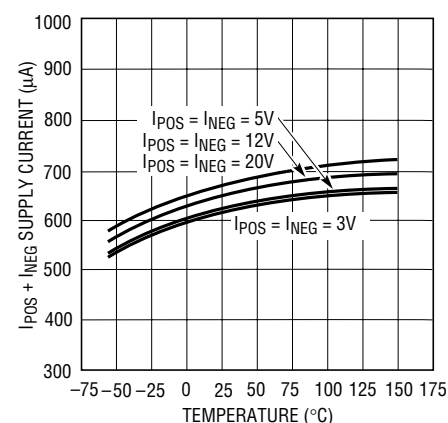
3150 G11

Gate Output Swing Low vs Temperature


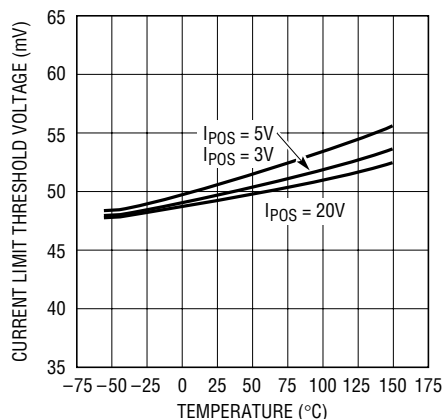
3150 G12

Gate Output Swing High ($V_{IN2} - V_{GATE}$) vs Temperature


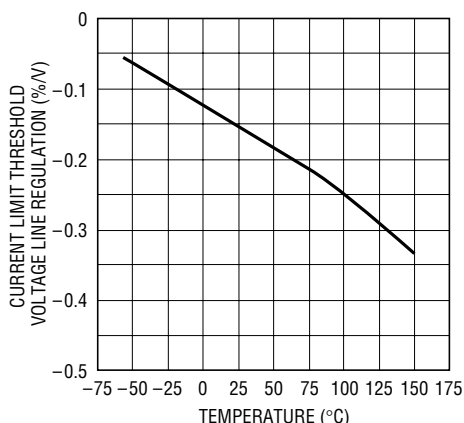
3150 G13

 $I_{POS} + I_{NEG}$ Supply Current vs Temperature


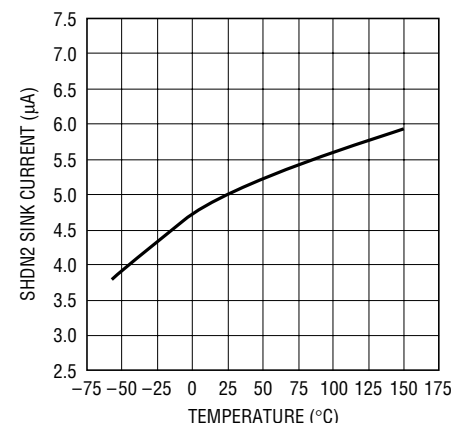
3150 G14

Current Limit Threshold Voltage vs Temperature


3150 G15

Current Limit Threshold Voltage Line Regulation vs Temperature


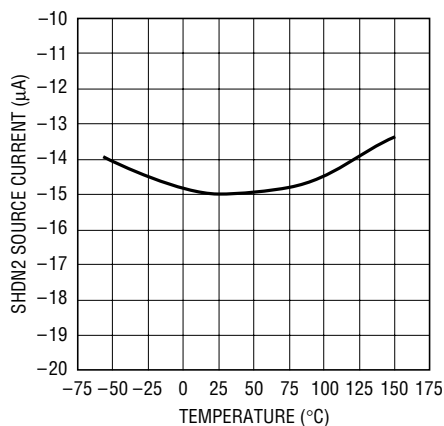
3150 G16

SHDN2 Sink Current vs Temperature


3150 G17

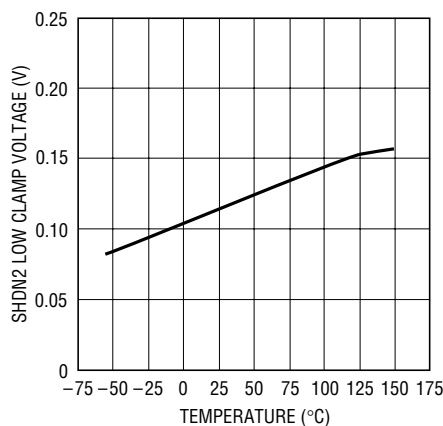
TYPICAL PERFORMANCE CHARACTERISTICS Linear Regulator Controller

SHDN2 Source Current
vs Temperature



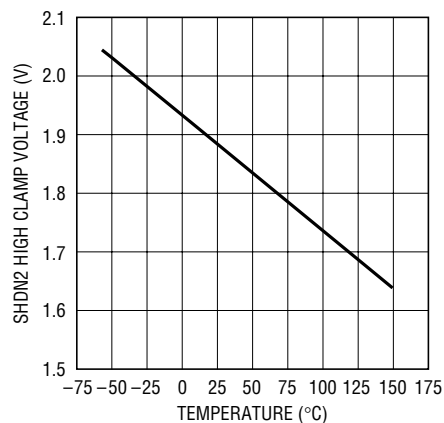
3150 G18

SHDN2 Low Clamp Voltage
vs Temperature



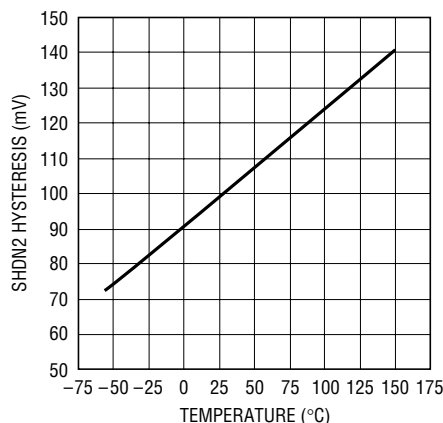
3150 G19

SHDN2 High Clamp Voltage
vs Temperature



3150 G20

SHDN2 Hysteresis vs Temperature



3150 G21

PIN FUNCTIONS

SW (Pin 1): Boost Converter Switch Pin. Connect inductor/diode here. Minimize trace area at this pin to keep EMI down.

SWGND (Pin 2): Switch Ground. Tie directly to the local ground plane and the GNDs at Pins 6 and 15.

V_{IN1} (Pin 3): Boost Converter Input Supply Pin. Must be locally bypassed.

SHDN2 (Pin 4): This is a multifunction shutdown pin that provides GATE drive latchoff capability. A 15μA current source, that turns on when current limit is activated,

charges a capacitor placed in series with SHDN2 to GND and performs a current limit time-out function. The pin is also the input to a comparator referenced to V_{REF} (1.21V). When the pin pulls above V_{REF} , the comparator latches the gate drive to the external MOSFET off. The comparator typically has 100mV of hysteresis and the SHDN2 pin can be pulled low to reset the latchoff function. This pin provides overvoltage protection or thermal shutdown protection when driven from various resistor divider schemes.

PIN FUNCTIONS

V_{IN2} (Pin 5): This is the input supply for the linear regulator control circuitry and provides sufficient gate drive compliance for the external N-channel MOSFET. The maximum operating V_{IN2} is 20V and the minimum operating V_{IN2} is set by V_{OUT} + (V_{GS} of the MOSFET at max I_{OUT}) + 1.6V (worst-case V_{IN2} to GATE output swing).

GND (Pin 6): Analog Ground. This pin is also the negative sense terminal for the internal 1.21V reference. Connect the LDO regulator external feedback divider network and frequency compensation components that terminate to GND directly to this pin for best regulation and performance.

NC (Pins 7, 10): No Connect.

FB2 (Pin 8): This is the inverting input of the error amplifier for the linear regulator. The noninverting input is tied to the internal 1.21V reference. Input bias current for this pin is typically 0.6μA flowing out of the pin. Tie this pin to a resistor divider network to set output voltage. Tie the top of the external resistor divider directly to the output load for best regulation performance.

COMP (Pin 9): This is the high impedance gain node of the error amplifier and is used for external frequency compensation. The transconductance of the error amplifier is 15 millimhos and open-loop voltage gain is typically 84dB. Frequency compensation is generally performed with a series RC + C network to ground.

GATE (Pin 11): This is the output of the error amplifier that drives N-channel MOSFETs with up to 5000pF of “effective” gate capacitance. The typical open-loop output impedance is 2Ω. When using low input capacitance MOSFETs (< 1500pF), a small gate resistor of 2Ω to 10Ω dampens high frequency ringing created by an LC resonance due to the MOSFET gate’s lead inductance and input capacitance. The GATE pin delivers up to 50mA for a few hundred nanoseconds when slewing the gate of the N-channel MOSFET in response to output load current transients.

I_{NEG} (Pin 12): This is the negative sense terminal of the current limit amplifier. A small sense resistor is connected in series with the drain of the external MOSFET and is connected between the I_{POS} and I_{NEG} pins. A 50mV threshold voltage in conjunction with the sense resistor value sets the current limit level. The current sense resistor can be a low value shunt or can be made from a piece of PC board trace. If the current limit amplifier is not used, tie the I_{NEG} pin to I_{POS} to defeat current limit. An alternative is to ground the I_{NEG} pin. This action disables the current limit amplifier and additional internal circuitry activates the timer circuit on the SHDN2 pin if the GATE pin swings to the V_{IN} rail. This option provides the user with a No R_{SENSE}[™] current limit function.

I_{POS} (Pin 13): This is the positive sense terminal of the current limit amplifier. Tie this pin directly to the main input voltage from which the output voltage is regulated.

SHDN1 (Pin 14): Boost Regulator Shutdown Pin. Tie to 1V or more to enable device. Ground to shut down. This pin must not float for proper operation. Connect SHDN1 externally as it does not incorporate an internal pull-up or pull-down.

GND (Pin 15): Boost Converter Analog Ground. This pin is also the negative sense terminal for the FB1 1.23V reference. Connect the external feedback divider network, which sets the V_{IN2} supply voltage and terminates to GND, directly to this pin for best regulation and performance. Also, tie this pin directly to SWGND (Pin 2) and GND (Pin 6).

FB1 (Pin 16): Boost Regulator Feedback Pin. Reference voltage is 1.23V. Connect resistive divider tap here. Minimize trace area at FB1. Set V_{OUT} = V_{IN2} according to V_{OUT} = 1.23V(1 + R1/R2).

No R_{SENSE} is a trademark of Linear Technology Corporation.

The schematic diagram illustrates the internal circuitry of the 3150 RD1. It features an input stage with resistors R1, R2, R3, R4, R5, and R6, and transistors Q1 and Q2. The input signals are VIN1 and VIN2. The output stage includes a comparator A2, a ramp generator, a 1.4MHz oscillator, a flip-flop (FF), a driver, and a transistor Q3. The output is SW. The circuit is powered by VDD1 and GND. The shutdown pin SHDN1 is connected to GND. The circuit is labeled 3150 RD1.

APPLICATIONS INFORMATION

Introduction

With each new generation of computing systems, total power increases while system voltages fall. CPU core, logic and termination supplies below 1.8V are now common. Power supplies must not only regulate low output voltages, but must also operate from low input voltages. A low voltage, very low dropout linear regulator is an attractive conversion option for applications with output current in the range of several amperes. Component count and cost are low in comparison with switching regulator solutions and with low input-to-output differential voltages, efficiencies are comparable.

In addition to low input-to-output voltage conversion, these systems require stringent output voltage regulation. The output voltage specification includes input voltage change, output load current change, temperature change and output load current transient response. Total tolerances as low as $\pm 2\%$ are now required. For a 1.5V output voltage, this amounts to a mere $\pm 30\text{mV}$. Transient load current response is the most critical component as output current can cycle from zero to amps in tens of nanoseconds. These requirements mandate the need for a very accurate, very high speed regulator.

Historically employed solutions include monolithic 3-terminal linear regulators, PNP transistors driven by low cost control circuits and simple buck converter switching regulators. The 3-terminal regulator provides high integration, the PNP driven regulator provides low dropout performance and the switching regulator provides high electrical efficiency.

However, these solutions manifest a common trait of transient response measured in many microseconds. This fact translates to a regulator output decoupling capacitor scheme requiring several hundred microfarads of very low ESR bulk capacitance using multiple capacitors in parallel. This required bulk capacitance is in addition to the ceramic decoupling capacitor network that handles the transient

load response during the first few hundred nanoseconds as well as providing high frequency noise immunity. The combined cost of all capacitors is a significant percentage of the total power supply cost.

The LT3150 controller IC is a unique, easy-to-use device that drives an external N-channel MOSFET as a source follower and realizes an extremely low dropout, ultrafast transient response regulator. The circuit achieves superior regulator bandwidth and transient load performance by eliminating expensive special polymer, tantalum or bulk electrolytic capacitors in the most demanding applications. Performance is optimized around the latest generation of low cost, low ESR, readily available ceramic capacitors. Users benefit directly by saving significant cost as all bulk capacitance is removed. Additional savings include insertion cost, purchasing/inventory cost and board space.

The precision-trimmed adjustable voltage LT3150 accommodates most power supply voltages. Proper selection of the N-channel MOSFET $R_{DS(ON)}$ allows user-settable dropout voltage performance. Transient load step performance is optimized for ceramic output capacitor networks allowing the regulator to respond to transient load changes in a few hundred nanoseconds. The output capacitor network typically consists of multiple $1\mu\text{F}$ to $10\mu\text{F}$ ceramic capacitors in parallel depending on the power supply requirements. The LT3150 also incorporates current limiting, on/off control for power supply sequencing and overvoltage protection or thermal shutdown with simple external components.

The LT3150 combines the benefits of low input voltage operation, very low dropout voltage performance, precision regulation and fast transient response. With low input/output differential voltage applications becoming the norm, an LT3150-based solution is a practical alternative to switching regulators providing comparable efficiency performance at an appreciable cost savings.

APPLICATIONS INFORMATION

Block Diagram Operation

Gate drive for the external N-channel MOSFET in the linear regulator loop is provided by a current mode, internally compensated, fixed frequency step-up switching regulator. Referring to the Block Diagram, Q1 and Q2 form a bandgap reference core whose loop is closed around the output of the regulator. The voltage drop across R5 and R6 is low enough such that Q1 and Q2 do not saturate, even when V_{IN1} is 1V. When there is no load, FB1 rises slightly above 1.23V, causing V_C (the error amplifier's output) to decrease. Comparator A2's output stays high, keeping switch Q3 in the off state. As increased output loading causes the FB1 voltage to decrease, A1's output increases. Switch current is regulated directly on a cycle-by-cycle basis by the V_C node. The flip flop is set at the beginning of each switch cycle, turning on the switch. When the summation of a signal representing switch current and a ramp generator (introduced to avoid subharmonic oscillations at duty factors greater than 50%) exceeds the V_C signal, comparator A2 changes state, resetting the flip flop and turning off the switch. More power is delivered to the output as switch current is increased. The output voltage, attenuated by external resistor divider R1 and R2, appears at the FB1 pin, closing the overall loop. Frequency compensation is provided internally by R_C and C_C . Transient response can be optimized by the addition of a phase lead capacitor C_{PL} in parallel with R1 in applications where large value or low ESR output capacitors are used.

As the load current is decreased, the switch turns on for a shorter period each cycle. If the load current is further decreased, the converter will skip cycles to maintain output voltage regulation.

The linear regulator controller section of the LT3150 Block Diagram consists of a simple feedback control loop and multiple protection functions. Examining the Block Diagram for the LT3150, a start-up circuit provides controlled start-up, including the precision-trimmed bandgap reference, and establishes all internal current and voltage biasing.

Reference voltage accuracy at the FB2 pin is specified as $\pm 0.6\%$ at room temperature and as $\pm 1\%$ over the full operating temperature range. This places the LT3150 among a select group of regulators with a very tightly

specified reference voltage tolerance. The 1.21V reference is tied to the noninverting input of the main error amplifier in the feedback control loop.

The error amplifier consists of a single high gain g_m stage with a transconductance equal to 15 millimhos. The inverting terminal is brought out as the FB2 pin. The g_m stage provides differential-to-single ended conversion at the COMP pin. The output impedance of the g_m stage is about $1M\Omega$ and thus, 84dB of typical DC error amplifier open-loop gain is realized along with a typical 75MHz uncompensated unity-gain crossover frequency. Note that the overall feedback loop's DC gain decreases from the gain provided by the error amplifier by the attenuation factor in the resistor divider network which sets the DC output voltage. External access to the high impedance gain node of the error amplifier permits typical loop compensation to be accomplished with a series RC + C network to ground.

A high speed, high current output stage buffers the COMP node and drives up to 5000pF of "effective" MOSFET gate capacitance with almost no change in load transient performance. The output stage delivers up to 50mA peak when slewing the MOSFET gate in response to load current transients. The typical output impedance of the GATE pin is typically 2Ω . This pushes the pole due to the error amplifier output impedance and the MOSFET input capacitance well beyond the loop crossover frequency. If the capacitance of the MOSFET used is less than 1500pF, it may be necessary to add a small value series gate resistor of 2Ω to 10Ω . This gate resistor helps damp the LC resonance created by the MOSFET gate's lead inductance and input capacitance. In addition, the pole formed by this resistance and the MOSFET input capacitance can be fine tuned.

Because the MOSFET pass transistor is connected as a source follower, the power path gain is much more predictable than designs that employ a discrete PNP transistor as the pass device. This is due to the significant production variations encountered with PNP Beta. MOSFETs are also very high speed devices which enhance the ability to produce a stable wide bandwidth control loop. An additional advantage of the follower topology is inherently good line rejection. Input supply disturbances

APPLICATIONS INFORMATION

do not propagate through to the output. The feedback loop for a regulator circuit is completed by providing an error signal to the FB2 pin. A resistor divider network senses the output voltage and sets the regulated DC bias point. In general, the LT3150 regulator feedback loop permits a loop crossover frequency on the order of 1MHz while maintaining good phase and gain margins. This unity-gain frequency is a factor of 20 to 30 times the bandwidth of currently implemented regulator solutions for microprocessor power supplies. This significant performance benefit is what permits the elimination of all bulk output capacitance.

Several other unique features are included in the design that increase its functionality and robustness. These functions comprise the remainder of the Block Diagram.

A high side sense, current limit amplifier provides active current limiting for the regulator. The current limit amplifier uses an external low value shunt resistor connected in series with the external MOSFET's drain. This resistor can be a discrete shunt resistor or can be manufactured from a Kelvin-sensed section of "free" PC board trace. All load current flows through the MOSFET drain and thus, through the sense resistor. The advantage of using high side current sensing in this topology is that the MOSFET's gain and the main feedback loop's gain remain unaffected. The sense resistor develops a voltage equal to $I_{OUT}(R_{SENSE})$. The current limit amplifier's 50mV threshold voltage is a good compromise between power dissipation in the sense resistor, dropout voltage impact and noise immunity. Current limit activates when the sense resistor voltage equals the 50mV threshold.

Two events occur when current limit activates: the first is that the current limit amplifier drives Q5 in the Block Diagram and clamps the positive swing of the COMP node in the main error amplifier to a voltage that provides an output load current of $50\text{mV}/R_{SENSE}$. This action continues as long as the output current overload persists. The second event is that a timer circuit activates at the SHDN2 pin. This pin is normally held low by a 5 μA active pull-down that limits to $\approx 100\text{mV}$ above ground. When current limit activates, the 5 μA pull-down turns off and a 15 μA pull-up current source turns on. Placing a capacitor in series with

the SHDN2 pin to ground generates a programmable time ramp voltage.

The SHDN2 pin is also the positive input of COMP1. The negative input is tied to the internal 1.21V reference. When the SHDN2 pin ramps above V_{REF} , the comparator drives Q7 and Q8. This action pulls the COMP and GATE pins low and latches the external MOSFET drive off. This condition reduces the MOSFET power dissipation to zero. The time period until the latched-off condition occurs is typically equal to $C_{SHDN2}(1.11\text{V})/15\mu\text{A}$. For example, a 1 μF capacitor on the SHDN2 pin yields a 74ms ramp time. In short, this unique circuit block performs a current limit time-out function that latches off the regulator drive after a pre-defined time period. The time-out period selected is a function of system requirements including start-up and safe operating area. The SHDN2 pin is internally clamped to typically 1.85V by Q9 and R10. The comparator tied to the SHDN2 pin has 100mV of typical hysteresis to provide noise immunity. The hysteresis is especially useful when using the SHDN2 pin for thermal shutdown.

Restoring normal operation after the load current fault is cleared is accomplished in two ways. One option is to recycle the V_{IN2} LT3150 supply voltage as long as an external bleed path for the SHDN2 pin capacitor is provided. The second option is to provide an active reset circuit that pulls the SHDN2 pin below V_{REF} . Pulling the SHDN2 pin below V_{REF} turns off the 15 μA pull-up current source and reactivates the 5 μA pull-down. If the SHDN2 pin is held below V_{REF} during a fault condition, the regulator continues to operate in current limit into a short. This action requires being able to sink 15 μA from the SHDN2 pin at less than 1V. The 5 μA pull-down current source and the 15 μA pull-up current source are designed low enough in value so that an external resistor divider network can drive the SHDN2 pin to provide overvoltage protection or to provide thermal shutdown with the use of a thermistor in the divider network. Diode-ORing these functions together is simple to accomplish and provides multiple functionality for one pin.

If the current limit amplifier is not used, two choices present themselves. The simplest choice is to tie the I_{NEG} pin directly to the I_{POS} pin. This action defeats current limit

APPLICATIONS INFORMATION

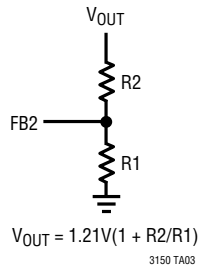
and provides the simplest, no frills circuit. Applications in which the current limit amplifier is not used are where extremely low dropout voltages must be achieved and the 50mV threshold voltage cannot be tolerated.

However, a second available choice permits a user to provide short-circuit protection with no external sensing. This technique is activated by grounding the I_{NEG} pin. This action disables the current limit amplifier because Schottky diode D1 clamps the amplifier's output and prevents Q5 from pulling down the COMP node. In addition, Schottky diode D2 turns off pull-down transistor Q4. Q4 is normally on and holds internal comparator COMP3's output low. This comparator circuit, now enabled, monitors the GATE pin and detects saturation at the positive rail. When a saturated condition is detected, COMP3 activates the shutdown timer. Once the time-out period occurs, the output is shut down and latched off. The operation of resetting the latch remains the same. Note that this technique does not limit the FET current during the time-out period. The output current is only limited by the input power supply and the input/output impedance. Setting the timer to a short period in this mode of operation keeps the external MOSFET within its SOA (safe operating area) boundary and keeps the MOSFET's temperature rise under control.

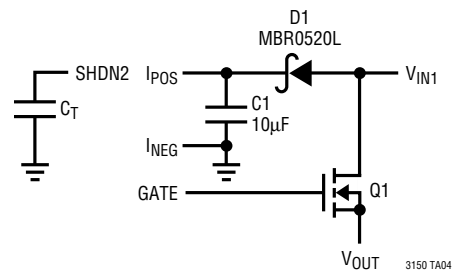
Unique circuit design incorporated into the LT3150 alleviates all concerns about power supply sequencing. The issue of power supply sequencing is an important topic as the typical LT3150 application has two separate power supply inputs, V_{IN1} and V_{IN2} . If the V_{IN2} supply voltage is slow in ramping up or is held off by SHDN1, insufficient MOSFET gate drive exists and therefore, the output voltage does not come up. If V_{IN2} is present, but the V_{IN1} supply voltage tied to the I_{POS} pin is slow in ramping, then the feedback loop wants to drive the GATE pin to the positive V_{IN2} rail. This results in a large current as the V_{IN1} supply ramps up. However, undervoltage lockout circuit COMP2, which monitors the I_{POS} supply voltage, holds Q6 on and pulls the COMP pin low until the I_{POS} voltage increases to greater than the internal 1.21 reference voltage. The undervoltage lockout circuit then smoothly releases the COMP pin and allows the output voltage to come up in dropout from the input supply voltage. An additional benefit derived from the speed of the LT3150 feedback loop is that turn-on overshoot is virtually nonexistent in a properly compensated system.

TYPICAL APPLICATIONS

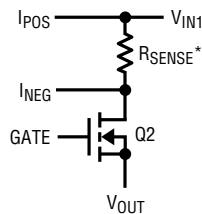
Setting the Linear Regulator Output Voltage



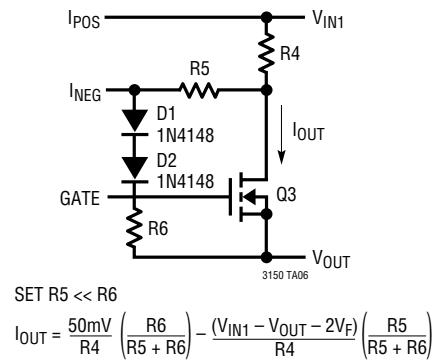
Using No R_{SENSE} Current Limit



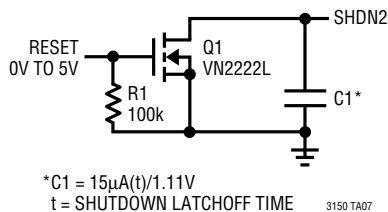
Setting Current Limit



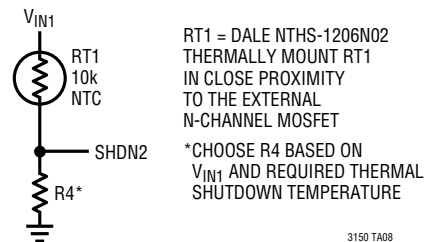
Current Limit with Foldback Limiting Example



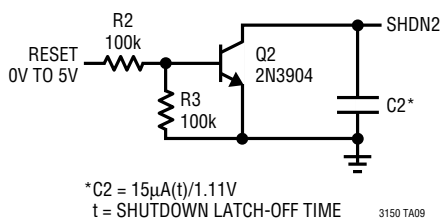
Shutdown Time-Out with Reset



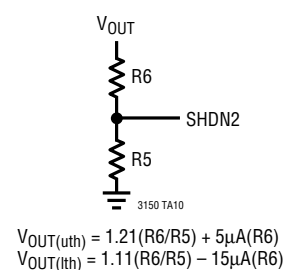
Basic Thermal Shutdown



Shutdown Time-Out with Reset

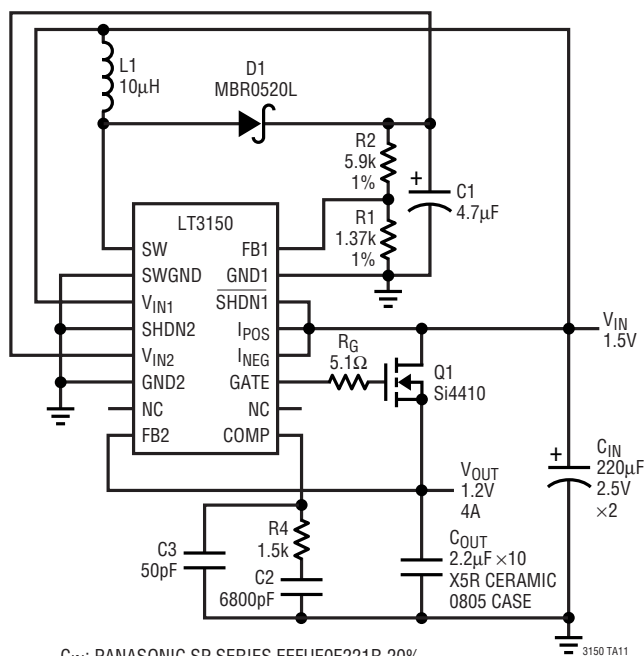


Overvoltage Protection

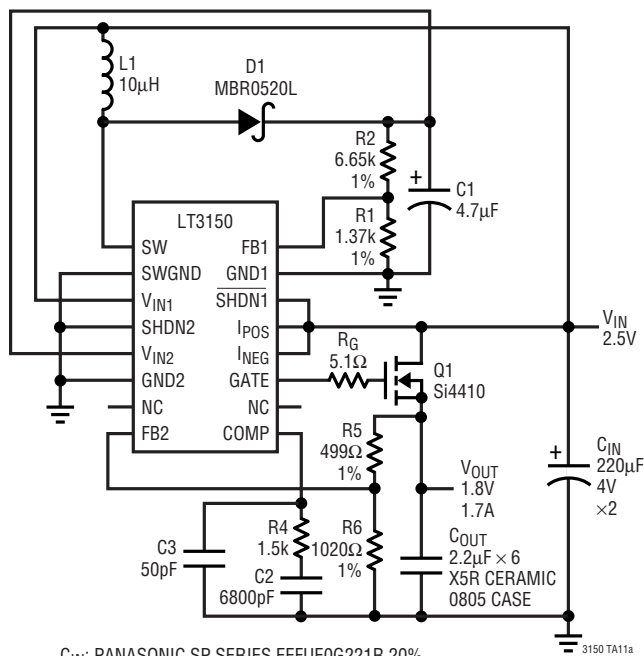


TYPICAL APPLICATIONS

1.5V to 1.2V, 4A Very Low Dropout Linear Regulator

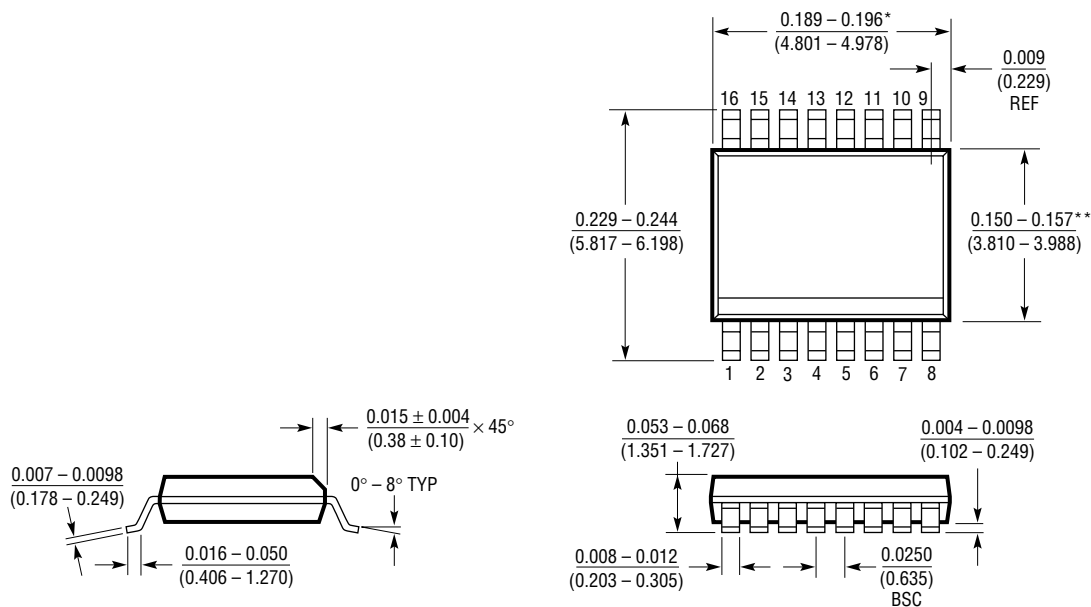


2.5V to 1.8V, 1.7A Low Dropout Linear Regulator



PACKAGE DESCRIPTION

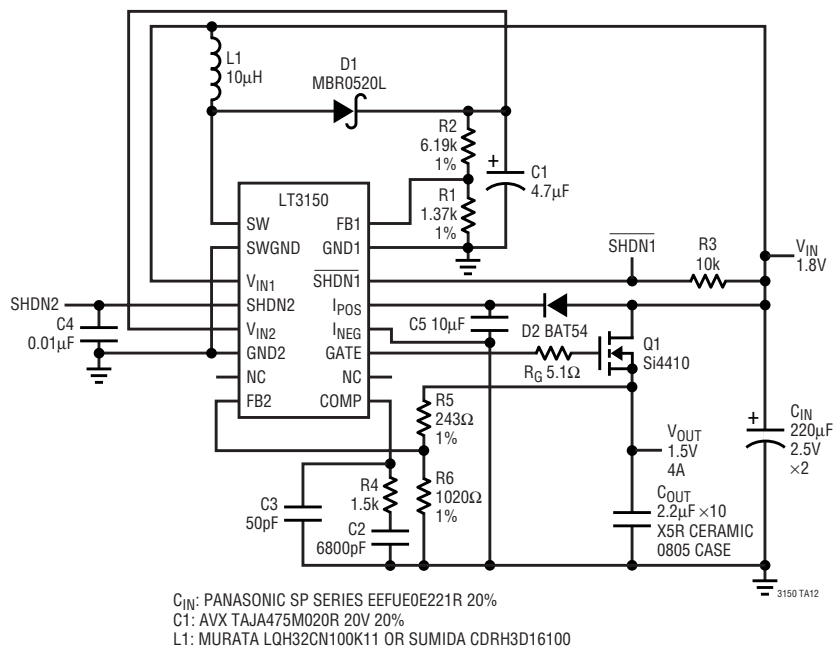
GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



- * DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
- ** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

TYPICAL APPLICATION

1.8V to 1.5V, 4A Very Low Dropout Linear Regulator with No R_{SENSE} Current Limiting and Shutdown

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1573	UltraFast Transient Response Low Dropout Regulator PNP Driver, Up to 5A	$V_{IN} = 2.8V$ to $10V$, $V_{OUT} = 1.265V$, $I_{OUT} = 0.35V$, $I_Q = 1.7mA$, $I_{SD} = 200\mu A$ Requires External PNP Transistor, S8 Package
LT1575/LT1577	UltraFast Transient Response Low Dropout Regulator MOSFET Driver, Up to 10A	$V_{IN} = 1.5V$ to $22V$, $V_{OUT} = 1.21V$, $I_{OUT} = 0.15V$, $I_Q = 12mA$, $I_{SD} = 5\mu A$ LT1577 is Dual Version, N8, S8 Packages
LT1761	100mA, Low Noise Micropower, LDO	$V_{IN} = 1.8V$ to $20V$, $V_{OUT} = 1.22V$, $I_{OUT} = 0.30V$, $I_Q = 20\mu A$, $I_{SD} < 1\mu A$ Low Noise $< 20\mu V_{RMS}$ P-P, Stable with $1\mu F$ Ceramic Capacitors, ThinSOT Package
LT1762	150mA, Low Noise Micropower, LDO	$V_{IN} = 1.8V$ to $20V$, $V_{OUT} = 1.22V$, $I_{OUT} = 0.30V$, $I_Q = 25\mu A$, $I_{SD} < 1\mu A$ Low Noise $< 20\mu V_{RMS}$ P-P, MS8 Package
LT1763	500mA, Low Noise Micropower, LDO	$V_{IN} = 1.8V$ to $20V$, $V_{OUT} = 1.22V$, $I_{OUT} = 0.30V$, $I_Q = 30\mu A$, $I_{SD} < 1\mu A$ Low Noise $< 20\mu V_{RMS}$ P-P, S8 Package
LT1764/LT1764A	3A, Low Noise, Fast Transient Response, LDO	$V_{IN} = 2.7V$ to $20V$, $V_{OUT} = 1.21V$, $I_{OUT} = 0.34V$, $I_Q = 1mA$, $I_{SD} < 1\mu A$ Low Noise $< 40\mu V_{RMS}$ P-P, "A" Version Stable with Ceramic Capacitors, DD, TO220-5 Packages
LT1962	300mA, Low Noise Micropower, LDO	$V_{IN} = 1.8V$ to $20V$, $V_{OUT} = 1.22V$, $I_{OUT} = 0.27V$, $I_Q = 30\mu A$, $I_{SD} < 1\mu A$ Low Noise $< 20\mu V_{RMS}$ P-P, MS8 Package
LT1963/LT1963A	1.5A, Low Noise, Fast Transient Response, LDO	$V_{IN} = 2.1V$ to $20V$, $V_{OUT} = 1.21V$, $I_{OUT} = 0.34V$, $I_Q = 1mA$, $I_{SD} < 1\mu A$ Low Noise $< 40\mu V_{RMS}$ P-P, "A" Version Stable with Ceramic Capacitors DD, TO220-5, SOT-223, S8 Packages
LTC3411	1.25A(I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN} = 2.5V$ to $5.5V$, $I_{OUT} = 1.25A$, $I_Q = 0.8V$, $I_{SD} < 1\mu A$, MS Package
LTC3412	2.5A(I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN} = 2.5V$ to $5.5V$, $I_{OUT} = 2.5A$, $I_Q = 0.8V$, $I_{SD} < 1\mu A$, TSSOP16E Package

3150i