2SK2084Ⓛ , 2SK2084Ⓢ

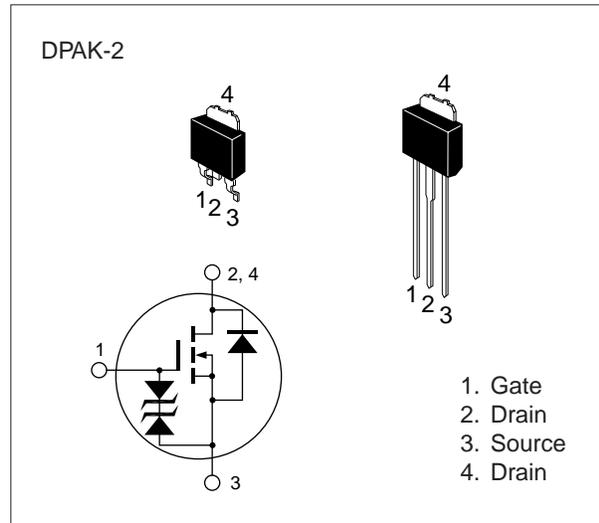**Silicon N Channel MOS FET**

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

DPAK-2

4

1 2 3

4

1 2 3

2, 4

1

3

1. Gate
2. Drain
3. Source
4. Drain

Table 1   Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

*   PW ≤ 10 μs, duty cycle ≤ 1 %
**   Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 10$ mA, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = ±100$ µA, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	µA	$V_{GS} = ±16$ V, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	$V_{DS} = 16$ V, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1$ mA, $V_{DS} = 10$ V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.04	0.053	Ω	$I_D = 4$ A $V_{GS} = 10$ V *
		—	0.058	0.075	Ω	$I_D = 4$ A $V_{GS} = 4$ V *
Forward transfer admittance	$|y_{fs}|$	5	9	—	S	$I_D = 4$ A $V_{DS} = 10$ V *
Input capacitance	Ciss	—	800	—	pF	$V_{DS} = 10$ V
Output capacitance	Coss	—	680	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	165	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	$I_D = 4$ A
Rise time	t_r	—	60	—	ns	$V_{GS} = 10$ V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	$R_L = 5$ Ω
Fall time	t_f	—	80	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 7$ A, $V_{GS} = 0$
Body–drain diode reverse recovery time	t_{rr}	—	80	—	ns	$I_F = 7$ A, $V_{GS} = 0$, diF / dt = 20 A / µs

* Pulse Test

Power vs. Temperature Derating

Channel Dissipation Pch (W) vs. Ambient Temperature Ta (°C)

Maximum Safe Operation Area

Drain Current I D (A) vs. Drain to Source Voltage V DS (V)

10 µs, 100 µs, PW = 10 ms (1shot), 1 ms, DC Operation (Tc = 25 °C)

Operation in this area is limited by R DS(on)

Ta = 25 °C

Typical Output Characteristics

Drain Current I D (A) vs. Drain to Source Voltage V DS (V)

Pulse Test

10 V, 6 V, 4 V, 3.5 V, 3 V, V_{GS} = 2.5 V

Typical Transfer Characteristics

Drain Current I D (A) vs. Gate to Source Voltage V GS (V)

V_{DS} = 10 V
Pulse Test

Tc = 75 °C, 25 °C, −25 °C

Drain to Source Saturation Voltage vs. Gate to Source Voltage

Drain to Source Saturation Voltage $V_{DS(on)}$ (V)

Gate to Source Voltage V_{GS} (V)

Pulse Test

$I_D = 5$ A

2 A

1 A

Static Drain to Source State Resistance vs. Drain Current

Drain to Source On State Resistance $R_{DS(on)}$ (Ω)

Drain Current I_D (A)

Pulse Test

$V_{GS} = 4$ V

10 V

Static Drain to Source on State Resistance vs. Temperature

Static Drain to Source on State Resistance $R_{DS(on)}$ (Ω)

Case Temperature T_C (°C)

Pulse Test

5 A
1 A
2 A

$V_{GS} = 4$ V

1 A
2 A
5 A

10 V

Forward Transfer Admittance vs. Drain Current

Forward Transfer Admittance $|y_{fs}|$ (S)

Drain Current I_D (A)

$V_{DS} = 10$ V
Pulse Test

$T_C = -25$ °C
25 °C
75 °C

Body–Drain Diode Reverse Recovery Time

Reverse Recovery Time t_{rr} (ns)

Reverse Drain Current I_{DR} (A)

di / dt = 20 A / µs

$V_{GS} = 0$, Ta = 25 °C

Typical Capacitance vs. Drain to Source Voltage

Capacitance   C (pF)

Drain to Source Voltage V_{DS} (V)

Ciss

Coss

Crss

$V_{GS} = 0$

f = 1 MHz

Dynamic Input Characteristics

Drain to Source Voltage V_{DS} (V)

Gate to Source Voltage V_{GS} (V)

Gate Charge   Qg (nc)

$V_{DD} = 20$ V

10 V

5 V

V_{GS}

V_{DS}

$I_D = 7$ A

$V_{DD} = 20$ V

10 V

5 V

Switching Characteristics

Switching Time   t (ns)

Drain Current I_D (A)

$t_{d(off)}$

t_f

t_r

$t_{d(on)}$

$V_{GS} = 10$ V

$V_{DD} = 20$ V

PW = 5 µs

duty ≦ 1 %

Reverse Drain Current vs. Souece to Drain Voltage

Pulse Test

Reverse Drain Current I$_{DR}$ (A)

Drain to Source Voltage V$_{DS}$ (V)

10 V

5 V

V$_{GS}$ = 0, −5 V

Normalized Transient Thermal Impedance vs. Pulse Width

Normalized Transient Thermal Impedance γs (t)

Pulse Width PW (S)

Tc = 25°C

D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse

$\theta_{ch-c}(t) = \gamma_s(t) \cdot \theta_{ch-c}$
$\theta_{ch-c} = 6.25\ °C/W,\ Tc = 25\ °C$

P$_{DM}$

PW

T

$D = \dfrac{PW}{T}$

Switching Time Test Circuit

Waveform

Vin Monitor

Vout Monitor

D.U.T.

R_L

Vin
10 V

50Ω

V_{DD}
20 V

Vin — 10%

Vout — 10%

90%

90%

90%

10%

td(on) tr td(off) t_f