

3918590 GENERAL SEMICONDUCTOR

95D 02160 D



**General
Semiconductor
Industries, Inc.**

SQUARE D COMPANY

2N6922, 2N6922A
2N6923, 2N6923A
2N6926, 2N6926A
2N6927, 2N6927A

T-33-13

HIGH POWER NPN *Switch Plus[®] III* TRANSISTORS

These NPN silicon transistors offer an unprecedented combination of speed and ruggedness for use in high speed switching systems. This unique series also features General Semiconductor Industries' planar C²R manufacturing process to provide surface stabilization for high voltage operation and to enhance long term reliability.

- Off-line Power Supplies • Inverters/Converters TO-204AA — 2N6922 (A), 23 (A) }
- Switching Amplifiers • Switching Regulators TO-247 — 2N6926 (A), 27 (A) }

*MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

SYMBOL	DESCRIPTION	2N6922/A	2N6923/A	2N6926/A	2N6927/A	UNIT
V _{CEV}	Collector-Emitter Voltage, Blocking	550/850	550/850	550/850	550/850	Volts
V _{CE(sus)}	Collector-Emitter Voltage, Inductive Switching	450	500	450	500	Volts
V _{CE(sus)}	Collector-Emitter Voltage, Sustaining	400	450	400	450	Volts
V _{EB0}	Emitter Base Voltage	8.0		8.0		Volts
I _C	Collector Current—Continuous/Peak	20/30		20/30		Amps
I _E	Emitter Current—Continuous/Peak	30/40		30/40		Amps
I _B	Base Current—Continuous/Peak	10/15		10/15		Amps
P _D	Total Power Dissipation @ T _C = 25°C	220		125		Watts
T _{oper} T _{stg}	Operating and Storage Junction Temperature Range	- 65 to +200		-55 to +150		°C

*ELECTRICAL CHARACTERISTICS (Applies to all types unless otherwise noted.)

			T _C = 25°C		T _C = 100°C		
SYMBOL	CONDITIONS	PART NO/NOTES	MIN.	MAX.	MIN.	MAX.	UNIT
OFF-STATE							
V _{CE(sus)}	I _C = 50mA	2N6922, 6 (A) 2N6923, 7 (A)	400 450				Volts
I _{CEV}	V _{CE} = Rated V _{CEV} , V _{EB} = 1.5V			1.0			mA
I _{CEV}	V _{CE} = 0.8 Rated V _{CEV} , V _{EB} = 1.5V			10		100	μA
I _{EB0}	V _{EB} = 8.0V			1.0			mA
ON-STATE							
h _{FE}	I _C = 15A, V _{CE} = 2.0V	Pulsed: Notes 1 & 2	8.0				
V _{CE(sus)}	I _C = 15A, I _B = 3.0A			1.0		1.5	Volts
V _{CE(sus)}	I _C = 20A, I _B = 5.0A			2.0			Volts
V _{CE(sus)}	I _C = 30A, I _B = 10A	Pulsed: Notes 1 & 3		5.0			Volts
V _{BE(sus)}	I _C = 15A, I _B = 3.0A	Pulsed: Notes 1 & 2		1.5			Volts
DYNAMIC							
t _f	V _{CE} = 10V, I _C = 1.0A, f = 10MHz		Pulsed: Note 2		15	50	MHz
C _{obo}	V _{CB} = 10V, f = 1.0MHz				200	500	pF
t _d	I _C = 15A I _{B1} = 3.0A	Resistive Load				20	ns
t _r		V _{CC} = V _{CE(sus)}				50	ns
t _{sd} (t _r)	I _C = 15A I _{B1} = 3.0A I _{B2} = 6.0A	Current Source Load	Measured to 10V		1.0		3.0 μs
t _{sv}		Inductive Load			1.0		1.5 μs
t _{rv}					30		40 ns
t _h					30		40 ns
t _c					50		70 ns

THERMAL

R _{θJC}	V _{CE} = 10V, I _C = 10A	2N6922, 3 (A)	0.8			°C/W
R _{θJC}	V _{CE} = 10V, I _C = 5.0A	2N6926, 7 (A)	1.0			°C/W

Notes: 1) Measured using Kelvin connections.

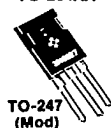
2) Pulse measurement conditions: Length = 300μs. Duty cycle < 2%.

3) Pulse measurement conditions: Length = 10μs. Duty cycle < 2%.

*JEDEC registered data.



TO-204AA

TO-247
(Mod)

NPN

UP TO

850V

V_{CEV}

UP TO

500V

INDUCTIVE

SWITCHING

At Rated Current

20 A

I_C (MAX)

15 A

SWITCHING

35ns

t_c

TYPICAL

Switch Plus[®] III

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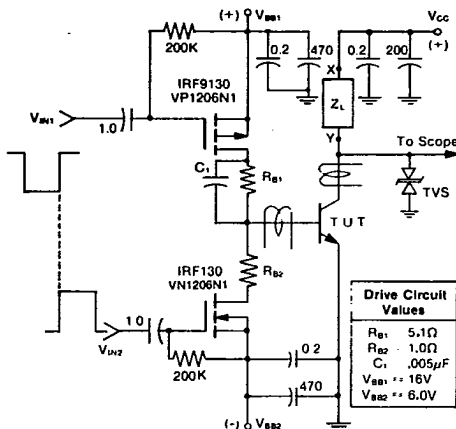
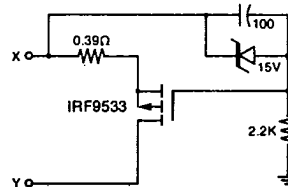


Figure 13—Switching Test Circuit

Notes:

1. Capacitance values in μF .
2. For inductive switching, the Transient Voltage Suppressor (TVS) diode is selected to allow $V_{CE(PK)}$ to equal rated $V_{CE(sus)}$. Since some overshoot caused by circuit inductance and TVS heating is inevitable, the specified TVS breakdown voltage will be about 100 volts less than $V_{CE(sus)}$. Correct voltage may be achieved by stacking TVS diodes and by making minor adjustments in the duty cycle.
3. For resistive switching, R_L is composed of a stack of 2W carbon resistors which may need to be trimmed to obtain the correct I_C . For inductive switching, $I_C \approx T_{ON} V_{CC}/L$. V_{CC} may need minor adjustment to obtain correct I_C . Duty cycle $\leq 1\%$.
4. Proper circuit performance is only achieved by a circuit layout which minimizes lead inductance. The

Load Circuit Values				
Test	$V_{CE(PK)}$	V_{CC}	Z_L	TVS
Resistive				
2N6922, 6	—	450V	30Ω	—
2N6923, 7	—	500V	33Ω	—
Inductive				
2N6922, 6	450V	50V	100μH	2 - SA160CA
2N6923, 7	500V	50V	100μH	2 - SA170CA
Dynamic Saturation	—	50V	Fig. 14	—

Figure 14—Current Source Load (Z_L)

emitter of the T.U.T. must be the ground focal point. To minimize stray coupling, a double sided heavy foil P.C.B. is suggested for the driver stage.

5. View the voltage across power supply lines and adjust bypassing so that ringing is a small percentage of signal levels. Sprague Extralytic[®] and metalized stacked film capacitors are used for supply bypassing.
6. Base current should be viewed with a current probe. C_1 is chosen to achieve an essentially flat topped current pulse. V_{B1} and V_{B2} are adjusted to obtain correct values for the base currents, I_{B1} and I_{B2} .
7. Ground loops through the scope and pulse generator must be avoided. A differential amplifier scope input is often the best solution when a ground loop is encountered.

[®]Registered trademark of Sprague Electric Co.

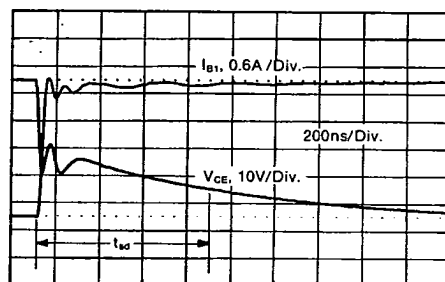


Figure 15—Dynamic Saturation Waveforms

Digitized Waveforms

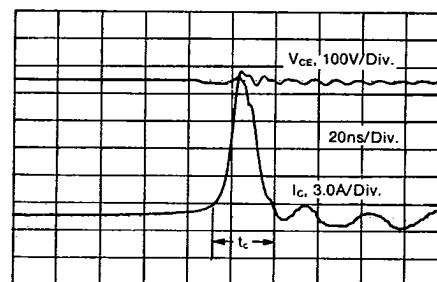


Figure 16—Crossover Waveforms



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INDUCTIVE TURN-OFF CHARACTERISTICS

CROSSOVER TIME

Figure 7—Effect of Collector Current Proportional Drive

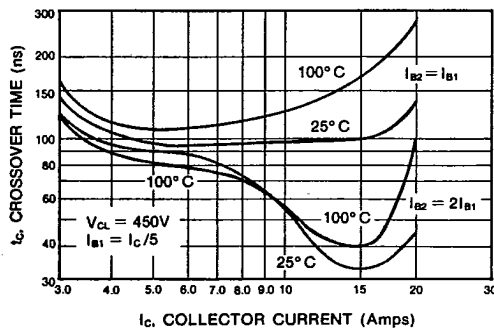


Figure 9—Effect of Collector Current Fixed Drive

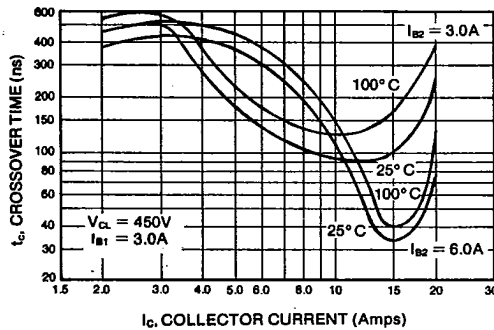
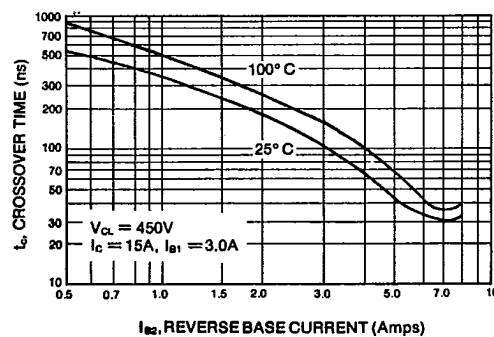


Figure 11—Effect of Reverse Drive



CURRENT FALL TIME

Figure 8—Effect of Collector Current Proportional Drive

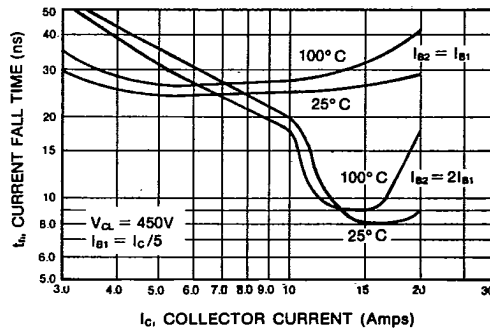


Figure 10—Effect of Collector Current Fixed Drive

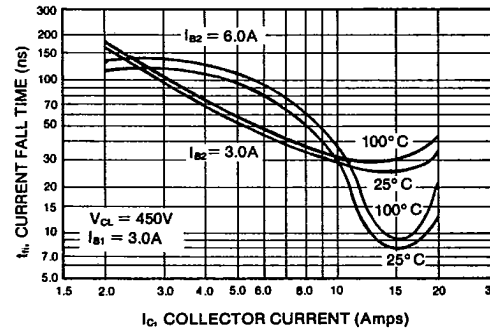
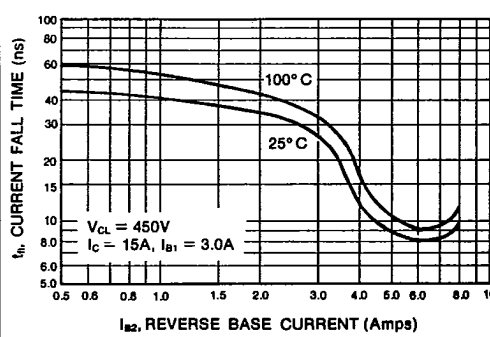


Figure 12—Effect of Reverse Drive



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TURN ON TIME

Figure 1—Rise Time

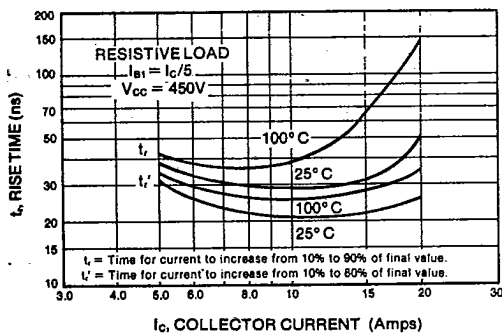
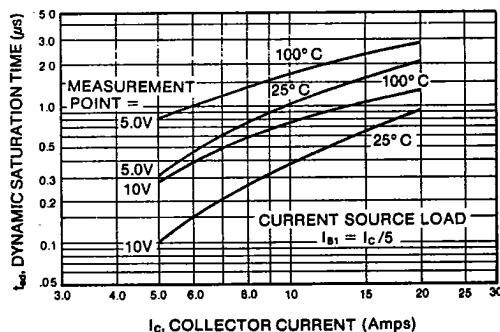


Figure 2—Dynamic Saturation Time



STORAGE TIME

Figure 3—Effect of Collector Current Proportional Drive

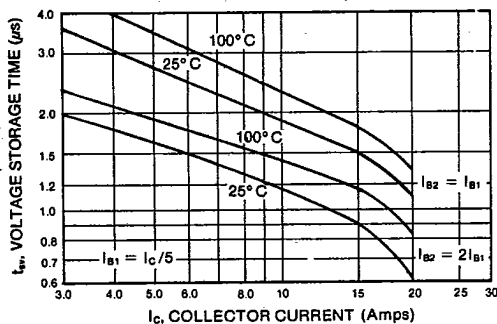


Figure 4—Effect of Collector Current Fixed Drive

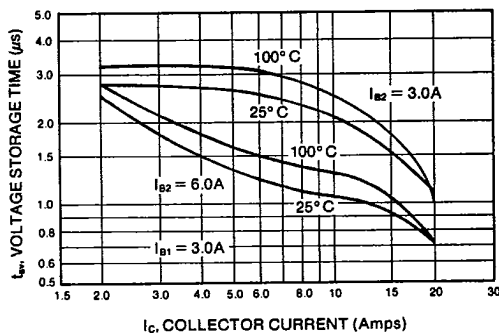


Figure 5—Effect of Pulse Width

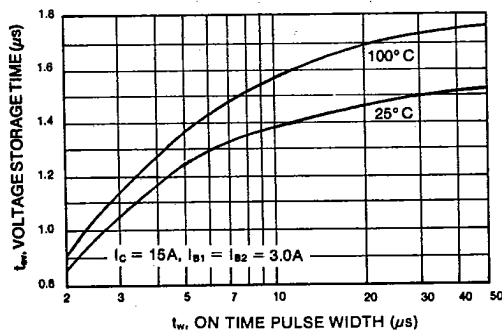
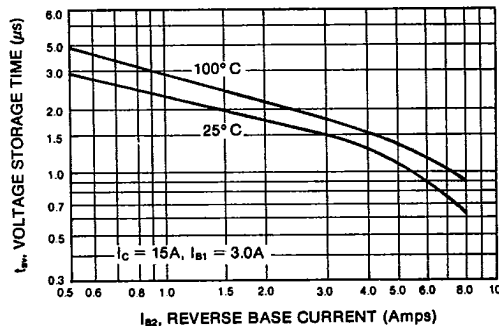


Figure 6—Effect of Reverse Drive



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NPN SWITCHING TRANSISTORS



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TYPICAL DC CHARACTERISTICS & RATINGS

Figure 17—DC Current Gain

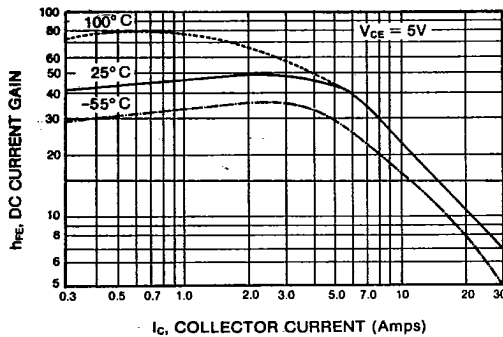


Figure 18—Forward Biased Safe Operating Area

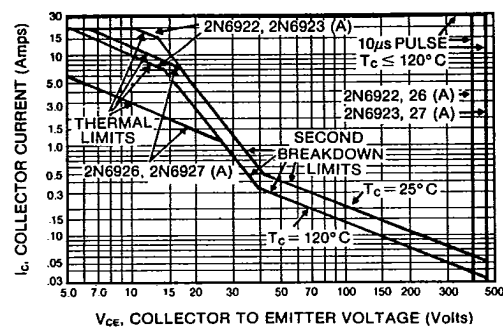


Figure 19—Saturation Voltage

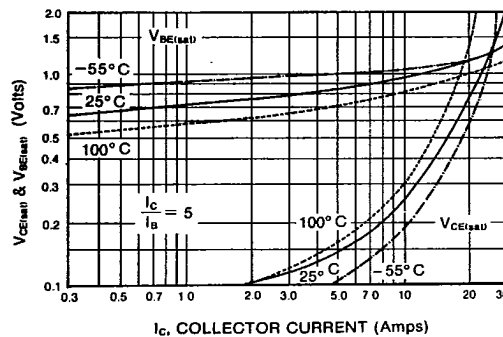


Figure 20—Power Derating

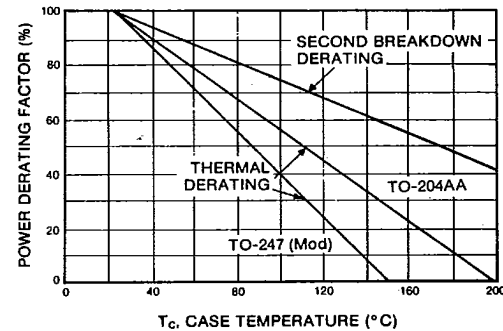


Figure 21—Saturation Region

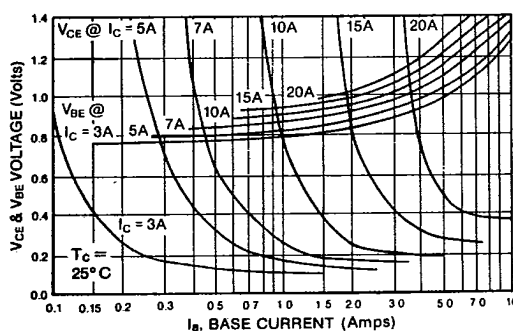
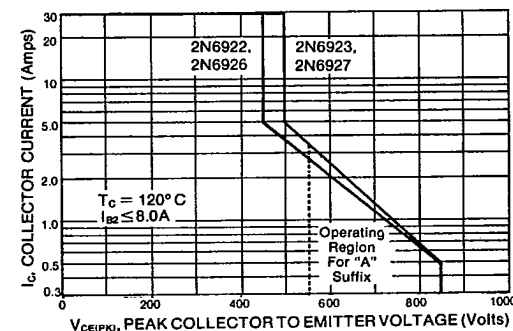


Figure 22—Reverse Bias Safe Operating Area



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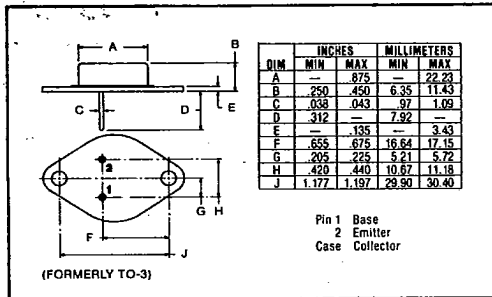
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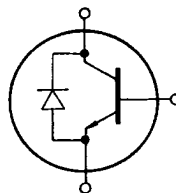
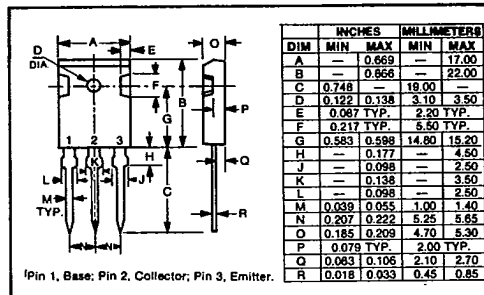
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T-33-13

Package Outline TO-204AA



Package Outline TO-247



Note:

The technology utilized to produce these devices results in an internal diode between the collector and emitter. In some cases this may eliminate the need for an external diode to clamp inductive loads. At 20 A, $t_{in} = 600$ ns and $V_F = 1.25$ V (typical).

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