LTC1592

16-Bit SoftSpan DAC with Programmable Output Range

December 2001

FEATURES

- **Six Programmable Output Ranges**
  Unipolar Mode: 0V to 5V, 0V to 10V
  Bipolar Mode: ±5V, ±10V, ±2.5V, –2.5V to 7.5V
- **1LSB Max DNL and INL Over the Industrial Temperature Range**
- Glitch Impulse < 2nV-s
- 16-Lead SSOP Package
- Power-On Reset to 0V
- Asynchronous Clear to 0V

APPLICATIONS

- Process Control and Industrial Automation
- Precision Instrumentation
- Direct Digital Waveform Generation
- Software-Controlled Gain Adjustment
- Automatic Test Equipment

DESCRIPTION

The LTC®1592 is a serial input 16-bit multiplying current output DAC that operates from a single 5V supply. The SoftSpan™ DAC can be software-programmed for either unipolar or bipolar mode through a 3-wire SPI interface. In either mode, the voltage output range can also be software-programmed. Two output ranges in unipolar mode and four output ranges in bipolar mode are available.

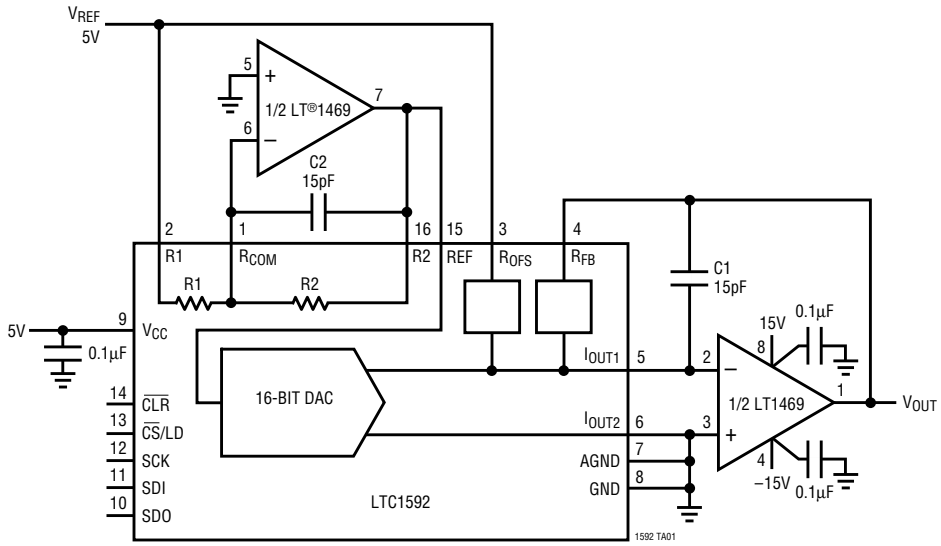
INL and DNL are accurate to 1LSB over the industrial temperature range in both unipolar and bipolar modes. True 16-bit 4-quadrant multiplication is achieved with on-chip four quadrant multiplication resistors. The LTC1592 is available in a 16-lead SSOP package.

The device includes an internal deglitcher circuit that reduces the glitch impulse to less than 2nV-s (typ).

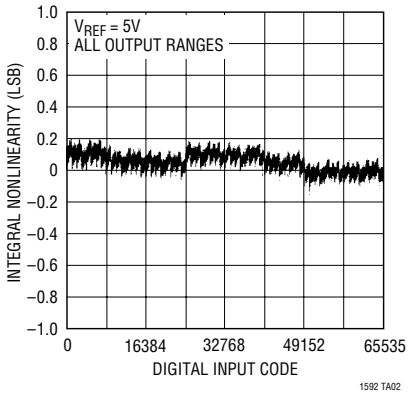
The asynchronous clear pin resets the LTC1592 to 0V in unipolar or bipolar mode.

TYPICAL APPLICATION

Programmable Output Range 16-Bit SoftSpan DAC



LTC1592 Integral Nonlinearity

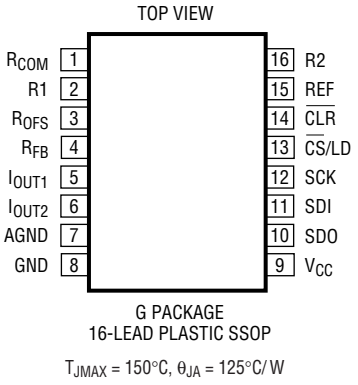


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to AGND, GND ..... –0.3V to 7V
AGND to GND ..... V_{CC} + 0.3V
GND to AGND ..... V_{CC} + 0.3V
R_{COM} to AGND, GND ..... –0.3V to 12V
REF to AGND, GND ..... ±15V
R_{OFS}, R_{FB}, R1, R2 to AGND, GND ..... ±15V
Digital Inputs to AGND, GND ..... –0.3V to (V_{CC} + 0.3V)
I_{OUT1}, I_{OUT2} to AGND, GND ..... –0.3V to (V_{CC} + 0.3V)
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC1592C ..... 0°C to 70°C
LTC1592I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 125°C/ W

ORDER PART NUMBER
LTC1592ACG
LTC1592AIG
LTC1592BCG
LTC1592BIG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V, V_{REF} = 5V, I_{OUT2} = AGND = GND = 0V.

SYMBOL	PARAMETER	CONDITIONS	TEMPERATURE		LTC1592B MIN	LTC1592B TYP	LTC1592B MAX	LTC1592A MIN	LTC1592A TYP	LTC1592A MAX	UNITS
Accuracy											
	Resolution			●	16			16			Bits
INL	Integral Nonlinearity	(Notes 2, 3)	T_A = 25°C				±2		±0.3	±1	LSB
			T_{MIN} to T_{MAX}	●			±2		±0.4	±1	LSB
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 3)	T_{MIN} to T_{MAX}	●			±1		±0.2	±1	LSB
GE	Gain Error	All Output Ranges (Note 3)	T_A = 25°C				±16		–2	±16	LSB
			T_{MIN} to T_{MAX}	●			±24		–3	±16	LSB
BZE	Bipolar Zero Error	All Bipolar Ranges (Note 3)	T_A = 25°C				±10			±5	LSB
			T_{MIN} to T_{MAX}	●			±16			±8	LSB
	Gain Temperature Coefficient	ΔGain/ΔTemperature (Note 4)		●			3		1	3	ppm/°C
I_{LKG}	I_{OUT1} Leakage Current	(Note 5)	T_A = 25°C				±5			±5	nA
			T_{MIN} to T_{MAX}	●			±15			±15	nA
PSRR	Power Supply Rejection	V_{CC} = 5V ±10%		●			±2		±0.2	±2	LSB/V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V$, $V_{REF} = 5V$, $I_{OUT2} = AGND = GND = 0V$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
R_{REF}	DAC Input Resistance (Unipolar)	(Note 6)	●	5	7	10	kΩ
R1, R2	R1, R2 Resistance	(Notes 6, 11)	●	10	14	20	kΩ
R_{OFS}	Offset Resistance (Bipolar)	±5V, ±10V, ±2.5V Ranges –2.5V to 7.5V Range	● ●	10 20	14 28	20 40	kΩ kΩ
R_{FB}	Feedback Resistance (Unipolar)	5V Range 10V Range	● ●	5 10	7 14	10 20	kΩ kΩ
	Feedback Resistance (Bipolar)	±5V and –2.5V to 7.5V Ranges ±10V Range ±2.5V Range	● ● ●	10 20 5	14 28 7	20 40 10	kΩ kΩ kΩ
Analog Outputs (Note 4)							
C_{OUT}	Output Capacitance	DAC Load All 1s DAC Load All 0s			160 100		pF pF
AC Performance (Note 4)							
	Settling Time	5V Range, 0V to 5V Step with LT1468 (Note 7)			2		µs
	Midscale Glitch Impulse	(Note 10)			2		nV-s
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sine Wave			1		mV_{P-P}
THD	Total Harmonic Distortion	(Note 8)			–108		dB
	Output Noise Voltage Density	(Note 9)			11		$nV/\sqrt{Hz}$
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●			±1	µA
C_{IN}	Digital Input Capacitance	V_{IN} = 0V (Note 4)	●			8	pF
Digital Outputs							
V_{OH}	Digital Output High Voltage	I_{OH} = 200µA	●	4			V
V_{OL}	Digital Output Low Voltage	I_{OL} = 1.6mA	●			0.4	V
Timing Characteristics							
t_1	Serial Input Valid to SCK Setup Time		●	60			ns
t_2	Serial Input Valid to SCK Hold Time		●	0			ns
t_3	SCK Pulse Width High		●	35			ns
t_4	SCK Pulse Width Low		●	35			ns
t_5	$\overline{CS}$/LD Pulse High Width		●	360			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	35			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	0			ns
t_8	SCK to SDO Propagation Delay	C_{LOAD} = 50pF	●	20		180	ns
t_9	SCK Low to $\overline{CS}$/LD Low		●	35			ns
t_{10}	Clear Pulse Low Width		●	100			ns
t_{11}	$\overline{CS}$/LD High to SCK Positive Edge		●	35			ns
	SCK Frequency	Non-Daisy Chain (Note 12) Daisy Chain (Note 13)	●			14.2 4.1	MHz MHz

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V$, $V_{REF} = 5V$, $I_{OUT2} = AGND = GND = 0V$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{DD}	Supply Voltage		●	4.5	5	5.5	V
I_{CC}	Supply Current, V_{CC}	Digital Inputs = 0V or V_{CC}	●			10	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: ±1LSB = ±0.0015% of full scale = ±15.3ppm of full scale.

Note 3: Using internal feedback resistor.

Note 4: Guaranteed by design, not subject to test.

Note 5: I_{OUT1} with DAC register loaded to all 0s.

Note 6: Typical temperature coefficient is 100ppm/°C.

Note 7: To 0.0015% for a full-scale change, measured from the falling edge of LD.

Note 8: REF = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s. Output amplifier = LT1468.

Note 9: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant (J/°K); R = resistance (Ω); T = temperature (°K); B = bandwidth (Hz).

Note 10: Midscale transition code 0111 1111 1111 1111 to 1000 0000 0000 0000,

Note 11: R1 and R2 are measured between R1 and R_{COM}, REF and R_{COM}.

Note 12: If a continuous clock is used with data changing on the rising edge of SCK, setup and hold time (t_1, t_2) will limit the maximum clock frequency. If data changes on the falling edge of SCK then the setup time will limit the maximum clock frequency to 8MHz (continues 50% duty cycle clock).

Note 13: SDO propagation delay and SD1 setup time (t_8, t_1) limit the maximum clock frequency for daisy chaining.

PIN FUNCTIONS

R_{COM} (Pin 1): Center Tap Point of the Two Bipolar Resistors R1 and R2. Normally tied to the inverting input of an external amplifier. When these resistors are not used, connect this pin to ground. The maximum voltage on this pin is –0.3V to 12V.

R1 (Pin 2): Bipolar Resistor R1. The main reference input V_{REF}, typically 5V. Accepts up to ±15V. Normally tied to R_{OFS} (Pin 3) and the reference input voltage V_{REF} (5V). When not used connect this pin to ground.

R_{OFS} (Pin 3): Bipolar Offset Network. This pin provides the offset of the output voltage range for bipolar modes. Accepts up to ±15V. Normally tied to R1 and the reference input voltage V_{REF} (5V). Alternatively, this pin may be driven from a different voltage than V_{REF}.

R_{FB} (Pin 4): Feedback Network. Normally tied to the output of the current to voltage converter op amp. Range limited to ±15V.

I_{OUT1} (Pin 5): True DAC Current Output. Tied to the inverting input of the current-to-voltage op amp.

I_{OUT2} (Pin 6): Complement of DAC Current Output. Normally tied to AGND pin.

AGND (Pin 7): Analog Ground. Tie to the system's analog ground plane.

GND (Pin 8): Ground. Tie to the system's analog ground plane.

V_{CC} (Pin 9): Positive Supply Input. $4.5V \leq V_{CC} \geq 5.5V$. Requires a 0.1µF bypass capacitor to ground.

SDO (Pin 10): Serial Data Output. Data at this pin is shifted out on the rising edge of SCK.

SDI (Pin 11): Serial Data Input.

SCK (Pin 12): Serial Interface Clock. Data on the SDI pin is shifted into the input shift register on rising edge of SCK.

$\overline{CS}$/LD (Pin 13): Chip Select Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data into the input shift register. When $\overline{CS}$/LD is pulled high, SCK is disabled and the control logic executes the control word (the first 4 bits of the input data stream as shown in Table 1).

$\overline{CLR}$ (Pin 14): When $\overline{CLR}$ is taken to a logic low, it sets the DAC output to 0V and all internal registers to zero code.

REF (Pin 15): DAC Reference Input. Typically 5V, accepts up to ±15V.

R2 (Pin 16): Bipolar Resistor R2. Normally tied to the DAC reference input REF (Pin 15) and the output of the inverting amplifier tied to R_{COM} (Pin 1).

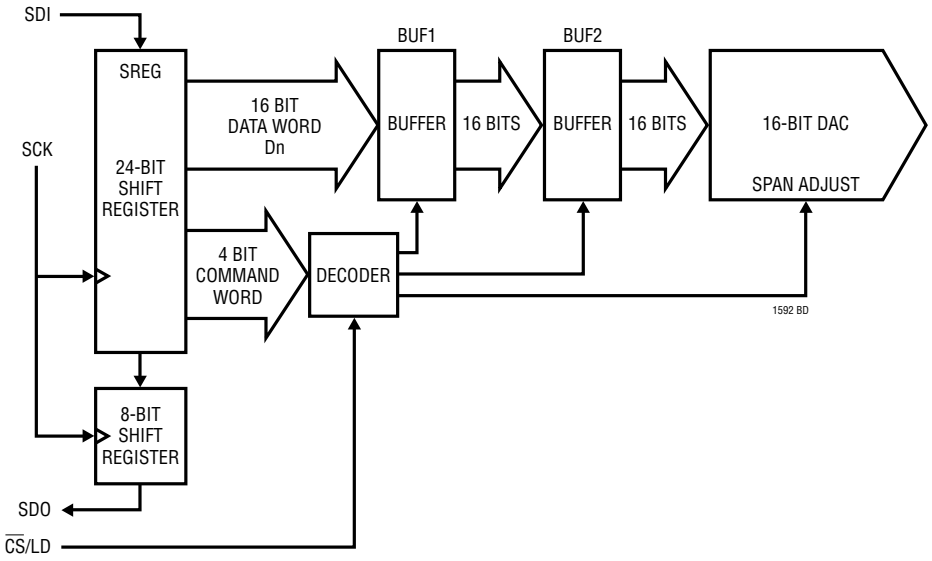
FUNCTION TABLE

Table 1

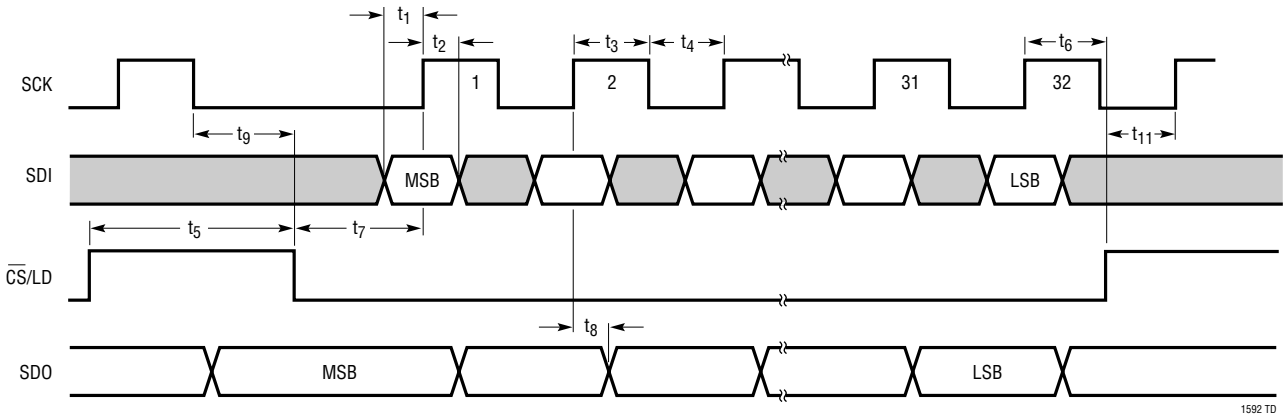
COMMAND				OPERATION EACH COMMAND IS EXECUTED ON THE RISING EDGE OF $\overline{CS}$/LD	Internal Register Status			
					SREG DATA WORD Dn IN INPUT SHIFT REGISTER	BUF1 INPUT BUFFER	BUF2 DAC BUFFER (DAC OUTPUT)	DAC OUTPUT RANGE
C3	C2	C1	C0					
0	0	0	0	Copy Data Word Dn in SReg to Buf1	Dn	Dn	No Change	No Change
0	0	0	1	Copy the Data in Buf1 to Buf2	X	Dn	Dn	No Change
0	0	1	0	Copy Data Word Dn in SReg to Buf1 and Buf2	Dn	Dn	Dn	No Change
0	0	1	1	Reserved (Do Not Use)				
0	1	0	0	Reserved (Do Not Use)				
0	1	0	1	Reserved (Do Not Use)				
0	1	1	0	Reserved (Do Not Use)				
0	1	1	1	Reserved (Do Not Use)				
1	0	0	0	Set Range to 5V. Copy Dn in SReg to Buf1 and Buf2	Dn	Dn	Dn	5V
1	0	0	1	Set Range to 10V. Copy Dn in SReg to Buf1 and Buf2	Dn	Dn	Dn	10V
1	0	1	0	Set Range to ±5V. Copy Dn in SReg to Buf1 and Buf2	Dn	Dn	Dn	±5V
1	0	1	1	Set Range to ±10V. Copy Dn in SReg to Buf1 and Buf2	Dn	Dn	Dn	±10V
1	1	0	0	Set Range to ±2.5V. Copy Dn in SReg to Buf1 and Buf2	Dn	Dn	Dn	±2.5V
1	1	0	1	Set Range to –2.5V to 7V. Copy Dn in SReg to Buf1 and Buf2	Dn	Dn	Dn	–2.5V to 7.5V
1	1	1	0	Reserved (Do Not Use)				
1	1	1	1	No Operation	X	No Change	No Change	No Change

Data Word Dn (n = 0 to 15) is the last 16 bits shifted into the input shift register SReg that corresponds to the DAC code.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Serial Interface

When the $\overline{CS}$/LD is brought to a logic low, the data on the SDI input is loaded into the shift register on the rising edge of the clock. A 4-bit command word (C3 C2 C1 C0), followed by four "don't care" bits and 16 data bits (MSB-first) is the minimum loading sequence required for the LTC1592. When the $\overline{CS}$/LD is brought to a logic high, the clock is disabled internally and the command word is executed.

If no daisy-chaining is required, the input stream can be 24-bit wide as shown in Figure 1. The first four bits are the command word, followed by four "don't care" bits, then a 16-bit data word.

If daisy-chaining is required or the input needs to be written in two 16-bit wide segments, then the input stream must be 32-bit wide and the first 8 bits loaded are "don't care" bits. The remaining bits work the same as a 24-bit stream which is described in the previous paragraph. The output of the internal 32-bit shift register is available on the SDO pin 32 clock cycles later.

Multiple LTC1592s may be daisy-chained together by connecting the SDO pin to the SDI pin of the next IC. The clock and $\overline{CS}$/LD signals should remain common to all ICs in the daisy-chain. The serial data is clocked to all ICs, then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously.

Power-On Reset and Clear

When the power supply is first turned on, the LTC1592 will power up in 5V unipolar mode (C3 C2 C1 C0 = 1000). All the internal registers are set to zeros and the DAC is set to zero code.

The LTC1592 must first be programmed in either unipolar or bipolar mode. There are six operating modes available and can be software-programmed by the command word. When a $\overline{CLR}$ signal is brought to low, it clears all internal registers to zero. The DAC output voltage goes to zero volts. If an update DAC command (C3 C2 C1 C0 = 0001) is issued immediately after the $\overline{CLR}$ signal, the DAC output remains at zero volts.

If a $\overline{CLR}$ signal is given within a 100ns interval immediately after $\overline{CS}$/LD goes high, the user should reload the output range.

OPERATION

Output Range Programming

There are two output ranges available in unipolar mode and four output ranges available in bipolar mode. See Function Table for details. All output ranges are with respect to a 5V input reference. When changing the LTC1592 to a new mode, the command word and data are given at the same time (24 or 32 bit). When $\overline{CS}$/LD goes high, the mode changes and the DAC output goes to a value corresponding to the data code.

Examples:

1. Using a 24-bit loading sequence, load the unipolar range of 0V to 10V with the DAC output at zero volt:
   a) $\overline{CS}$/LD ↓
   b) Clock SDI = 1001 XXXX 0000 0000 0000 0000
   c) $\overline{CS}$/LD ↑; then V_{OUT} = 0V
2. Using a 24-bit loading sequence, load the bipolar range of ±5V and the DAC output at zero volt:
   a) $\overline{CS}$/LD ↓
   b) Clock SDI = 1010 XXXX 1000 0000 0000 0000
   c) $\overline{CS}$/LD ↑; then V_{OUT} = 0V on the ±5V range
3. Using a 32-bit load sequence, load the bipolar range of ±10V with the DAC output voltage at 5V initially. Then change the DAC output to –5V:
   a) $\overline{CS}$/LD ↓
   b) Clock SDI = XXXX XXXX 1011 XXXX 1100 0000 0000 0000
   c) $\overline{CS}$/LD ↑; then V_{OUT} = 5V on the ±10V range

   Next, the bipolar range of ±10V is retained and the DAC output voltage is changed to V_{OUT} = –5V:
   a) $\overline{CS}$/LD ↓
   b) Clock SDI = XXXX XXXX 0010 XXXX 0100 0000 0000 0000
   c) $\overline{CS}$/LD ↑; then V_{OUT} = –5V on the ±10V range

OPERATION

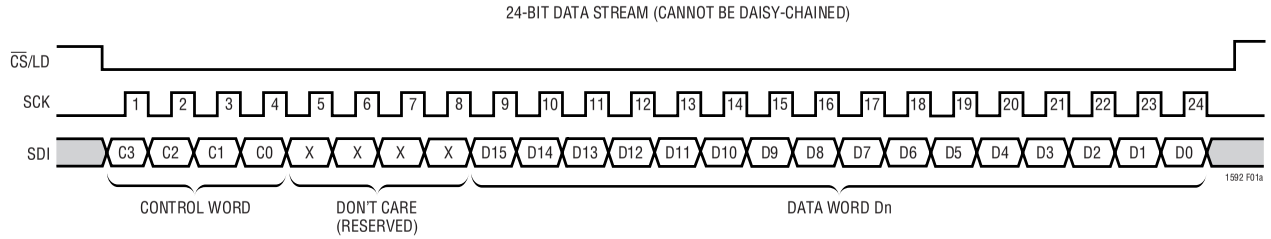


Figure 1a. 24-Bit Load Sequence (Cannot Daisy-Chain Multiple LTC1592s)

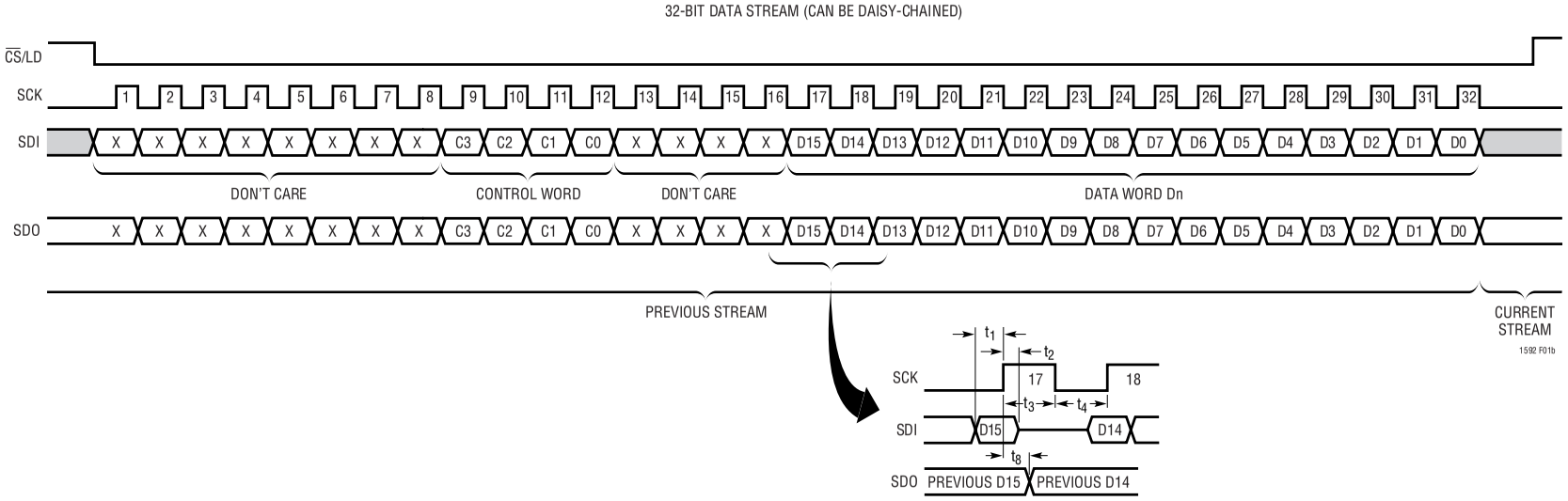


Figure 1b. 32-Bit Load Sequence (for Single and Daisy-Chained LTC1592s)

APPLICATIONS INFORMATION

Op Amp Selection

Because of the extremely high accuracy of the 16-bit LTC1592, careful thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Tables 2 and 3 contain equations for evaluating the effects of op amp parameters on the LTC1592's accuracy when programmed in a unipolar or bipolar output range. These are the changes the op amp can cause to the INL, DNL, unipolar offset, unipolar gain error, bipolar zero and bipolar gain error. Table 4 contains a partial list of LTC precision op amps recommended for use with the LTC1592. The easy-to-use design equations simplify the selection of op amps to meet the system's specified error budget. Select the amplifier from Table 4 and insert the specified op amp parameters in Table 3. Add up all the errors for each category to determine the effect the op amp has on the accuracy of the LTC1592. Arithmetic summation gives an (unlikely) worst-case effect. A root-sum-square (RMS) summation produces a more realistic estimate.

Op amp offset will contribute mostly to output offset and gain error and has minimal effect on INL and DNL. For the LTC1592, a 250µV op amp offset will cause about 0.65LSB INL degradation and 0.15LSB DNL degradation with a 10V full-scale range (20V range in bipolar). For the LTC1592 programmed in a unipolar mode, the same 250µV op amp

Table 2. Variables for Each Output Range That Adjust the Equations in Table 3

OUTPUT RANGE	A1	A2	A3	A4	A5
5V	1.1	2	1		
10V	2.2	3	1.5		
±5V	2	2	1.2	1	1.5
±10V	4	4	1.2	1	2.5
±2.5V	1	1	1.6	1	1
–2.5V to 7.5V	1.9	3	1	0.5	1.5

Table 3. Easy-to-Use Equations Determine Op Amp Effects on DAC Accuracy in All Output Ranges

OP AMP	INL (LSB)	DNL (LSB)	UNIPOLAR OFFSET (LSB)	BIPOLAR ZERO ERROR (LSB)	UNIPOLAR GAIN ERROR (LSB)	BIPOLAR GAIN ERROR (LSB)
V_{OS1} (mV)	$V_{OS1} \bullet 2.4 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 0.6 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 13.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$A3 \bullet V_{OS1} \bullet 19.8 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 13.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 13.2 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B1} (nA)	$I_{B1} \bullet 0.0003 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.00008 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.13 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.01 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0018 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0018 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL1} (V/V)	$A1 \bullet \left(\frac{16.5k}{A_{VOL1}}\right)$	$A2 \bullet \left(\frac{1.5k}{A_{VOL1}}\right)$	0	0	$A3 \bullet \left(\frac{131k}{A_{VOL1}}\right)$	$A5 \bullet \left(\frac{131k}{A_{VOL1}}\right)$
V_{OS2} (mV)	0	0	0	$A4 \bullet \left(V_{OS2} \bullet 13.1 \bullet \left(\frac{5V}{V_{REF}}\right)\right)$	$V_{OS2} \bullet 26.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS2} \bullet 26.2 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B2} (mV)	0	0	0	$A4 \bullet \left(I_{B2} \bullet 0.05 \bullet \left(\frac{5V}{V_{REF}}\right)\right)$	$I_{B2} \bullet 0.1 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B2} \bullet 0.1 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL2} (V/V)	0	0	0	$A4 \bullet \left(\frac{66k}{A_{VOL2}}\right)$	$\left(\frac{131k}{A_{VOL2}}\right)$	$\left(\frac{131k}{A_{VOL2}}\right)$

Table 4. Partial List of LTC Precision Amplifiers Recommended for Use with the LTC1592, with Relevant Specifications

	AMPLIFIER SPECIFICATIONS								
AMPLIFIER	V_{OS} µV	I_B nA	A_{OL} V/mV	VOLTAGE NOISE nV/√Hz	CURRENT NOISE pA/√Hz	SLEW RATE V/µs	GAIN BANDWIDTH PRODUCT MHz	$t_{SETTLING}$ with LTC1592 µs	POWER DISSIPATION mW
LT1001	25	2	800	10	0.12	0.25	0.8	120	46
LT1097	50	0.35	1000	14	0.008	0.2	0.7	120	11
LT1112 (Dual)	60	0.25	1500	14	0.008	0.16	0.75	115	10.5/Op Amp
LT1124 (Dual)	70	20	4000	2.7	0.3	4.5	12.5	19	69/Op Amp
LT1468	75	10	5000	5	0.6	22	90	2.5	117
LT1469 (Dual)	125	10	2000	5	0.6	22	90	2.5	123/Op Amp

APPLICATIONS INFORMATION

offset will cause a 3.3LSB zero-scale error and a 3.3LSB gain error with a 10V full-scale range.

While not directly addressed by the simple equations in Tables 2 and 3, temperature effects can be handled just as easily for unipolar and bipolar applications. First, consult an op amp's data sheet to find the worst-case V_{OS} and I_B over temperature. Then, plug these numbers in the V_{OS} and I_B equations from Table 3 and calculate the temperature induced effects.

For applications where fast settling time is important, Application Note 74, entitled "*Component and Measurement Advances Ensure 16-Bit DAC Settling Time*," offers a thorough discussion of 16-bit DAC settling time and op amp selection.

Precision Voltage Reference Considerations

Much in the same way selecting an operational amplifier for use with the LTC1592 is critical to the performance of the system, selecting a precision voltage reference also requires due diligence. The output voltage of the LTC1592 is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 16-bit applications: output voltage initial tolerance, output voltage temperature coefficient and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LT1236 (±0.05%), minimizes the gain error caused by the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

As precision DAC applications move to 16-bit and higher performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references, like the LT1236, produce low output noise in the 0.1Hz to 10Hz region, well below the 16-bit LSB level in 5V or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.

Table 5. Partial List of LTC Precision References Recommended for Use with the LTC1592, with Relevant Specifications

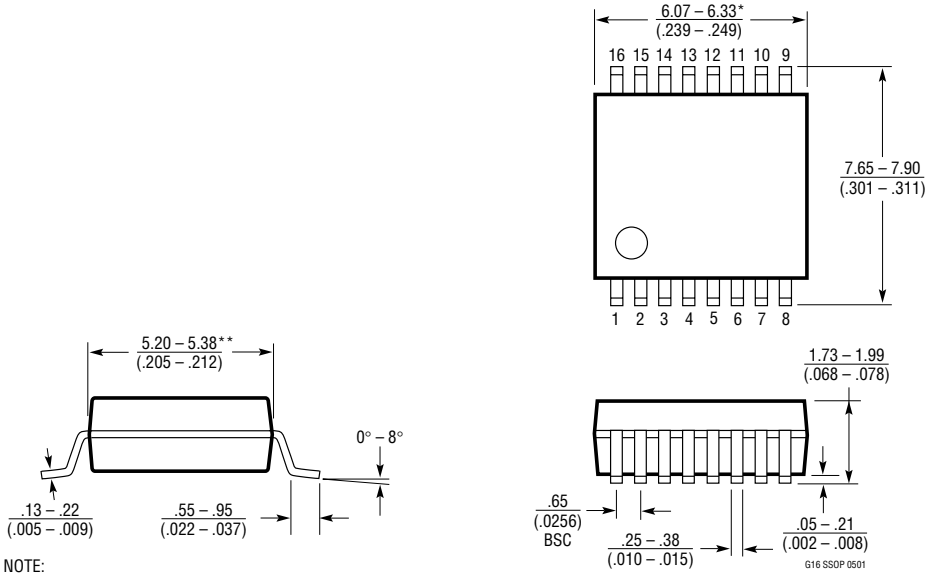
REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz to 10Hz NOISE
LT1019A-5, LT1019A-10	±0.05%	5ppm/°C	$12\mu V_{P-P}$
LT1236A-5, LT1236A-10	±0.05%	5ppm/°C	$3\mu V_{P-P}$
LT1460A-5, LT1460A-10	±0.075%	10ppm/°C	$20\mu V_{P-P}$
LT1790A-2.5	±0.05%	10ppm/°C	$12\mu V_{P-P}$

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding techniques should be used. I_{OUT2} must be tied to the star ground with as low a resistance as possible. When it is not possible to locate star ground close to I_{OUT2}, a low resistance trace should be used to route this pin to star ground. This minimizes the voltage drop from this pin to ground caused by the code dependent current flowing to ground. When the resistance of this circuit board trace becomes greater than 1Ω, a force/sense amplified configuration should be used to drive this pin (see Figure 2). This preserves the excellent accuracy (1LSB INL and DNL) of the LTC1592.

PACKAGE DESCRIPTION

G Package
16-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

TYPICAL APPLICATION

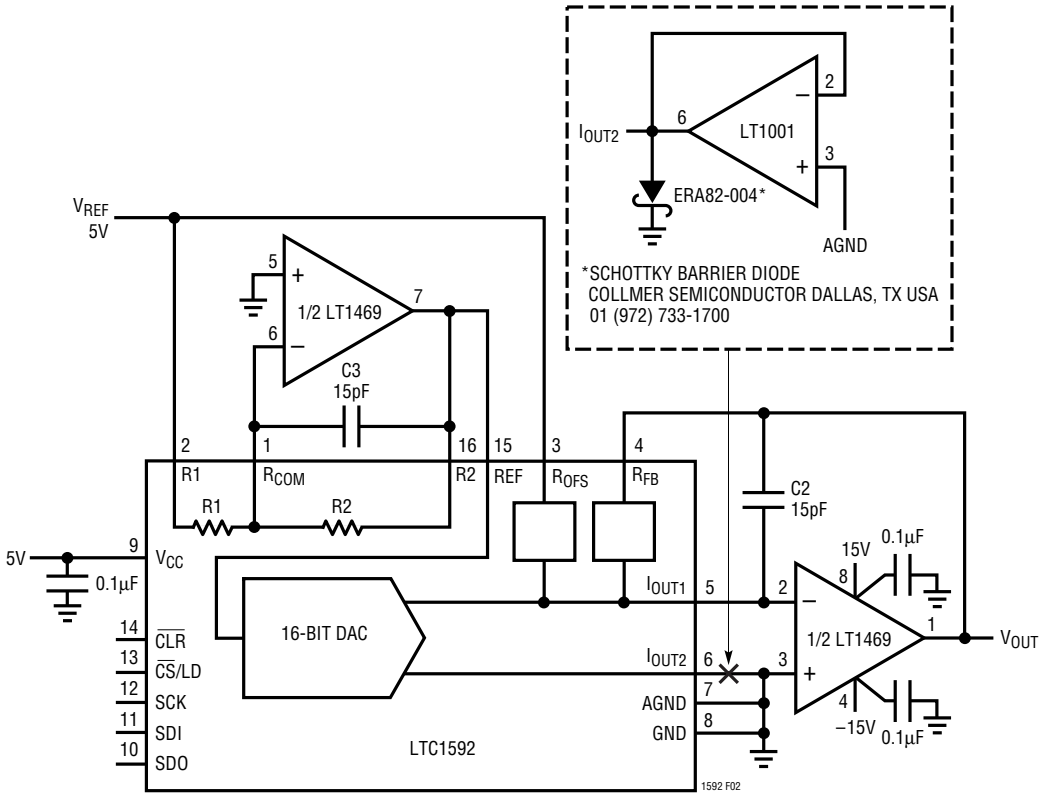


Figure 2. Driving I_{OUT2} from AGND with a Force/Sense Amplifier

PART NUMBER	DESCRIPTION	COMMENTS
LTC1591/LTC1597	Parallel 14-/16-Bit Current Output DACs	On-Chip 4-Quadrant Resistors
LTC1595/LTC1596	Serial 16-Bit Current Output DACs	Low Glitch, ±1LSB Maximum INL, DNL
LTC1599	2-Byte, 16-Bit Current Output DAC	On-Chip 4-Quadrant Resistors
LTC1821	Parallel 16-Bit Voltage Outupt DAC	Precision 16-Bit Settling in 2µs for 10V Step

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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