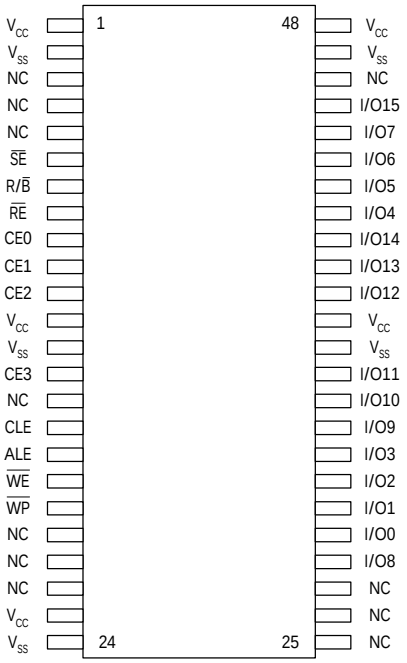
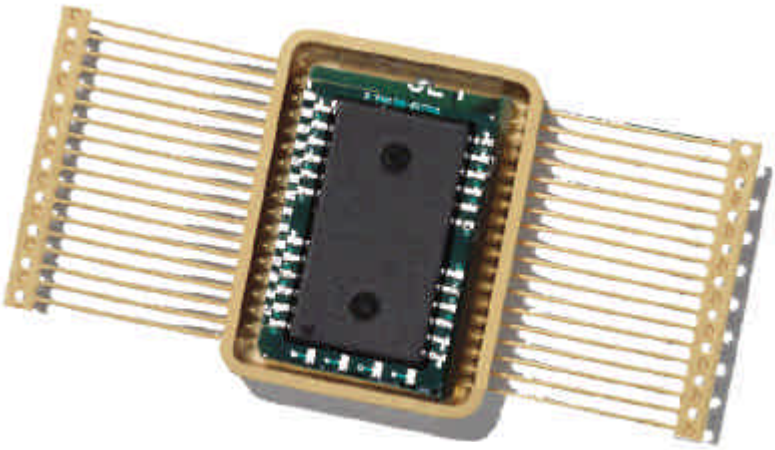
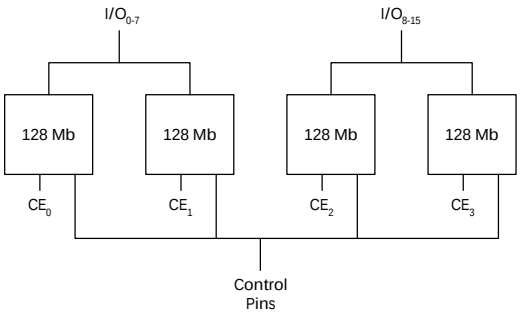
PRELIMINARY

SPACE ELECTRONICS INC.
SPACE PRODUCTS

512 MEGABIT FLASH MEMORY
69F51208RP







FEATURES:

- Identical footprint for ¼, ½ and 1 Gigabit stacks
- User configurable as x8 and x16
- Automatic program and erase
  - Page program: (512 + 16) byte
  - Block erase: (16K + 512) byte
- 528-byte page read operation
  - Random access: 7 µs (max)
  - Serial page access: 50 ns (min)
- Fast write cycle time
  - Program time: 200 µs (typ)
  - Block erase time: 2 ms (typ)
- Command/Address/Data multiplexed I/O port
- Hardware data protection
  - Program/Erase lockout during power transitions
- Reliable CMOS floating-gate technology
  - Endurance: 1M program/erase cycles
  - Data retention: 10 years

DESCRIPTION:

Space Electronics' 69F51208RP (RP for RAD-PAK®) 512 Megabit flash memory provides the highest density, lowest cost memory products available today. This component provides for ½ Gigabit (64 Mbytes) of non-volatile flash memory in a footprint of less than 1.5 square inch. It also provides a cost-effective method to reduce PCB count and size in systems requiring large amounts of memory.

The 69F51208 is configured as a 16-bit wide device and can be user configured as an 8- or 16-bit wide device. Separate chip enables are available for each chip in the stack. For 8-bit applications, the data pins needing to be tied together are adjacent to each other to simplify the PCB design. Similarly, in 16-bit applications, the CEs needing to be tied together are adjacent. This device is the optimum solution for large nonvolatile storage applications such as solid state file storage, digital voice recorder, digital still camera, and other portable applications requiring non-volatility. Capable of surviving space environments, the 69F51208RP is ideal for satellite, spacecraft, and space probe missions. Space Electronics' RAD-PAK® incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing required lifetime in orbit. This product is available with packaging and screening up to Class S.

(858) 452-4167 - Fax: (858) 452-5499 - www.spaceelectronics.com

TABLE 1. 69F51208RP PIN DESCRIPTION

PIN NAME	PIN FUNCTION
$I/O_0 \sim I/O_{15}$	Data Inputs/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}_{0-3}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
$\overline{SE}$	Spare area Enable
$R/\overline{B}$	Ready/Busy output
V_{CC}	Power (2.7V ~ 3.6V)
V_{SS}	Ground
NC	No Connection

TABLE 2. 69F51208RP ABSOLUTE MAXIMUM RATINGS [1,2]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}	-0.6	4.6	V
Temperature Under Bias	T_{BIAS}	-40	85	°C
Storage Temperature	T_{STG}	-65	150	°C
Short Circuit Output Current	I_{OS}	--	5	mA

1. Minimum DC voltage is -0.3V on input/output pins. During transitions, this level may undershoot to -2.0V for periods < 30ns. Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods < 20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 3. 69F51208RP RECOMMENDED OPERATING CONDITIONS

(VOLTAGE REFERENCE TO GND, T_A= -40 TO 85 °C)

PIN	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

TABLE 4. 69F51208RP AC TEST CONDITIONS

(T_A= -40 TO 85 °C, V_{CC} = 3.0 ~ 3.6V UNLESS OTHERWISE SPECIFIED)

PARAMETER	MIN	TYP	MAX	UNIT
Input Pulse Levels	0.4		2.6	V
Input Rise and Fall Times	--	5	--	ns
Input and Output Timing Levels	--	1.5	--	V
Output Load (3.0V +/- 10%)	--	1 TTL GATE and C_L = 50	--	pF
Output Load (3.0V +/- 10%)	--	1 TTL GATE and C_L = 100	--	pF

TABLE 5. 69F51208RP DC AND OPERATING CHARACTERISTICS

(RECOMMENDED OPERATING CONDITIONS OTHERWISE NOTED)

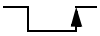
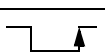
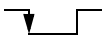
PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Operating Current	Sequential Read x8	I_{CC1}	tcycle=50ns	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA	--	10	25	mA
	Sequential Read x16				--	10	50	
	Program x8	I_{CC2}			--	10	25	
	Program x16				--	10	50	
	Erase x8	I_{CC3}			--	10	25	
	Erase x16				--	10	50	
Stand-by Current (TTL)		I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = $\overline{SE}$ = 0V/V_{CC}		--	--	4	mA
Stand-by Current (CMOS)		I_{SB2}	$\overline{CE}$ = V_{CC} -0.2, $\overline{WP}$ = $\overline{SE}$ = 0V/V_{CC}		--	10	200	µA
Input Leakage Current		I_{LI}	V_{IN} = 0 to 3.6V		--	--	±15	µA
Output Leakage Current		I_{LO}	V_{OUT} = 0 to 3.6V		--	--	±15	µA
Input High Voltage		V_{IH}			2.0	--	V_{CC}+0.3	V
Input Low Voltage, All inputs		V_{IL}			-0.3	--	0.8	V
Output High Voltage Level		V_{OH}	I_{OH} = -400µA		2.4	--	--	V
Output Low Voltage Level		V_{OL}	I_{OL} = 2.1mA		--	--	0.4	V
Output Low Current (R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL} = 0.4V		8	10	--	mA

TABLE 6. 69F51208RP CAPACITANCE

(T_A = 25 °C, V_{CC} = 3.3V, f = 1.0 MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	--	20	pF
Input Capacitance	C_{IN}	V_{IN}=0V	--	20	pF

TABLE 7. 69F51208RP MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{SE}$	$\overline{WP}$	MODE	
H	L	L		H	X	X	Read Mode	Command Input
L	H	L		H	X	X		Address Input (3Clock)
H	L	L		H	X	H	Write Mode	Command Input
L	H	L		H	X	H		Address Input (3Clock)
L	L	L		H	L/H[1]	H	Data Input	
L	L	L	H		L/H[1]	X	Sequential Read & Data Output	
L	L	L	H	H	L/H[1]	X	During Read(Busy)	
X	X	X	X	X	L/H[1]	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X[2]	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}[3]	0V/V_{CC}[3]	Stand-by	

1. When $\overline{SE}$ is high, spare area is deselected.
2. X can be V_{IL} or V_{IH}.
3. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

TABLE 8. 69F51208RP PROGRAM/ERASE CHARACTERISTICS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Program Time		t_{PROG}	--	200	500	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	--	--	2	cycles
	Spare Array		--	--	3	
Block Erase Time		t_{BERS}	--	2	3	ms

TABLE 9. 69F51208RP AC TIMING CHARACTERISTICS FOR COMMAND/ADDRESS/DATA INPUT

PARAMETER	SYMBOL	MIN	MAX	UNIT
CLE Set-up Time	t_{CLS}	0	--	ns
CLE Hold Time	t_{CLH}	10	--	ns
$\overline{CE}$ Setup Time	t_{CS}	0	--	ns
$\overline{CE}$ Hold Time	t_{CH}	10	--	ns
$\overline{WE}$ Pulse Width	t_{WP}	25	--	ns
ALE Setup Time	t_{ALS}	0	--	ns
ALE Hold Time	t_{ALH}	10	--	ns

TABLE 9. 69F51208RP AC TIMING CHARACTERISTICS FOR COMMAND/ADDRESS/DATA INPUT

PARAMETER	SYMBOL	MIN	MAX	UNIT
Data Setup Time	t_{DS}	20	--	ns
Data Hold Time	t_{DH}	10	--	ns
Write Cycle Time	t_{WC}	50	--	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	--	ns

TABLE 10. 69F51208RP AC CHARACTERISTICS FOR OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT
Data Transfer from Cell to Register	t_{R}	--	10	ms
ALE to $\overline{RE}$ Delay(ID read)	t_{AR1}	100	--	ns
ALE to $\overline{RE}$ Delay(Read cycle)	t_{AR2}	50	--	ns
$\overline{CE}$ to $\overline{RE}$ Delay(ID read)	t_{CR}	100	--	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	--	ns
$\overline{RE}$ Pulse Width	t_{RP}	30	--	ns
$\overline{WE}$ High to Busy	t_{WB}	--	100	ns
Read Cycle Time	t_{RC}	50	--	ns
$\overline{RE}$ Access Time	t_{REA}	--	35	ns
$\overline{RE}$ High to Output Hi-Z [1]	t_{RHZ}	15	30	ns
$\overline{CE}$ High to Output Hi-Z [1]	t_{CHZ}	--	20	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	--	ns
Output Hi-Z to $\overline{RE}$ Low [1]	t_{IR}	0	--	ns
Last $\overline{RE}$ High to Busy(at sequential read)	t_{RB}	--	100	ns
$\overline{CE}$ High to Ready(in case of interception by $\overline{CE}$ at read) [2]	t_{CRY}	--	50 +tr(R/B) [3]	ns
$\overline{CE}$ High Hold Time(at the last serial read) [4]	t_{CEH}	100	--	ns
$\overline{RE}$ Low to Status Output	t_{RSTO}	--	35	ns
$\overline{CE}$ Low to Status Output	t_{CSTO}	--	45	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	--	ns
$\overline{RE}$ access time(Read ID)	t_{READID}	--	35	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	--	5/10/500	ms

1. Not tested.
2. If $\overline{CE}$ goes high within 30ns after the rising edge of the last $\overline{RE}$, R/$\overline{B}$ will not return to V_{OL}.
3. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.
4. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than t_{CEH}.

FIGURE 1. FLOW CHART TO CREATE INVALID BLOCK TABLE

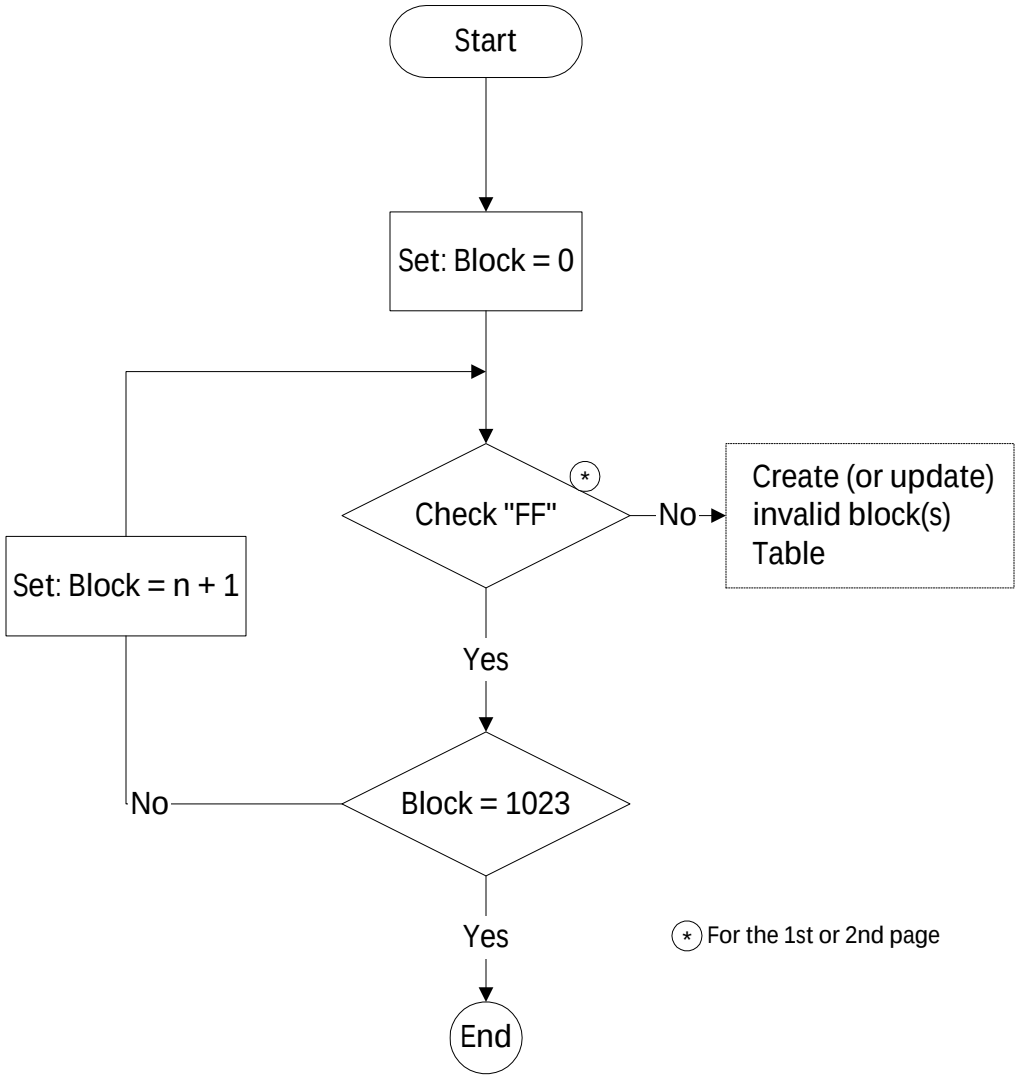
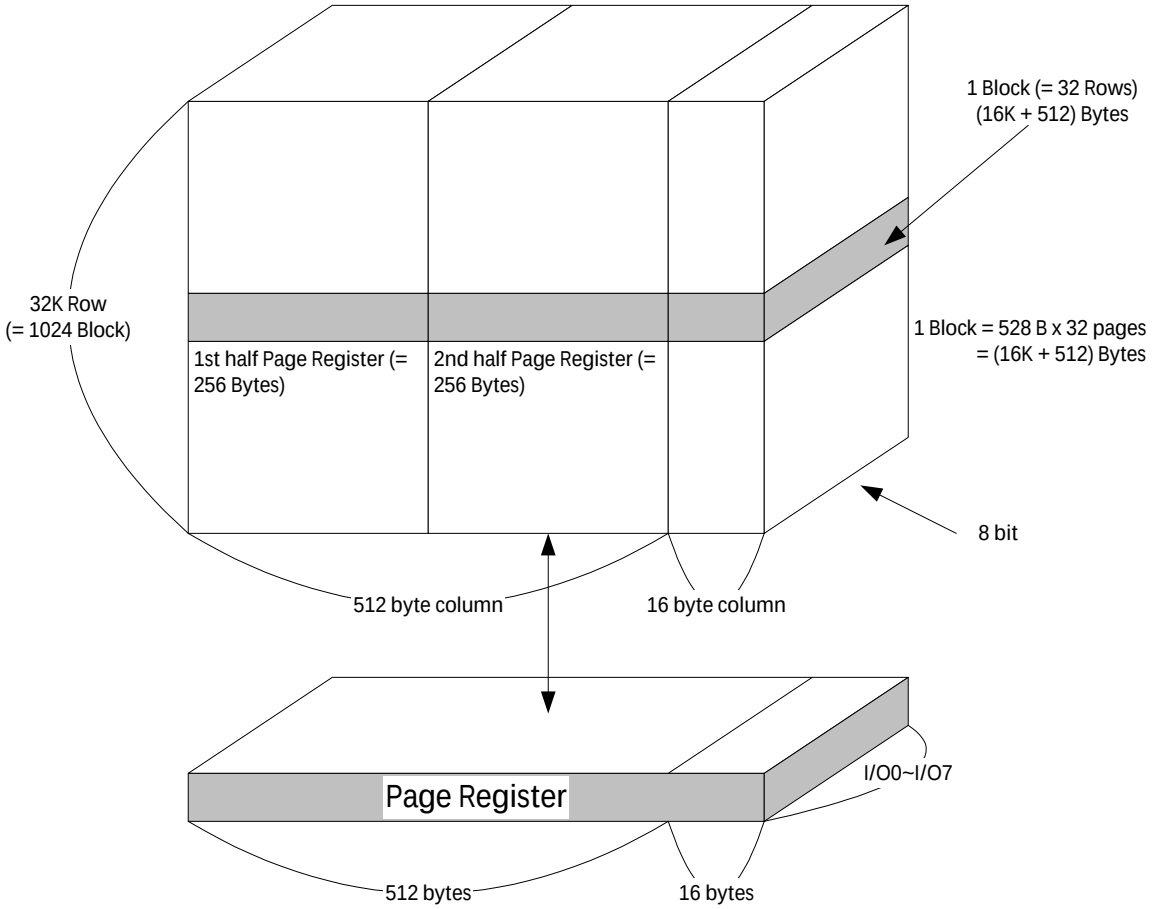
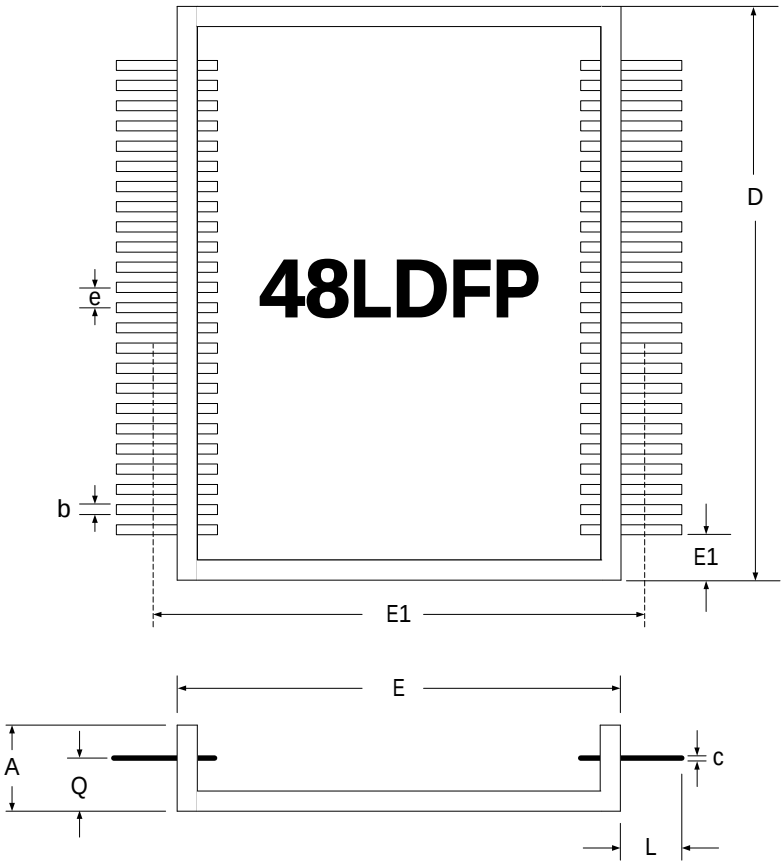


FIGURE 2. ARRAY ORGANIZATION



	I/O_0,I/O_8	I/O_1,I/O_9	I/O_2,I/O_{10}	I/O_3,I/O_{11}	I/O_4,I/O_{12}	I/O_5,I/O_{13}	I/O_6,I/O_{14}	I/O_7,I/O_{15}	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address[1]
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16	Row Address
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	X[2]	(Page Address)

1. Column address: Starting Address of the Register.
   00h Command(Read) : Defines the starting address of the 1st half of the register.
   01h Command(Read) : Defines the starting address of the 2nd half of the register.
2. A8 is initially set to "Low" or "High" by the 00h or 01h Command.
   X can be High or Low.



48 LEAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.570	0.580	0.595
b	0.010	0.015	0.020
c	0.005	0.010	0.015
D	0.900	1.000	1.100
E	1.300	1.400	1.500
E1	--	--	1.800
e	0.050 BSC		
L	0.500	--	--
Q	0.182	0.195	0.208
S1	0.363	0.368	0.373
N	48		

F48-01
Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Space Electronics verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Space Electronics assumes no responsibility for the use of this information.

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