To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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6AM14

Silicon N-Channel/P-Channel Power MOS FET Array

Application

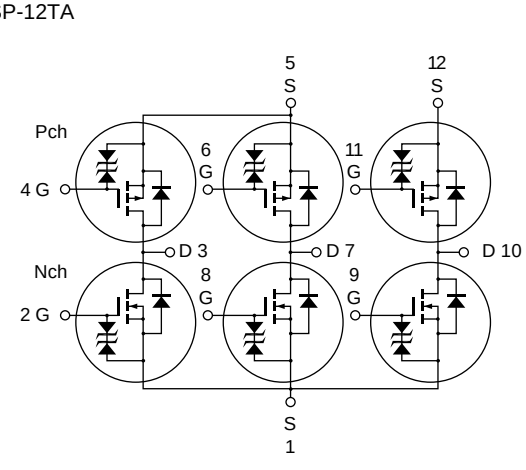
High speed power switching

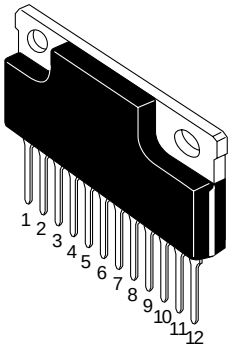
Features

- Low on-resistance
- Low drive current
- High speed switching
- High density mounting

Outline

SP-12TA





1.	N-ch Source
2, 8, 9	N-ch Gate
3, 7, 10.	N-ch Drain P-ch Drain
4, 6, 11.	P-ch Gate
5, 12.	P-ch Source

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	7	–7	A
Drain peak current	$I_{D(pulse)}$*[1]	28	–28	A
Reverse drain current	I_{DR}	7	–7	A
Channel dissipation	Pch*[2]	42		W
Channel dissipation	Pch*[2]	4.8		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at 6 Drive operation

Electrical Characteristics N Channel (Ta = 25°C)

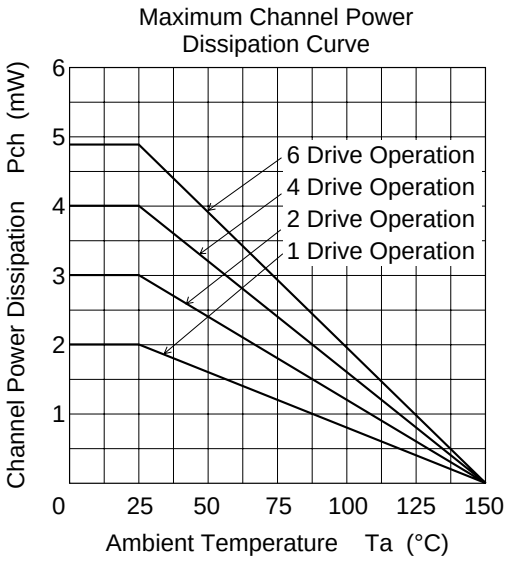
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.14	0.2	Ω	I_D = 4 A V_{GS} = 4 V*[1]
		—	0.22	0.5	Ω	I_D = 2 A V_{GS} = 2.5 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	4.0	6.5	—	S	I_D = 4 A V_{DS} = 10 V*[1]
Input capacitance	Ciss	—	500	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	240	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	30	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = 10 V, I_D = 4 A
Rise time	t_r	—	90	—	ns	R_L = 7.5 Ω
Turn-off delay time	$t_{d(off)}$	—	110	—	ns	
Fall time	t_f	—	250	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 7 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	170	—	ns	I_F = 7 A, V_{GS} = 0 diF/dt = 50 A/µs

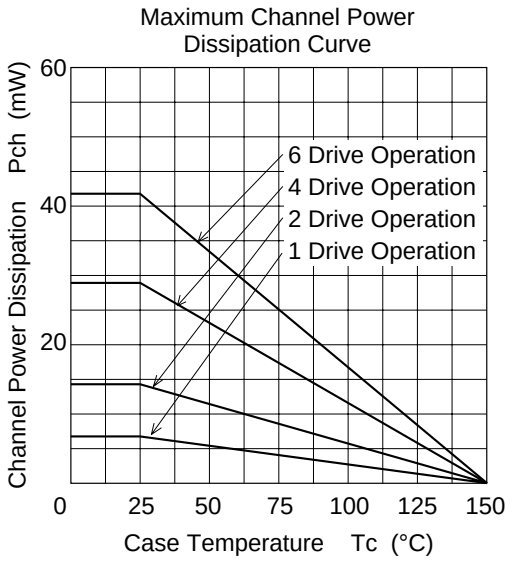
Note: 1. Pulse Test

Electrical Characteristics P Channel (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	I_D = –4 A V_{GS} = –4 V*[1]
		—	0.16	0.3	Ω	I_D = –2 A V_{GS} = –2.5 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	5.0	8.0	—	S	I_D = –4 A V_{DS} = –10 V*[1]
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	590	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	120	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = –10 V, I_D = –4 A
Rise time	t_r	—	75	—	ns	R_L = 7.5 Ω
Turn-off delay time	$t_{d(off)}$	—	240	—	ns	
Fall time	t_f	—	180	—	ns	
Body to drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –7 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	210	—	ns	I_F = –7 A, V_{GS} = 0 diF/dt = 50 A/µs

Note: 1. Pulse Test


Maximum Channel Power Dissipation Curve
Channel Power Dissipation Pch (mW)
6
5
4
3
2
1
0
25
50
75
100
125
150
Ambient Temperature Ta (°C)
6 Drive Operation
4 Drive Operation
2 Drive Operation
1 Drive Operation


Maximum Channel Power Dissipation Curve
Channel Power Dissipation Pch (mW)
60
40
20
0
25
50
75
100
125
150
Case Temperature Tc (°C)
6 Drive Operation
4 Drive Operation
2 Drive Operation
1 Drive Operation

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