69003 / 69004
PC Video Pro

Video Windowing Controller

Data Sheet

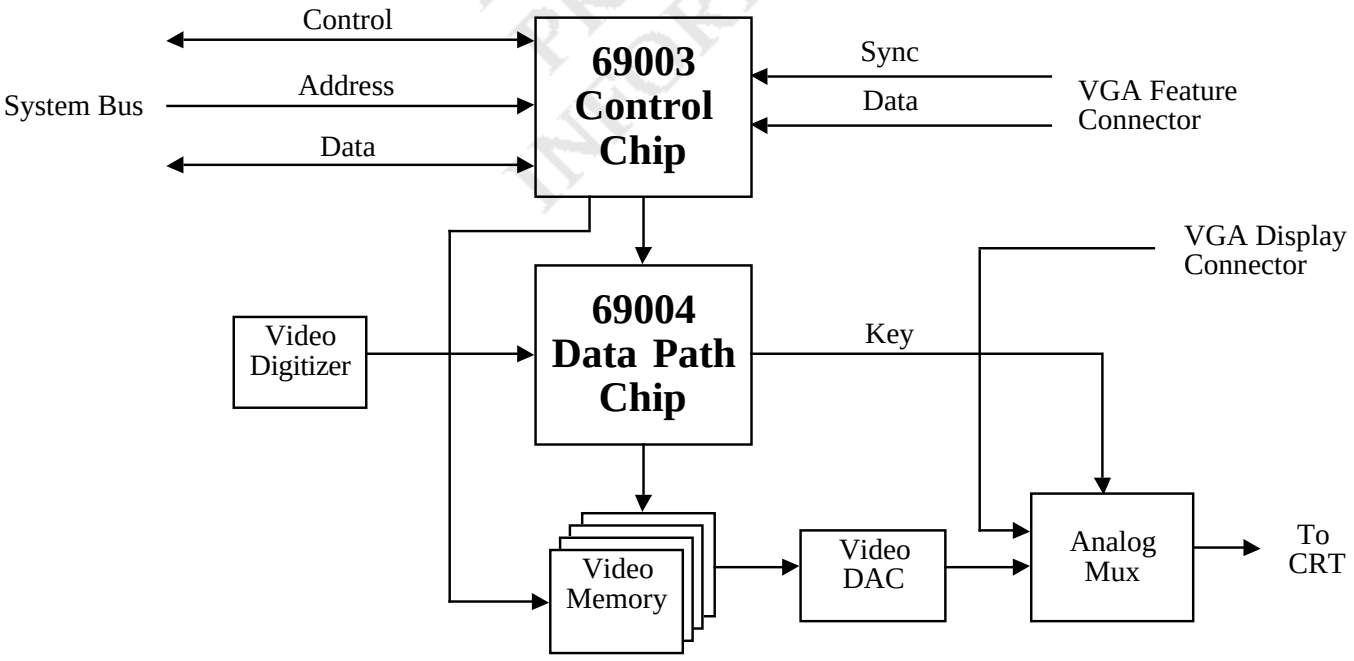
January 1992

P R E L I M I N A R Y

CHIPS®

69003 / 69004
PC Video Pro
Video Windowing Controller

- Scan rate conversion and windowing control for display of a live video image on a computer graphics monitor
- Supports standard 4:1:1 and 4:2:2 YUV and 16-bit per pixel or 24-bit per pixel or 32-bit per pixel RGB digital formats
- Window positioning controlled by independent X-Y coordinates and by color keying
- Independent X-Y scaling of video image to 1/64 original image size
- Still-frame capture and display of true-color images
- Input resolutions up to 1024H x 1024V pixels with full broadcast quality video bandwidth
- Supports NTSC, PAL, SECAM, S-VHS, and RGB input formats from industry-standard video digitizer chipsets
- Interlaced or non-interlaced input video
- Interlaced or non-interlaced output support
- Output zoom by factors of 2, 4 and 8
- Output resolutions up to 1024 x 768
- Supports full-screen PAL display
- Software compatible with PC Video (82C9001)



PC Video Pro System Block Diagram

Revision History

Revision	Date	By	Comment
0.1	11/22/91	ME/ST	Initial Draft Copy
0.2	12/4/91	ME/JF	Added System Diagram, Pinouts, and Mechanical Specification
0.3	1/15/92	ST	Official Release

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Introduction

OVERVIEW

The PC Video Pro video windowing chip set is the core component of a video subsystem which converts a standard full-motion video image into a format for display on a computer graphics monitor. PC Video Pro controls positioning and scaling of the video image on the output display and allows the video image to be merged with computer graphics for interactive multimedia applications. The PC Video Pro is targeted for the workstation requirements of high-resolution and 24-bit color. Market applications of a subsystem based on PC Video Pro include interactive video training, computer-based education programs, point-of-sale information, business presentations, video conferencing, and desktop publishing. PC Video Pro integrates all the controlling logic for video scan rate conversion, windowing control, and scaling. Operation with VGA graphics is supported via the graphics feature connector.

A video windowing sub-system can be implemented with the following components:

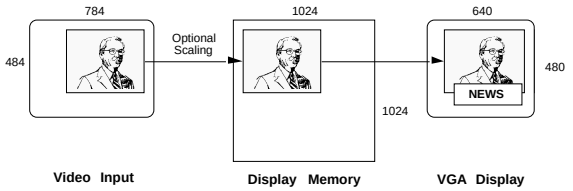
PC Video Pro
A standard "Digital TV" chip set
6 VRAMs

Other optional configurations are supported for higher color and luminance bandwidth.

PC Video Pro is register-compatible to the 82C9001A PC Video chip, allowing software applications written for PC Video to be easily ported to PC Video Pro.

WINDOW AQUISITION AND POSITIONING

PC Video Pro provides the control signals for a standard video digitizer chip set. Interlaced and non-interlaced video sources, at full broadcast quality bandwidth, are supported at resolutions up to 1024 x 1024 pixels. PC Video Pro may be programmed to capture a full-size video image or a user-defined cropped or reduced area.



Acquisition & Display Process

Video output window positioning is provided by programmable X-Y coordinates and color keying to a specified color. Color Keying is based on the digital color information from the VGA feature connector. Color keying is supported independently or in conjunction with X-Y coordinates.

SCALING

PC Video Pro provides independent X-Y scaling of the input video image in integer increments of 1/64. Images may be compressed down to 1/64 of the original image size, supporting video icons for graphical user interfaces.

MEMORY INTERFACE

PC Video Pro operates with 256K x 4 100 ns VRAMs. Five configurations are supported: 4 VRAMs for 2:1:1 encoding, 6 VRAMs for 4:1:1 encoding, 8 VRAMs for 4:2:2 or 16-bit RGB encoding, 12 VRAMs for 24-bit RGB and 16 VRAMs for 1024 x 1024 resolution or 24-bit RGB + 8-bit overlay.

MEMORY REQUIREMENTS

Bits per Pixel	Format	Memory Required	Video Quality
12-bit	2:1:1 YUV	4 VRAM	Compressed luminance bandwidth
12-bit	4:1:1 YUV	6 VRAM	Broadcast video bandwidth
16-bit	4:2:2 YUV	8 VRAM	Improved chroma bandwidth
16-bit	16-bit RGB	8 VRAM	65,536 colors
16-bit	4:2:2 YUV	16 VRAM	1024 x 1024 High resolution
24-bit	24-bit RGB	12 VRAM	16.8 million colors
32-bit	24-bit RGB	16 VRAM	16.8 million colors + 8-bit overlay

QUICK-START KIT

The PC Video Pro Quick-Start Kit offers a working example of a 16-bit, full-screen PAL implementation at resolutions up to 1024 x 768. A Windows DLL and sample application are included in the kit. The development kit also includes an OEM software license.

PC VIDEO PRO DESCRIPTION

Video Formats

Color images in computer graphics are typically represented by R, G, and B components. Video and TV images are typically represented by one luma (Y) and two chroma (U, V) components which make up a composite video signal. The luma component has twice the bandwidth of the individual chroma components. Digitized video systems typically use luma/chroma components because of the ease of conversion to and from composite video signals. Representation of an image in luma/chroma is also more memory efficient than in R, G, and B components. A 640x480 image in 16-bit RGB produces 65,536 colors and requires 1 meg of VRAM. The same image can be saved in Luma/Chroma coordinates in 768k of VRAM and produces 2 million colors.

PC Video Pro is flexible to support both R, G, B and Y, U, V components. Four main formats are supported as described below.

The X:Y:Z numbers refer to the number of samples for the three input video components.

1) 4:1:1 – The luma component (Y) is sampled every pixel and the chroma components (U, V, or Yr, Yb) are averaged over four pixels. For every four input pixels, there are four luma samples and one U and V (chroma) sample, for six samples total.

2) 4:2:2 – This format expands the color bandwidth of the 4:1:1 format. The chroma components are averaged over two pixels. For every four input pixels, there are four luma samples and two of each chroma samples, for eight samples total. This is the international broadcast standard CCIR 601.

3) 4:4:4 – This format is typically used for R, G, B components but could also be used for luma and chroma components. The components are sampled at every pixel, resulting in 12 samples to four pixel times. The bandwidth on all components is the same.

Signal Flow

Image acquisition and display in a PC Video Pro subsystem are two independently programmable processes which occur at asynchronous clock rates.

Acquisition

PC Video Pro provides the control signals to a standard digital video chipset. The acquisition window coordinates are programmable, enabling cropping and panning of the input image. The digitized video passes through PC Video's internal FIFO and is stored in the frame buffer. The acquisition process is synchronized to the input video VSYNC and HBLANK signals and is executed at the video sampling rate. The image acquisition data is applied to the random access ports of the dual-ported video rams. Scaling is performed upon the input video data as part of the acquisition process. The scaled image is stored in the frame buffer.

The input window supports both interlaced (default) and non-interlaced video. Four capture modes are available: (a) Interlaced frame, (b) Even field, (c) Odd field), and (d) Non-interlaced frame. In unscaled, interlaced mode the raster address is advanced by two, with the even field writing the even line numbers and the odd field writing odd lines. The even field starts at line 0 and advances by 2's: 0, 2, 4. The odd field starts at line 1 and advances by 2's: 1, 3, 5, up to the maximum line count.

An address multiplexer selects addresses from the acquisition window, video display window or the host processor. Either live video acquisition or CPU read/write access may take place but not both simultaneously.

Display

The display process is synchronized to the VGA HSYNC, VSYNC, BLANK, and CLOCK signals from the feature connector. The data is output from the serial port of the video rams. The video image may be displayed inside or outside any rectangular window on the VGA screen.

System Clocks

The video ram control/timing logic uses the double rate video input clock. The double clock rate of 27 MHz is line-locked, tracking variations in input video sync, which occur with video tape recorders (VTR's), still-video cameras and other non-time base stable sources. The maximum input clock rate is 30 MHz.

CPU Interface

PC Video Pro has a non-multiplexed 24 bit address bus and a 16 bit data bus. PC Video Pro latches AT bus addresses LA[20:23] using the AT bus signal ALE. PC Video Pro memory is accessible using 8 and 16 bit bus cycles while PC Video Pro I/O registers are accessible using 8 bit cycles only. PC Video Pro handles all byte swapping for memory accesses. PC Video Pro supports 16 bit memory cycles and generates MEMCS16/ when memory is

mapped above 1M byte in the PC address space. PC Video Pro-based boards can be plugged into a 16 bit bus slot.

PC Video Pro may be programmed to respond to either a fixed I/O address or software programmed I/O address. When the bus RESET signal goes from high to low, the status of CS/ pin is sampled by PC Video Pro. If CS/ is sampled active (low) then PC Video Pro responds to I/O addresses 0AD6-7h. However if CS/ is inactive (high) then it uses the Programmed I/O Address Register bits 7:0 and CS/ to detect the valid I/O address space. When this mode is selected, the Programmed I/O Address Register bits are written by the first CPU I/O write cycle with CS/ active. Since PC Video Pro always occupies two consecutive I/O addresses, bit-0 of this register is ignored.

Memory Interface

Memory is organized as 2 banks 1K wide by 512 or 1K high. The depth of the memory is either 12 bits for 4:1:1 multiplexed data format, 16 bits for the 4:2:2 multiplexed data formats, 24 bits for RGB format, or 32 bits for RGB + Key (refer to memory configuration diagram below).

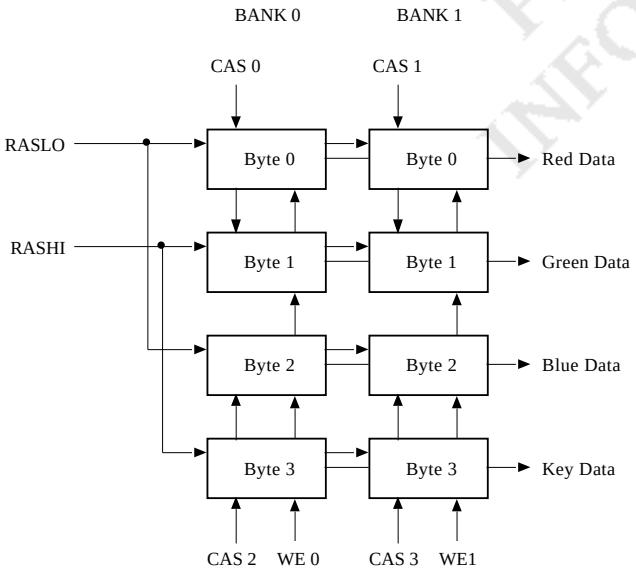
PC Video Pro uses 256K x 4, 100 nS VRAMs and supports four VRAM configurations. PC Video Pro also supports the VRAM Write Bit Mask function. Frame buffer memory is accessible in the extended memory address space above 1 MByte (100000h), located on any 2 MByte boundary. The memory can be accessed as a 2 MByte linear space or as two 1 MByte spaces selected by the paging bit in register 6. The Video Frame Buffer memory can be accessed as byte or word cycles. PC Video Pro generates one wait state for memory accesses, or more than one when memory accesses conflict with VRAM refresh cycles or VRAM data transfer cycles. PC Video Pro memory is not accessible on RESET and must explicitly be enabled to access the PC Video Pro memory.

Interrupt Support

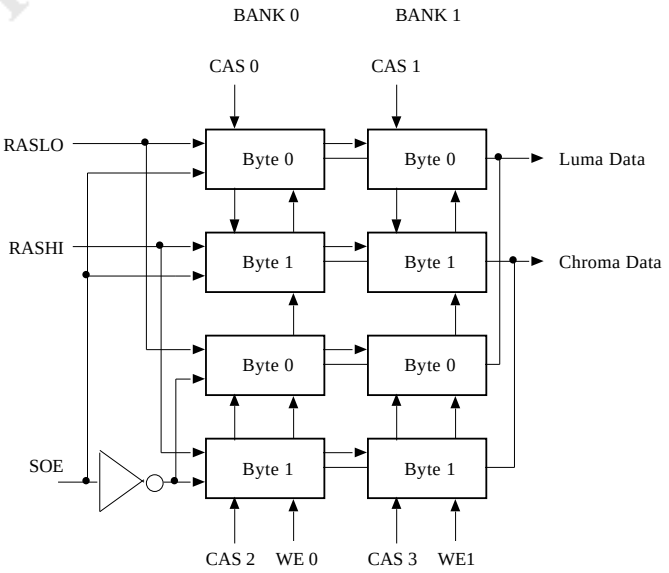
PC Video Pro supports CPU interrupts upon receipt of a video Vsync. The interrupt source bits are held until cleared by software.

Video RAM Timing Generator

A synchronous timing generator operates the video RAM control signals, derived from the double rate video data clock. The video RAM is operated as two



1024H x 512V x 32 bit



1024H x 1024V x 16 bit

Example Memory Configurations

Each box represents two 256K X 4 VRAMS. SCLK and DTOE are common to each VRAM.

banks each running in "fast-page" mode along the line. Each bank receives alternating pixels across the horizontal line, using a common data bus driven at the pixel rate of 13.5 MHz. The column address signal (CAS) or write enable (WE) of each bank strobes in the pixel data.

Memory refresh occurs during input video horizontal blanking. PC Video Pro provides limited access to the memory during acquisition in the vertical blanking of an acquisition frame. Additional access time is available in field grab mode. Along with the vertical interval, the unused field time can be used for processor access. During acquisition, the CPU may poll a bit to verify that memory is available for a CPU access. Once the memory is available the CPU can initiate a cycle. When the cycle is completed, the CPU can verify that no conflict occurred by checking the Error bit of register 9, the interrupt polling/mask register. If the Error bit is set then the CPU must assume that the cycle did not occur, clear the Error bit, and reissue the cycle when the memory is available.

CPU access utilizes a standard read/write cycle using the parallel data path, bypassing the input video FIFO.

The VGA display window uses the 1 MEG (256K x 4) VRAM serial shift register to scan-out the display data. The VRAM serial output is used only in read mode and two banks of VRAMs operate in a ping-pong style data organization providing 1024 pixels per line from two 512 pixel VRAM shift registers.

The following VRAM memory cycles are supported:

Cycle Type	Function
1) Random Read/Write cycle	processor access
2) CAS before RAS refresh	refresh only
3) Shift Register Load	loading shift register for output display
4) Fast-page mode write	video acquisition
5) Write Bit Mask	masking of data bits during video acquisition or CPU write
6) Shift register output	clocked at one half the output display rate

Scaling

Two independent input scaling ratios are supported: one for the horizontal, the other for the vertical. The vertical ratio accounts for interlace.

Scaling is performed by dropping pixels horizontally and dropping lines vertically. Independent scaling factors, ranging from 1/64 to 63/64 in integer multiples of 1/64 are supported in the horizontal and vertical directions. 64/64 is supported by turning scaling off.

Display Window Overlay

The mixing of the analog VGA and analog video data is performed externally using an analog multiplexer. The multiplexer control signal can be generated in three different ways:

a) By defining an output window in the PC Video Pro X-Y Window Control Registers,
b) By keying to a VGA Color (Color compare) or
c) Use overlay plane as a key source.

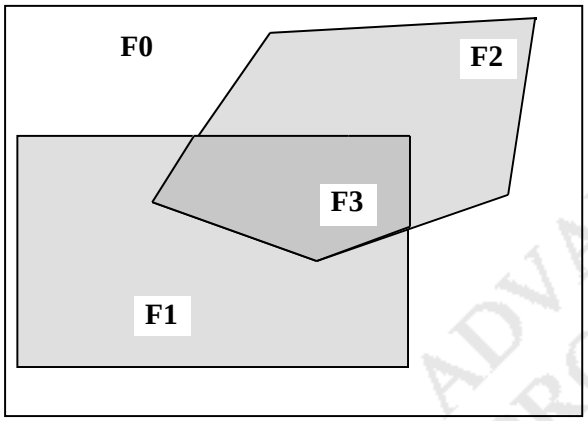
The multiplexer function for cases (a) and (b) is generated by PC Video Pro and is clocked by the VGA clock (PCLK). In case (c), the overlay memory output drives an external video multiplexer. With more bits of the overlay memory driving a DAC (4 or 8 bit) a linear key signal can be generated to control an external video mixer.

X-Y Window Control Registers:
The X-Y window area is defined by four registers that specify a rectangular region using X-start, X-end, Y-start, and Y-end. The X-Y window position is referenced to the VGA sync signals. The size of the X-Y window is defined in VGA clocks and lines.

Color Keying:
A control signal is generated by comparing the 8 bit VGA TTL video data (P7:0) to an 8 bit value in the Color Key register. Comparison of certain color key bits can be disabled by setting the corresponding bit in the color compare mask register. This allows keying on more than one color. The VGA pixel data is sampled by PCLK.

Overlay Memory Data:
One or more bits of the overlay (KEY) memory may be used to control the combination of live video and VGA data. Through support of the Write Mask, the overlay can be protected, and a keying pattern written to it. Using one bit of the overlay creates a one bit mask, which can control an analog or digital multiplexer. This forms a “Hard-Edge KEY”. Four bits or more of KEY memory can drive a DAC which forms a linear key signal. This signal is sent to a linear mixer, which can smoothly combine the VGA and video picture. The image written into the overlay plane decides the transparency or opacity of the mixed VGA and video signal.

Color Key Functions:
There are four possible combinations of the display window and color key areas. They are: non window and non key area (F0), window area but not key (F1), key area but not window (F2) and both window and key area (F3). These four functions select one of the function bits on a pixel by pixel basis. If the function bit for that area is a '0', that display area shows the VGA graphics. If the function bit for that area is '1', the video output data is overlayed on the VGA graphics. If the X-Y window is disabled, areas F1 and F3 do not exist. If color keying is disabled, areas F2 and F3 do not exist.



Overlay Functions

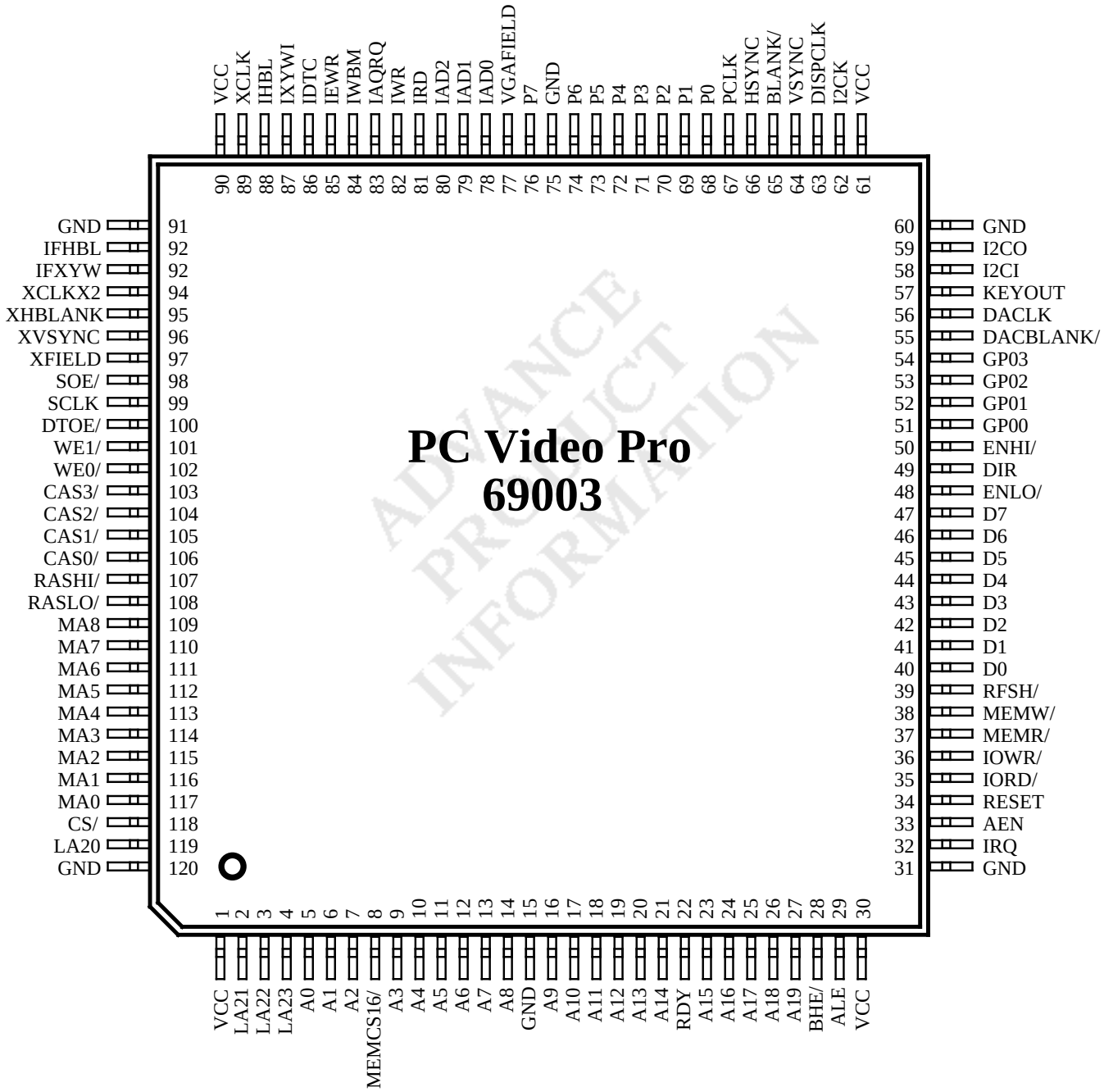
Display Area Panning

Video data in the display area can be panned horizontally by 1024 pixels in steps of 4 pixels for 4:1:1 input Y/C format or in steps of 2 pixels for 4:2:2 input Y/C format. Video data may be panned vertically by 1024 in steps of 1 scan line.

Global Enable/Disable of PC Video Pro

PC Video Pro I/O register index FFh is reserved for global enable and disable of PC Video Pro. This register is a write only register. Bit-0 of this register is used to control this function. This bit is cleared on RESET. After PC Video's I/O address is determined, this bit should be set to '1' to enable access to other PC Video Pro I/O registers. The PC Video Pro frame buffer is accessible when bit-1 of this register is set to '1'. The upper 4 bits of this register are readable and they reflect the 69003 Revision/Part Number.

69003 Pinouts



PIN DESCRIPTIONS — 69003 System Bus Interface

Pin #	Pin Name	Type	Active	Description
5	A0	In	Both	20 bits of system address bus
6	A1	In	Both	
7	A2	In	Both	
9	A3	In	Both	
10	A4	In	Both	
11	A5	In	Both	
12	A6	In	Both	
13	A7	In	Both	
14	A8	In	Both	
16	A9	In	Both	
17	A10	In	Both	
18	A11	In	Both	
19	A12	In	Both	
20	A13	In	Both	
21	A14	In	Both	
23	A15	In	Both	
24	A16	In	Both	
25	A17	In	Both	
26	A18	In	Both	
27	A19	In	Both	
119	LA20	In	Both	Upper 4 bits of the system address bus. These address bits are latched on the falling edge of ALE.
2	LA21	In	Both	
3	LA22	In	Both	
4	LA23	In	Both	
40	D0	I/O	Both	System data bus
41	D1	I/O	Both	
42	D2	I/O	Both	
43	D3	I/O	Both	
44	D4	I/O	Both	
45	D5	I/O	Both	
46	D6	I/O	Both	
47	D7	I/O	Both	
34	RESET	In	High	Reset
39	RFSH/	In	Low	System Refresh. When this input is low, the current memory cycle is ignored.
48	ENLO/	Out	Low	Enable controls for external data transceivers for the data bus.
50	ENHI/	Out	Low	

PIN DESCRIPTIONS **69003 System Bus Interface (continued)**

Pin #	Pin Name	Type	Active	Description
49	DIR	Out	Both	Direction control for external data bus transceivers: 0 = read from PC Video, 1 = write to PC Video.
28	BHE/	In	Low	Enable for 16-bit interface. Low indicates that the high order byte at the current word address is being accessed. Along with A0, indicates which bytes are transferred over the bus (all byte steering is done internally): BHE/ A0 Effect 0 0 Both bytes on D15:0 0 1 High byte on D15:8 1 0 Low byte on D7:0
33	AEN	In	Both	Defines valid I/O address: 0 = valid I/O address, 1 = Invalid I/O address (DMA cycle). If single-cycle DMA is used, memory addresses will be on the bus at the same time that IORD/ or IOWR/ is active. PC Video will not respond to IORD/ or IOWR/ while AEN=1.
29	ALE	In	High	Address latch enable. The system address is latched on the falling edge of this signal.
22	RDY	Out	High	Ready. Driven low to indicate the current cycle should be extended with wait states. Driven high at end of cycle to indicate 'ready' then tri-stated. This signal is normally high and is only driven low if PC Video cannot respond immediately to a memory request and wait states are necessary.
8	MEMCS16/		Out	Indicates 16-bit Memory cycle. Asserted by PC Video to indicate that the chip is capable of transferring 16 bits over the bus at the requested address.
37	MEMR/	In	Low	Indicates a memory read cycle from AT bus
38	MEMW/	In	Low	Indicates a memory write cycle from AT bus
35	IORD/	In	Low	Indicates an I/O Read cycle
36	IOWR/	In	Low	Indicates an I/O Write cycle
32	IRQ	Out	Both	Video VSYNC Interrupt. This pin is low when interrupts are enabled but no interrupt is pending, and high when interrupts are enabled and an interrupt is pending.

PIN DESCRIPTIONS — 69003 Memory Interface

Pin #	Pin Name	Type	Active	Description
109	MA8	Out	High	VRAM Address bus for both banks and planes of memory.
110	MA7	Out	High	
111	MA6	Out	High	
112	MA5	Out	High	
113	MA4	Out	High	
114	MA3	Out	High	
115	MA2	Out	High	
116	MA1	Out	High	
117	MA0	Out	High	
107	RASHI/	Out	Low	VRAM Row Address Strobe for Luminance plane.
108	RASLO/	Out	Low	VRAM Row Address Strobe for Chrominance plane.
103	CAS3/	Out	Low	VRAM Column Address Strobe. There is a strobe for each bank of memory.
104	CAS2/	Out	Low	
105	CAS1/	Out	Low	
106	CAS0/	Out	Low	
101	WE1/	Out	Low	VRAM Write Enable. There is an enable for each bank of memory.
102	WE0/	Out	Low	
100	DTOE/	Out	Low	Data Transfer / Output Enable.
99	SCLK	Out	High	VRAM shift Clock for all VRAMs. This signal is also used to multiplex the output data from the VRAM banks.

PIN DESCRIPTIONS 69003 VGA/Video Interface

Pin #	Pin Name	Type	Active	Description
67	PCLK	In	Both	VGA Pixel Clock. This clock is used to latch the VGA pixel data and synchronize the video overlay window.
66 64 65	HSYNC VSYNC BLANK/	In In In	Both Both Low	Horizontal, Vertical Sync, and Blank signals from the VGA feature connector. These signals are used to synchronize the overlay of video and VGA graphics.
77	VGAFIELD		In	Both External Field bit. Chip uses internally generated field signal for display out overlay, by default. However, if required, field signal from this pin can be selected by setting bit D1 of Reg. 50 to 1.
76 74 73 72 71 70 69 68	P7 P6 P5 P4 P3 P2 P1 P0	In In In In In In In In	Both Both Both Both Both Both Both Both	Pixel Data from the VGA feature connector. This data is used for color matching to control overlay of VGA graphics and video output.
89	XCLK	In	Both	Video Data Clock. This clock is to latch the Video data from the digital video source.
94	XCLKX2	In	Both	Twice Video Data Clock. This clock is twice the Video data clock. It is used to generate the VRAM timing.
96	XVSYNC	In	Both	Vertical Sync signal from the digital video source. This signal is used to synch. the storage of the video data.
95	XHBLANK	In	Both	Horizontal Blank. This signal is used to identify the active area in the digital video output data stream.
97	XFIELD	In	Both	External Field. Chip uses internally generated field signal, by default. However, if required, field signal from this pin can be selected by setting bit D6 of Reg. 21 to 1.
118	CS/	In	Low	Chip Select (I/O only.) This pin is sampled on the falling edge of reset. If it is low, PC Video will respond to I/O accesses at locations 0AD6 and 0AD7. If it is high, then the Programmed I/O Register and the CS/ input are used to detect a valid I/O address.
62 59 58	I2CK I2CO I2CI	Out Out In	Both Both Both	These open collector I/O pins are designed to support the Inter-Integrated Circuit (I2C) bus.

PIN DESCRIPTIONS **69003 VGA/Video Interface (continued)**

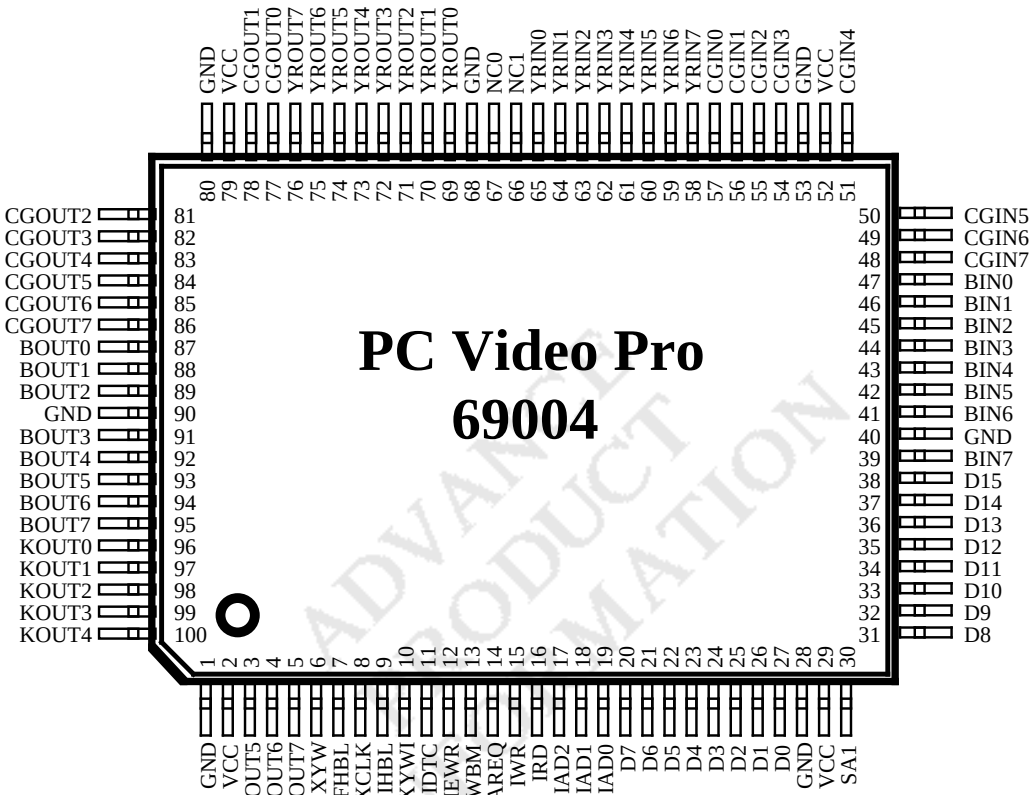
Pin #	Pin Name	Type	Active	Description
63	DISPCLK	In	Both	Display Clock input. This input supplies the clock that is used to output the digital video data.
56	DACLK	Out	Both	Video DAC Clock. This signal clocks the output video data into the video DACs. Derived from DISPCLK.
55	DACBLANK/	Out	Low	Video Blank output to DAC. This signal is synchronized with DISPCLK and qualifies valid video data from the VRAM memory.
57	KEYOUT	Out	Low	Video/VGA Mux. When high, the output data mux selects Video data; when low, the output is VGA graphics.
54	GPO3	Out	Both	General Purpose I/O strobes. These pins may be used as I/O strobes for additional user defined external registers. GP01 can be defined as a Phase locked loop reference output by setting bit 5 of Register 18 to '0'.
53	GPO2	Out	Both	
52	GPO1	Out	Both	
51	GPO0	Out	Both	
78	IAD0	Out	Both	Inter-chip control signals. These pins connect to the corresponding pins on the 69004.
79	IAD1	Out	Both	
80	IAD2	Out	Both	
81	IRD	Out	Both	
82	IWR	Out	Both	
83	IAQRQ	Out	Both	
84	IWBM	Out	Both	
85	IEWR	Out	Both	
86	IDTC	Out	Both	
87	IXYW	Out	Both	
88	IHBL	Out	Both	
92	IFHBL	In	Both	
93	IFXYW	In	Both	

PIN DESCRIPTIONS

69003 Power and Ground

Pin #	Pin Name	Type	Active	Description
1 30 61 90	VCC	Pwr	-	+ 5V Power
15 31 60 75 91 120	GND	Pwr	-	Ground

69004 Pinouts



PIN DESCRIPTIONS

69004 System Bus Interface

Pin #	Pin Name	Type	Active	Description
30	A1	In	Both	1 bit of system address bus
27	D0	I/O	Both	System data bus
26	D1	I/O	Both	
25	D2	I/O	Both	
24	D3	I/O	Both	
23	D4	I/O	Both	
22	D5	I/O	Both	
21	D6	I/O	Both	
20	D7	I/O	Both	
31	D8	I/O	Both	
32	D9	I/O	Both	
33	D10	I/O	Both	
34	D11	I/O	Both	
35	D12	I/O	Both	
36	D13	I/O	Both	
37	D14	I/O	Both	
38	D15	I/O	Both	

PIN DESCRIPTIONS — 69004 Video Memory Interface

Pin #	Pin Name	Type	Active	Description
76	YROUT7	I/O	High	Luminance/Red Data bus. These pins connect to the VRAM data pins.
75	YROUT6	I/O	High	
74	YROUT5	I/O	High	
73	YROUT4	I/O	High	
72	YROUT3	I/O	High	
71	YROUT2	I/O	High	
70	YROUT1	I/O	High	
69	YROUT0	I/O	High	
86	CGOUT7	I/O	High	Chrominance/Green Data bus. These pins connect to the VRAM data pins.
85	CGOUT6	I/O	High	
84	CGOUT5	I/O	High	
83	CGOUT4	I/O	High	
82	CGOUT3	I/O	High	
81	CGOUT2	I/O	High	
78	CGOUT1	I/O	High	
77	CGOUT0	I/O	High	
95	BOUT7	I/O	High	Blue Data bus. These pins connect to the VRAM data pins.
94	BOUT6	I/O	High	
93	BOUT5	I/O	High	
92	BOUT4	I/O	High	
91	BOUT3	I/O	High	
89	BOUT2	I/O	High	
88	BOUT1	I/O	High	
87	BOUT0	I/O	High	
5	KOUT7	I/O	High	Alpha Data bus. These pins connect to the VRAM data pins.
4	KOUT6	I/O	High	
3	KOUT5	I/O	High	
100	KOUT4	I/O	High	
99	KOUT3	I/O	High	
98	KOUT2	I/O	High	
97	KOUT1	I/O	High	
96	KOUT0	I/O	High	

PIN DESCRIPTIONS **69004 VGA / Video Interface**

Pin #	Pin Name	Type	Active	Description	
65	YRIN0	In	Both	Luminance/Red Data from the digital video source. This data is buffered and stored in the VRAM for Video output.	
64	YRIN1	In	Both		
63	YRIN2	In	Both		
62	YRIN3	In	Both		
61	YRIN4	In	Both		
60	YRIN5	In	Both		
59	YRIN6	In	Both		
58	YRIN7	In	Both		
57	CGIN0	In	Both	Chrominance/Green Data from the digital video source. This data is buffered and stored in the VRAM for Video output.	
56	CGIN1	In	Both		
55	CGIN2	In	Both		
54	CGIN3	In	Both		
51	CGIN4	In	Both		
50	CGIN5	In	Both		
49	CGIN6	In	Both		
48	CGIN7	In	Both		
47	BIN0	In	Both	Blue Data from the digital video source. This data is buffered and stored in the VRAM for Video output.	
46	BIN1	In	Both		
45	BIN2	In	Both		
44	BIN3	In	Both		
43	BIN4	In	Both		
42	BIN5	In	Both		
41	BIN6	In	Both		
39	BIN7	In	Both		
114	XCLK	In	Both	Video Data Clock. This clock is to latch the Video data from the digital video source.	

PIN DESCRIPTIONS — 69004 Inter-Chip, Power, and Ground

Pin #	Pin Name	Type	Active	Description
6	IFXYW	Out	Both	Inter-Chip control signals. These pins connect to the corresponding pins on the 69003.
7	IFHBL	Out	Both	
9	IHBL	In	Both	
10	IXYW	In	Both	
11	IDTC	In	Both	
12	IEWR	In	Both	
13	IWBM	In	Both	
14	IAQREQ	In	Both	
15	IWR	In	Both	
16	IRD	In	Both	
17	IAD2	In	Both	
18	IAD1	In	Both	
19	IAD0	In	Both	
2 29 52 79	VCC	Pwr	-	+ 5V Power Pins
1 28 40 53 68 80 90	GND	Pwr	-	Ground Pins
67	NC0	-	-	Reserved. These pins should be left unconnected.
66	NC1	-	-	

Registers

REGISTER ADDRESSING

The address location of the PC Video Pro control registers is determined by the status of the CS/ input at RESET. If the CS/ input is low on the falling edge of RESET, then PC Video Pro responds to a fixed I/O address, 0AD6h, 0AD7h. If CS/ is inactive (high) then a programmable address is used. The value present on the data bus during the first valid I/O write (CS/=0, IOWR/=0) following a RESET cycle, is loaded into the Programmed I/O Address Register bits 7:0. This value is then used to determine the I/O address location for the PC Video Pro registers. Since PC Video Pro always occupies two consecutive I/O addresses, bit-0 of this register is ignored. The least significant 8 bits of the I/O address are determined by the value in the Programmed I/O register. The remaining address bits are then dependent on the external decode logic that generates the CS/ strobe.

The setup and control registers for the PC Video Pro chip occupy two consecutive address locations. The first or even location contains an index register. The index register determines or "points" to all the other registers. The second or odd location is the data port for the selected register. To access a PC Video Pro register, the index value for the desired register is written to the index register. The data for that register may then be read or written at the data register location.

There are four groups of control registers inside the PC Video Pro chip. They are CPU interface, General Purpose I/O control, Video Acquisition, and Display Window control. All registers are read/write once PC Video Pro has been enabled using bit-0 of the Global Enable Register.

CPU INTERFACE REGISTERS

These registers are used to enable/disable PC Video Pro, store the I/O address location, specify the memory address and configuration, set the buffer memory write mask and service interrupts. Bit 0 of the Global Enable Register (Index: FFh) must be set to '1' before any other registers may be read or written. This register and the Index Register are write-only until this bit is set.

GENERAL PURPOSE I/O REGISTERS

These registers control the General Purpose I/O pins and the I²C bus interface.

VIDEO ACQUISITION REGISTERS

These register are used to control acquisition of a live motion video data stream. They provide data on the current acquisition status and control the input acquisition window, scaling and storage location in memory.

DISPLAY WINDOW REGISTERS

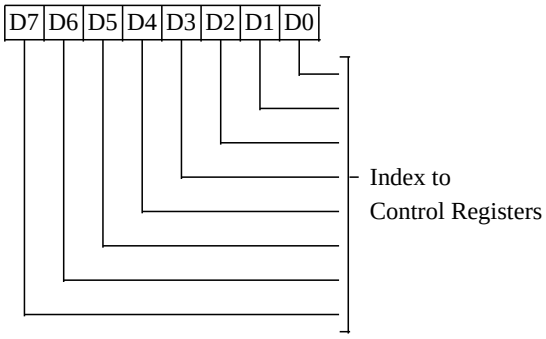
These registers are used to control the output video data stream and color keying. They provide control of the output window location and size, data start location (panning), shift clock and analog multiplexer skew and VGA color key and mask.

Control Registers

Register Mnemonic	Register Group	Register Name	Index	I/O Access	State After Reset	Page
RX	--	Control Register Index	--	RW	x x x x x x x x	25
R00	CPU Interface	I/O Address	00h	RW	1 1 0 1 1 1 0 -	25
R01	CPU Interface	Memory Access	01h	RW	0 0 0 0 - - 0 0	25
R04	CPU Interface	Data Mask, Blue Data	04h	RW	x x x x x x x x	25
R05	CPU Interface	Data Mask, Key Data	05h	RW	x x x x x x x x	26
R06	CPU Interface	Linear Memory Base Address	06h	RW	- - - 1 1 1 1 1	26
R07	CPU Interface	Data Mask, Luminance Data	07h	RW	x x x x x x x x	26
R08	CPU Interface	Data Mask, Chrominance Data	08h	RW	x x x x x x x x	26
R09	CPU Interface	Interrupt Mask	09h	RW	- R R R R R 0 0	27
R10	G.P. I/O	General Purpose I/O 0	10h	External	- - - - - - - -	28
R11	G.P. I/O	General Purpose I/O 1	11h	External	- - - - - - - -	28
R12	G.P. I/O	General Purpose I/O 2	12h	External	- - - - - - - -	28
R13	G.P. I/O	General Purpose I/O 3	13h	External	- - - - - - - -	28
R18	G.P. I/O	General Purpose I/O Control	18h	RW	0 0 0 0 0 0 1 1	28
R20	Video Acquisition	Video Acquisition Mode	20h	RW	0 - 0 0 0 0 0 0	29
R21	Video Acquisition	Acquisition Window Control	21h	RW	x x x x x x x x	29
R22	Video Acquisition	Acquisition Window, X-start Low	22h	RW	x x x x x x x x	30
R23	Video Acquisition	Acquisition Window, X-start High	23h	RW	- - - - - - x x	30
R24	Video Acquisition	Acquisition Window, Y-start Low	24h	RW	x x x x x x x x	30
R25	Video Acquisition	Acquisition Window, Y-start High	25h	RW	- - - - - - x x	30
R26	Video Acquisition	Acquisition Window, X-end Low	26h	RW	x x x x x x x x	31
R27	Video Acquisition	Acquisition Window, X-end High	27h	RW	- - - - - - x x	31
R28	Video Acquisition	Acquisition Window, Y-end Low	28h	RW	x x x x x x x x	31
R29	Video Acquisition	Acquisition Window, Y-end High	29h	RW	- - - - - - x x	31
R2A	Video Acquisition	Acquisition Address, Low	2Ah	RW	x x x x x x x x	32
R2B	Video Acquisition	Acquisition Address, Middle	2Bh	RW	x x x x x x x x	32
R2C	Video Acquisition	Acquisition Address, High	2Ch	RW	- - - x x x x x	32
R2D	Video Acquisition	Acquisition Horizontal Scale	2Dh	RW	- - x x x x x x	33
R2E	Video Acquisition	Acquisition Vertical Scale	2Eh	RW	- x x x x x x x	33
R2F	Video Acquisition	Scaling Field Adjust	2Fh	RW	- x x x x x x x	33
R30	Video Acquisition	Input Video Start	30h	RW	- - x x x x x x	33
R38	Video Acquisition	Scaling Control	38h	RW	0 - - 0 0 0 0 0	34
R40	Display Window	Display Area Control	40h	RW	0 0 0 0 0 0 0 0	34
R41	Display Window	Window X-Start, Low	41h	RW	x x x x x x x x	35
R42	Display Window	Window X-Start, High	42h	RW	- - - - - - x x	35
R43	Display Window	Window Y-Start, Low	43h	RW	x x x x x x x x	35
R44	Display Window	Window Y-Start, High	44h	RW	- - - - - - x x	35
R45	Display Window	Window X-End, Low	45h	RW	x x x x x x x x	36
R46	Display Window	Window X-End, High	46h	RW	- - - - - - x x	36
R47	Display Window	Window Y-End, Low	47h	RW	x x x x x x x x	36
R48	Display Window	Window Y-End, High	48h	RW	- - - - - - x x	36
R49	Display Window	X-Panning, Low	49h	RW	x x x x x x x x	37
R4A	Display Window	Y-Panning, Low	4Ah	RW	x x x x x x x x	37
R4B	Display Window	X,Y-Panning, High	4Bh	RW	- - x x - - - x	37
R4C	Display Window	Shift Clock	4Ch	RW	- x x x x x x x	37
R4D	Display Window	Sync Polarity Register/Zoom	4Dh	RW	- 0 0 0 0 0 0 0	38
R4E	Display Window	Color Compare	4Eh	RW	x x x x x x x x	38
R4F	Display Window	Color Mask	4Fh	RW	x x x x x x x x	38
R50	Display Window	Interlaced Output Control	50h	RW	- - - x x x x x	39
RFF	Misc	Global Enable / Version	FFh	R7:4 W2:0	0 0 1 0 - 0 0 0	39

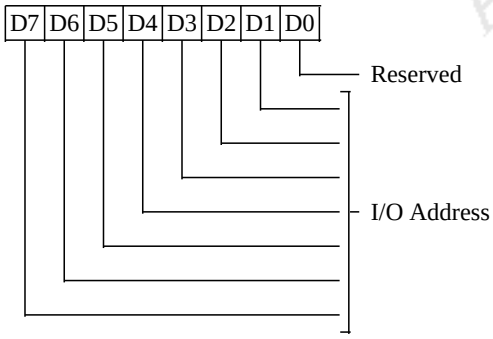
Note: Read and Write to all registers (except the Index and Global Enable Registers) is disabled until the Global Enable Bit is set. The Index and Global Enable Registers are Write only until the Global Enable Bit is set. x = Undefined state on power-up.

CONTROL REGISTER INDEX (RX)
Read/Write



7-0 Index value used to access the control registers.

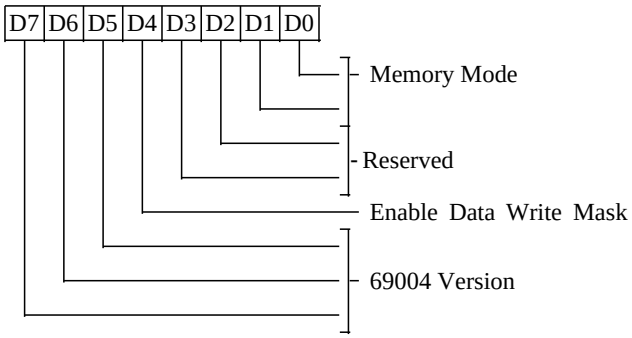
I/O ADDRESS REGISTER (R00)
Read/Write
Index 00h



0 Reserved (0)

7-1 These bits are compared with the address inputs, A7:1, to detect a valid I/O address. If CS/ is low on RESET, this register is initialized to D6h. If CS is high on RESET, this register is loaded with the value present on the data inputs (D7:1) during the first I/O write to the chip (IOWR/=0 and CS/=0).

MEMORY ACCESS REGISTER (R01)
Read/Write
Index 01h



1-0 These bits define the memory configuration:

00	1K x 512	16 bit
01	1K x 512	24 bit
10	1K x 1K	16 bit
11	1K x 512	32 bit

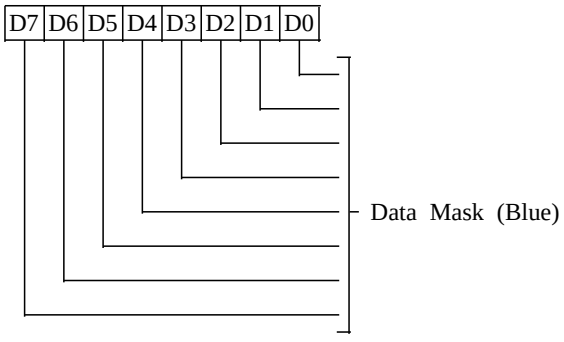
3-2 Reserved (0)

4 Enable VRAM Write Mask

0 Disabled
1 Enabled

7-5 69004 Version

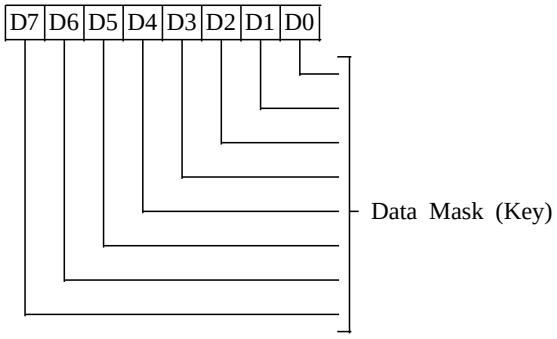
DATA MASK REGISTER, BLUE DATA (R04)
Read /Write
Index 07h



7-0 These bits control the "Write per bit" feature of the VRAMs on the blue data. A '0' in a bit position prevents the data in that bit position from being modified during video data acquisition.

DATA MASK REGISTER, KEY DATA (R05)

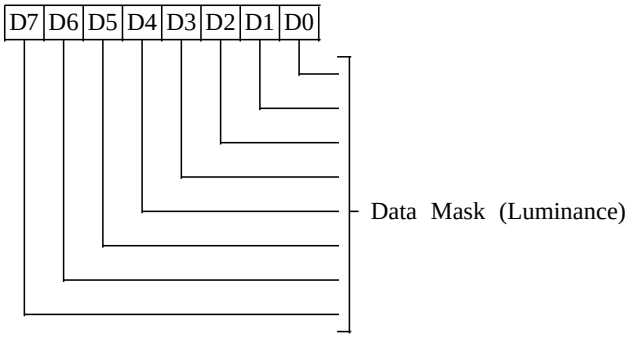
Read /Write
Index 07h



7-0 These bits control the "Write per bit" feature of the VRAMs on the key data. A '0' in a bit position prevents the data in that bit position from being modified during video data acquisition.

DATA MASK REGISTER, LUMINANCE DATA (R07)

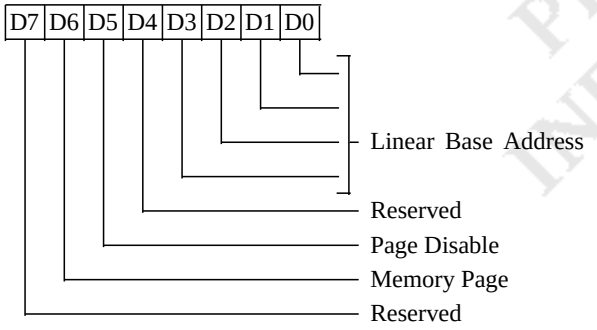
Read /Write
Index 07h



7-0 These bits control the "Write per bit" feature of the VRAMs on the luminance data. A '0' in a bit position prevents the data in that bit position from being modified during video data acquisition.

LINEAR MEMORY BASE ADDRESS REGISTER (R06)

Read /Write
Index 06h



3-0 Linear Base Address. These bits define the starting address for the linear memory space. The address space should start on 2 MByte boundaries (bit 0 = 0).

4 Reserved (0)

5 Page Disable

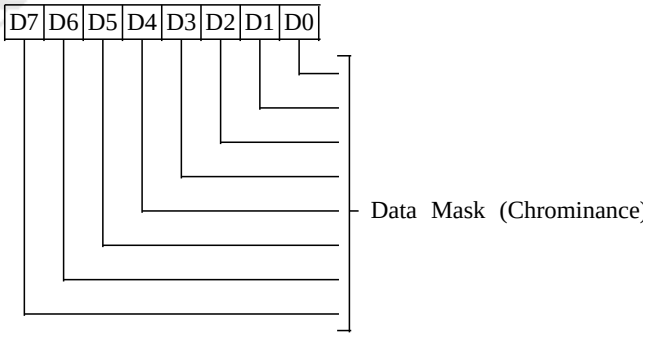
- 0 Memory paging selection is done with bit-6 of this register.
- 1 Linear Addressing, Pin LA20 selects upper or lower MByte of memory.

6 Memory Page. When bit-5 is '0' this bit selects the upper or lower MByte of image memory.

7 Reserved (0)

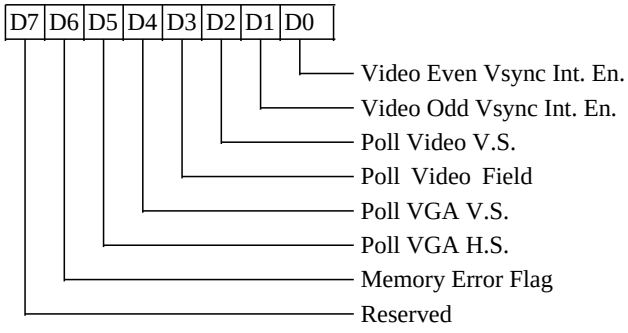
DATA MASK REGISTER, CHROMINANCE DATA (R08)

Read /Write
Index 08h



7-0 These bits control the "Write per bit" feature of the VRAMs on the chrominance data. A '0' in a bit position prevents the data in that bit position from being modified during video data acquisition.

INTERRUPT MASK REGISTER (R09)
Read /Write
Index 09h



0 Video Even Vsync Interrupt Enable.

0 Disabled
1 Enabled

1 Video Odd VSync Interrupt Enable.

0 Disable
1 Enable

2-6 These bits can be polled to monitor the status of the signals listed below.

2 Poll Video VSync
3 Poll Video Field (0=Even; 1=Odd)
4 Poll VGA VSync
5 Poll VGA HSync
6 Memory Error Flag. Set when Display memory is incorrectly accessed during acquisition. Writting a zero to this bit clears this flag. This bit is reset on power up.

7 Reserved (0)

GENERAL PURPOSE I/O REGISTER 0 (R10)
I/O at Index 10h

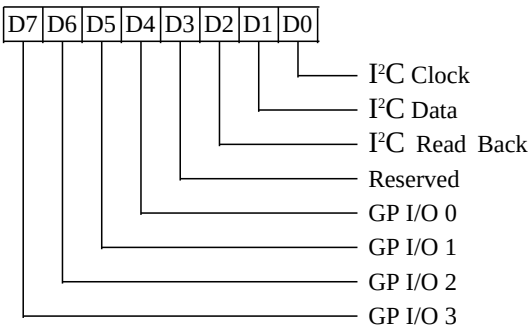
GENERAL PURPOSE I/O REGISTER 1 (R11)
I/O at Index 11h

GENERAL PURPOSE I/O REGISTER 2 (R12)
I/O at Index 12h

GENERAL PURPOSE I/O REGISTER 3 (R13)
I/O at Index 13h

These four registers are implemented through external latches and/or buffers. If enabled through the General Purpose I/O Control register, a strobe is generated on the appropriate GP I/O pin when a read or write occurs to that register. The external logic is responsible for latching the data from or driving to the system bus as needed. The data transceiver control signals are active for these I/O cycles.

GENERAL PURPOSE I/O CONTROL REGISTER (R18)
Read /Write
Index 18h



0 I²C Bus Clock

1 I²C Bus Data

Bits 0 and 1 are designed to control the I²C bus. They are connected to their respective I²C output pins. The status of these bits are reflected at the output. When read, the data returned is the value present on the pins. Since these outputs are open collector, the input may be pulled low by other signals.

2 I²C bus read back input pin I2CI. This pin should be tied to I2CO. This bit reflects status of I2CI pin when I2CK pin goes from '0' to '1'.

3 Reserved (0)

4 General Purpose I/O 0

0 Output decode of R10 on GPIO0
1 Reserved

5 General Purpose I/O 1

0 Output "PLLHREF" on GPIO1
1 Output decode of R11 on GPIO1

6 General Purpose I/O 2

0 Output decode of R12 on GPIO2
1 Reserved

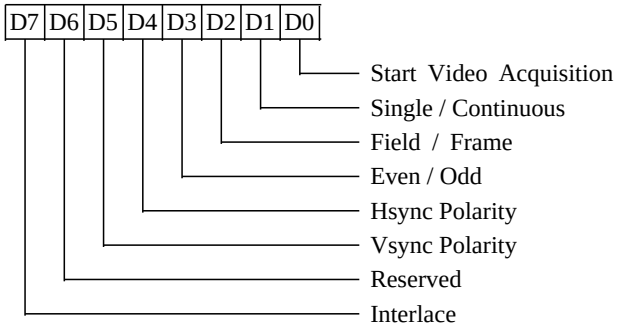
7 General Purpose I/O 3

0 Output decode of R13 on GPIO3
1 Reserved

Note: Bits 4, 6, and 7 should be programmed to 0 for correct operation.

VIDEO ACQUISITION MODE REGISTER (R20)

Read /Write
Index 20h



0 Start Video Acquisition

- 0 Stop Video Acquisition and allow CPU access to the frame buffer.
- 1 Start Video Acquisition. The type of acquisition, continuous/single frame, interlaced, etc. is determined by bits 1-3 of this register.

During continuous acquisition the memory is available during the verticle blanking interval and at the data under the "cropping" window. Software must read back this bit as a 0 to ensure access to the frame buffer after stopping video acquisition.

1 Single / Continuous

- 0 Continuous video acquisition
- 1 Acquire a single field or frame (as determined by bits 2&3). Bit-0 of this register is cleared at the end of a field or frame.

2 Field / Frame

- 0 Acquire input video frame
- 1 Acquire input video field (interlaced mode only)

3 Even / odd

- 0 Acquire a even (first) field
- 1 Acquire a odd (second) field

4 Hsync Polarity

- 0 Video Hsync input is active low
- 1 Video Hsync input is active high

5 Vsync Polarity

- 0 Video Vsync input is active low
- 1 Video Vsync input is active high

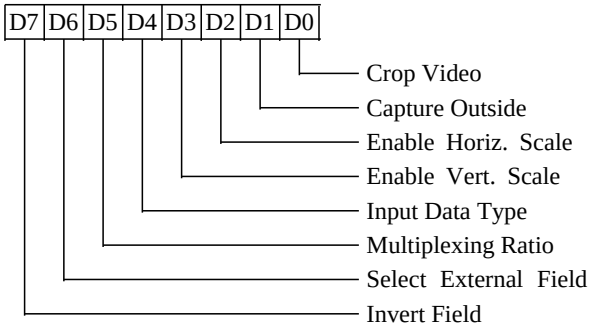
6 Reserved (0)

7 Interlace

- 0 Input video is interlaced
- 1 Input video is non-interlaced

ACQUISITION WINDOW CONTROL REGISTER (R21)

Read /Write
Index 21h



0 Video Input Cropping

- 0 Disabled
- 1 Enabled

1 Video Capture

- 0 Capture video inside cropping window
- 1 Capture video outside cropping window

2 Video Input Scaling, Horizontal

- 0 Disabled
- 1 Enabled

3 Video Input Scaling, Vertical

- 0 Disabled
- 1 Enabled

4 Video Input Data Multiplexing. This bit determines whether input data is multiplexed or non-multiplexed, ie. YUV or RGB.

- 0 Multiplexed (YUV)
- 1 Non-multiplexed (RGB)

5 Multiplexing Ratio. This bit determines the multiplexing ratio for the luma and chroma input data. It is active only if bit-4 is '0'.

- 0 4:1:1 / 2:1:1
- 1 4:2:2

6 Select External Field

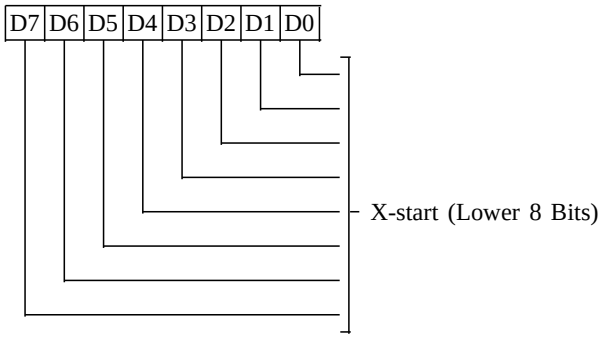
- 0 Internal Field. The field is detected one clock after the trailing edge of the XVSYNC input pin.
- 1 Field bit is input through the XFIELD pin, and reclocked by XCLK before use. XFIELD input should transition after the trailing edge of XVSYNC. A '0' on XFIELD indicates the "even field" and '1' indicates "odd field".

7 Invert Field. Inverts the polarity of either internally or externally generated field bit.

- 0 Field bit unmodified
- 1 Field polarity inverted

ACQUISITION WINDOW, X-START LOW BYTE REGISTER (R22)

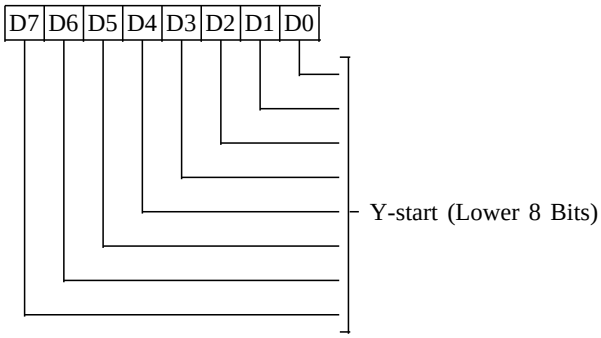
Read /Write
Index 22h



7-0 The eight low order bits of a 10-bit register. This value defines the start of the video acquisition horizontally. This value is measured in input pixel clocks and is referenced to the trailing edge of the video Hsync.

ACQUISITION WINDOW, Y-START LOW BYTE REGISTER (R24)

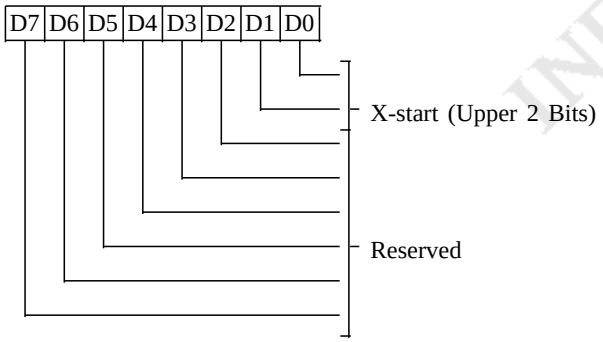
Read /Write
Index 24h



7-0 The eight low order bits of a 10-bit register. This value defines the start of the video acquisition vertically. This value is measured in input lines and is referenced to the trailing edge of the video Vsync + V Start Adjust (R30).

ACQUISITION WINDOW, X-START HIGH BYTE REGISTER (R23)

Read /Write
Index 23h

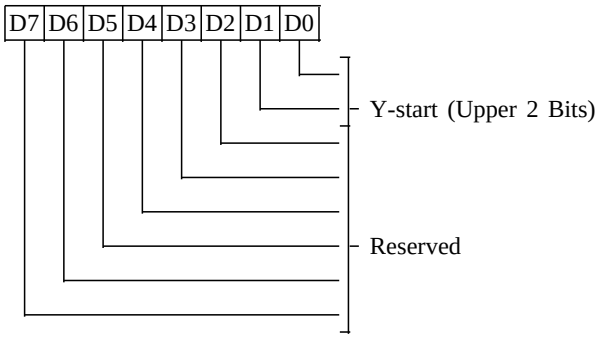


1-0 The two high order bits of a 10-bit register. This value defines the start of the video acquisition horizontally. This value is measured in input pixel clocks and is referenced to the trailing edge of the video Hsync.

7-2 Reserved (0)

ACQUISITION WINDOW, Y-START HIGH BYTE REGISTER (R25)

Read /Write
Index 25h

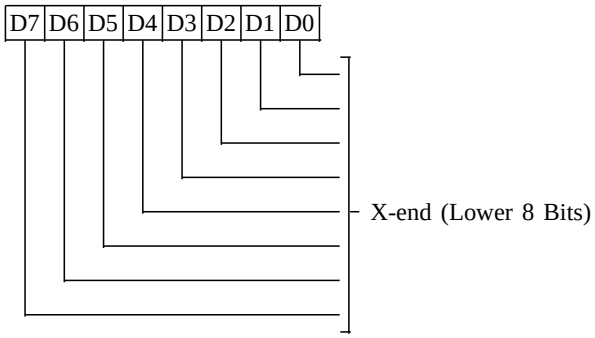


1-0 The two high order bits of a 10-bit register. This value defines the start of the video acquisition horizontally. This value is measured in input lines and is referenced to the trailing edge of the video Vsync + V Start Adjust (R30).

7-2 Reserved (0)

ACQUISITION WINDOW, X-END LOW BYTE REGISTER (R26)

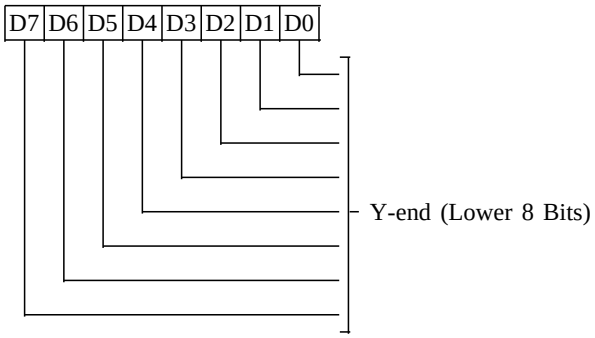
Read /Write
Index 26h



7-0 The eight low order bits of a 10-bit register. This value defines the end of the video acquisition horizontally. This value is measured in input pixel clocks and is referenced to the trailing edge of the video Hsync.

ACQUISITION WINDOW, Y-END LOW BYTE REGISTER (R28)

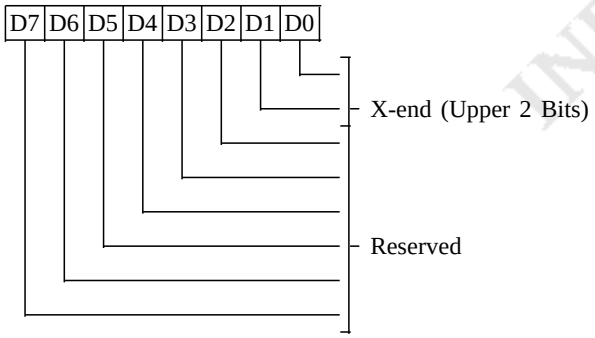
Read /Write
Index 28h



7-0 The eight low order bits of a 10-bit register. This value defines the end of the video acquisition vertically. This value is measured in input lines and is referenced to the trailing edge of the video Vsync + V Start Adjust (R30).

ACQUISITION WINDOW, X-END HIGH BYTE REGISTER (R27)

Read /Write
Index 27h

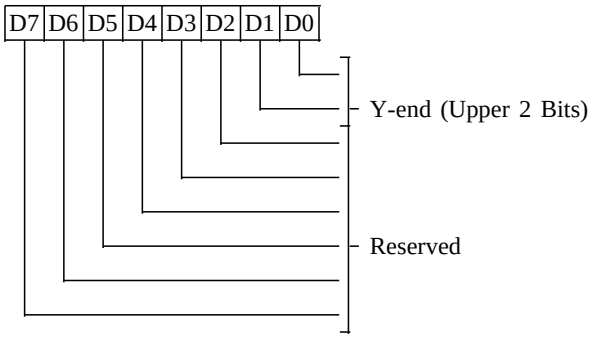


1-0 The two high order bits of a 10-bit register. This value defines the end of the video acquisition horizontally. This value is measured in input pixel clocks and is referenced to the trailing edge of the video Hsync.

7-2 Reserved (0)

ACQUISITION WINDOW, Y-END HIGH BYTE REGISTER (R29)

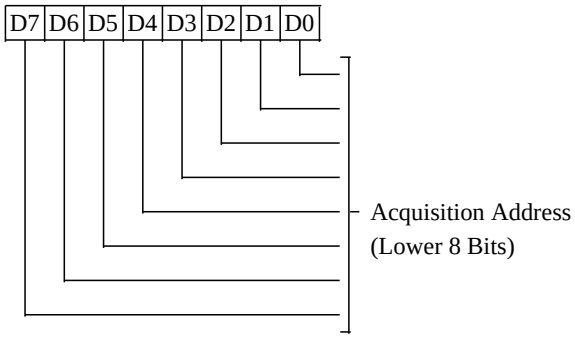
Read /Write
Index 29h



1-0 The two high order bits of a 10-bit register. This value defines the end of the video acquisition horizontally. This value is measured in input lines and is referenced to the trailing edge of the video Vsync + V Start Adjust (R30).

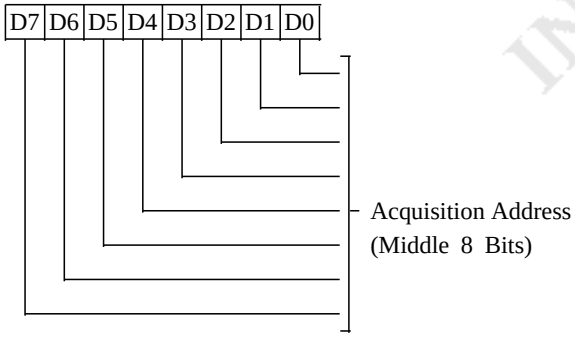
7-2 Reserved (0)

ACQUISITION ADDRESS LOW REGISTER (R2A)
Read /Write
Index 2Ah



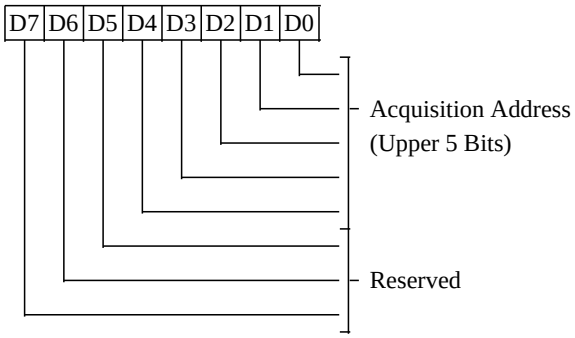
7-0 The eight low order bits of a 20-bit pointer. This value points to the frame memory location where video acquisition starts. This is a linear address. At the end of a video line, the address is reset to the beginning of the line and an offset of 1024 bytes is added to form the start address for the next line.

ACQUISITION ADDRESS MIDDLE REGISTER (R2B)
Read /Write
Index 2Bh



7-0 The eight middle bits of a 20-bit pointer. This value points to the frame memory location where video acquisition starts. This is a linear address. At the end of a video line, the address is reset to the beginning of the line and an offset of 1024 bytes is added to form the start address for the next line.

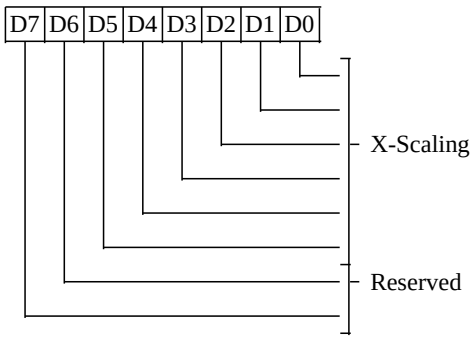
ACQUISITION ADDRESS UPPER REGISTER (R2C)
Read /Write
Index 2Ch



7-0 The five upper order bits of a 21-bit pointer. This value points to the frame memory location where video acquisition starts. This is a linear address. At the end of a video line, the address is reset to the beginning of the line and an offset of 1024 bytes is added to form the start address for the next line.

ACQUISITION HORIZONTAL-SCALING REGISTER (R2D)

Read /Write
Index 2Dh

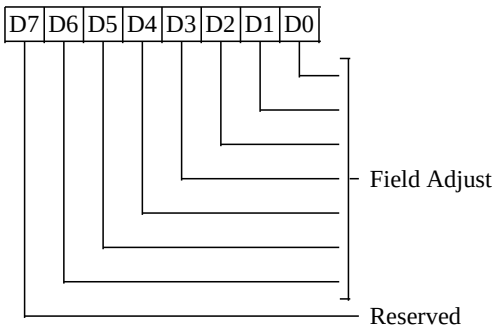


5-0 These bits define the number of pixels written per 64 input pixels. Valid values are 1-63. Horizontal scaling is disabled through R21 bit 2.

7-6 Reserved (0)

SCALING FIELD ADJUST REGISTER (R2F)

Read /Write
Index 2Fh

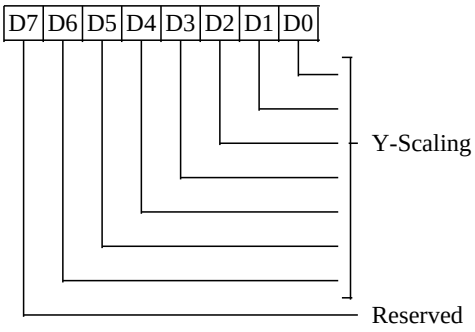


6-0 Modifies scaling value for odd field during acquisition. This is a diagnostic register and should be set to the same value as the Y-scaling register R2E for normal operation.

7 Reserved (0)

ACQUISITION VERTICAL-SCALING REGISTER (R2E)

Read /Write
Index 2Eh

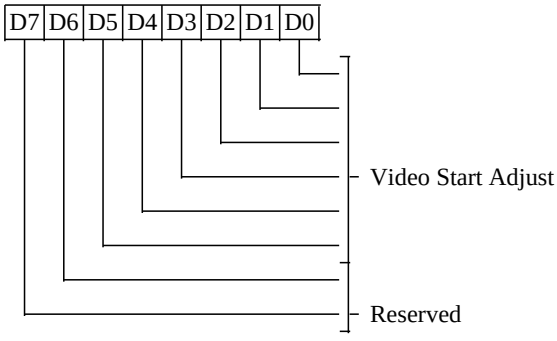


6-0 These bits define the number of lines written per 64 input lines. Valid values are 1-63. Vertical scaling is disabled through R21 bit 3.

7 Reserved (0)

INPUT VIDEO START ADJUST (R30)

Read /Write
Index 30h

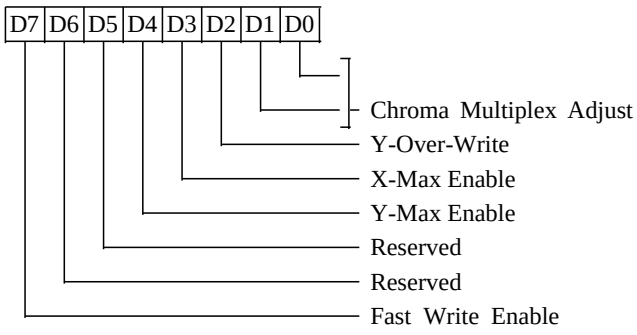


5-0 This register specifies the number of scan lines from the trailing edge of video Vsync to the start of active video frame.

7-6 Reserved (0)

SCALING CONTROL REGISTER (R38)

Read /Write
Index 38h



1-0 Chroma Multiplex Adjust Bits. These two bits provide adjustments to maintain luma/chroma alignment.

2 Y-Over-Write Mode. This bit is used with vertical scaling of less than 1/2 to reduce the motion artifacts caused by moving images with interfield movement. When scaling by less than 1/2, both the Field Grab bit and this bit should be set to '1'. This results in writing a scaled image from only one of the video fields.

0 Normal scaling
1 Modifed scaling

3 X-Max Enable. This bit prevents wrap around of memory X-address.

0 Disabled
1 Enabled

4 Y-Max Enable. This bit prevents wrap around of memory Y-address. This bit should be enabled for PAL video data.

0 Disabled
1 Enabled

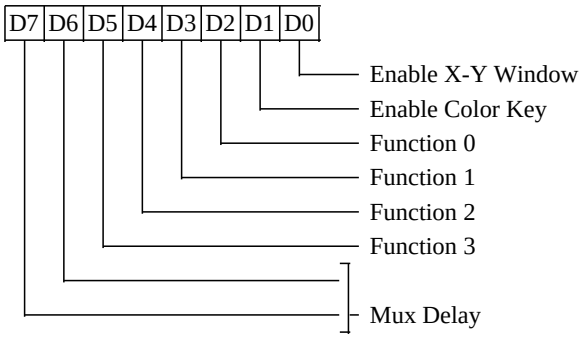
5 Reserved. (0) Should be set to '0' for normal operation.

6 Reserved. (0) Should be set to '0' for normal operation.

7 Fast Write Enable. When this bit is set to '1', CPURDY is asserted one clock earlier to improve the CPU memory write cycle speed. This bit defaults to '0' on RESET.

DISPLAY AREA CONTROL REGISTER (R40)

Read /Write
Index 40h



0 Overlay Window using an X-Y Window

0 Disabled
1 Enabled

1 Overlay Window using Color Keying

0 Disabled
1 Enabled

2 Non-color key or X-Y Window area (Function 0).

0 Display VGA
1 Display Frame Buffer Data

3 X-Y Window only area. (Function 1) This area does not exist if bit-0 of this register is '0'.

0 Display VGA
1 Display Frame Buffer Data

4 Color Key only area. (Function 2) This area does not exist if bit-1 of this register is '0'.

0 Display VGA
1 Display Frame Buffer Data

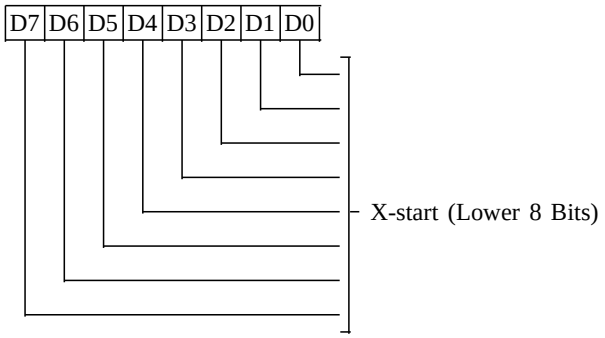
5 Both X-Y Window and Color Key area. (Function 3) This area does not exist if either bits-0 or 1 of this register are '0'.

0 Display VGA
1 Display Frame Buffer Data

7-6 These bits define the skew between the VGA data input and the multiplexer control output in VGA clocks.

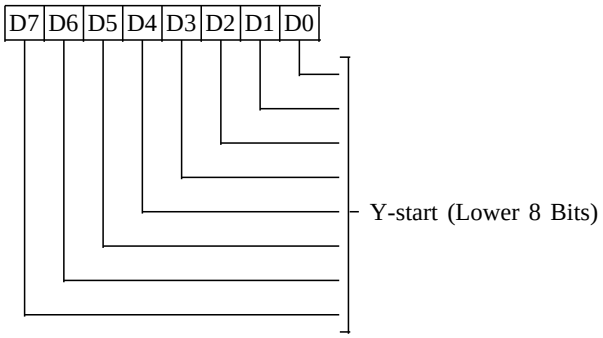
00 2 VGA clock delay
01 3 VGA clock delay
10 4 VGA clock delay
11 5 VGA clock delay

DISPLAY WINDOW,
X-START LOW BYTE REGISTER (R41)
Read /Write
Index 41h



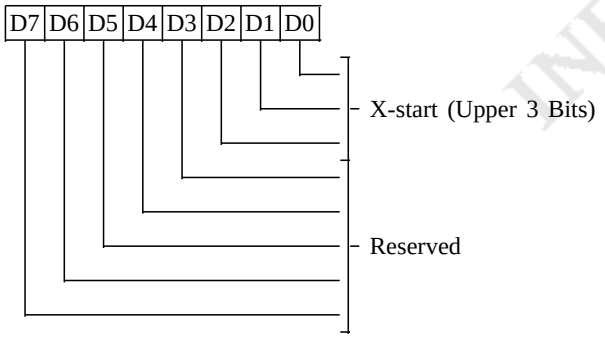
7-0 The eight low order bits of a 11-bit register. This value defines the start of the video display window, horizontally. This value is measured in VGA pixel clocks and is referenced to the trailing edge of the VGA Hsync.

DISPLAY WINDOW,
Y-START LOW BYTE REGISTER (R43)
Read /Write
Index 43h



7-0 The eight low order bits of a 10-bit register. This value defines the start of the video display window, vertically. This value is measured in VGA lines and is referenced to the trailing edge of the VGA Vsync.

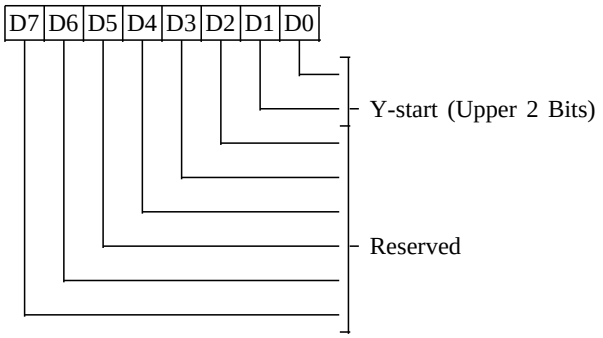
DISPLAY WINDOW,
X-START HIGH BYTE REGISTER (R42)
Read /Write
Index 42h



2-0 The three high order bits of a 11-bit register. This value defines the start of the video display window, horizontally. This value is measured in VGA pixel clocks and is referenced to the trailing edge of the VGA Hsync.

7-3 Reserved (0)

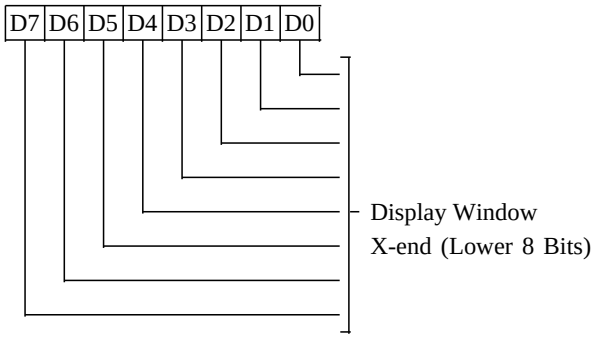
DISPLAY WINDOW,
Y-START HIGH BYTE REGISTER (R44)
Read /Write
Index 44h



1-0 The two high order bits of a 10-bit register. This value defines the start of the video display window, horizontally. This value is measured in VGA lines and is referenced to the trailing edge of the VGA Vsync.

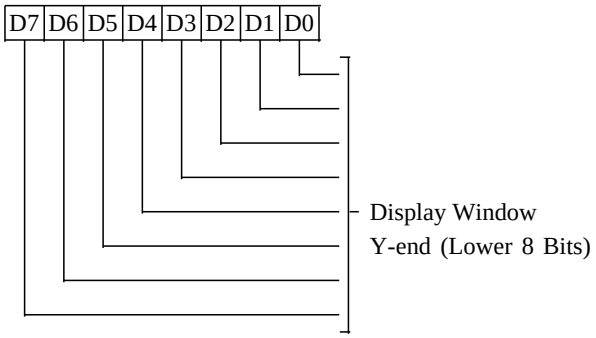
7-2 Reserved (0)

DISPLAY WINDOW,
X-END LOW BYTE REGISTER (R45)
Read /Write
Index 45h



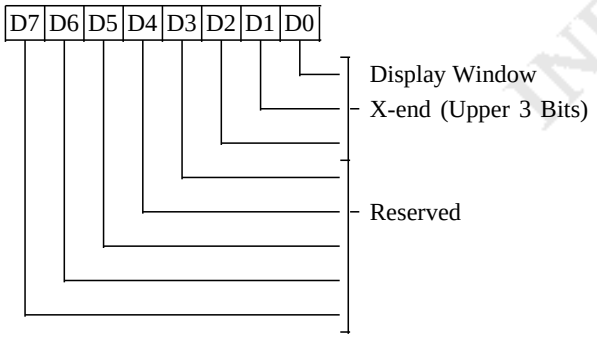
7-0 The eight low order bits of a 11-bit register. This value defines the end of the video display window, horizontally. This value is measured in VGA pixel clocks and is referenced to the trailing edge of the VGA Hsync.

DISPLAY WINDOW,
Y-END LOW BYTE REGISTER (R47)
Read /Write
Index 47h



7-0 The eight low order bits of a 10-bit register. This value defines the end of the video display window, vertically. This value is measured in VGA lines and is referenced to the trailing edge of the VGA Vsync.

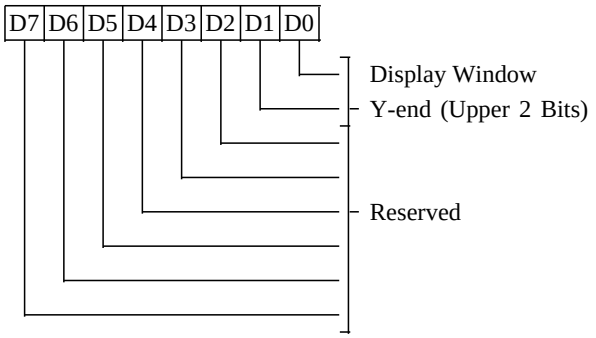
DISPLAY WINDOW,
X-END HIGH BYTE REGISTER (R46)
Read /Write
Index 46h



2-0 The three high order bits of a 11-bit register. This value defines the end of the video display window, horizontally. This value is measured in VGA pixel clocks and is referenced to the trailing edge of the VGA Hsync.

7-3 Reserved (0)

DISPLAY WINDOW,
Y-END HIGH BYTE REGISTER (R48)
Read /Write
Index 48h

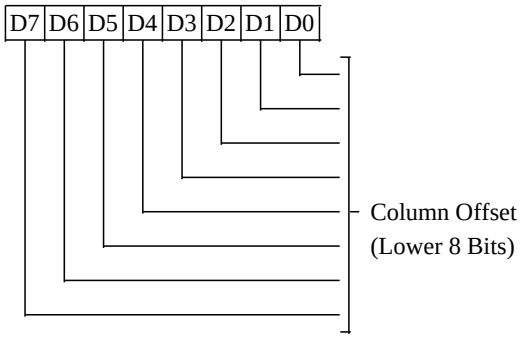


1-0 The two high order bits of a 10-bit register. This value defines the end of the video display window, horizontally. This value is measured in VGA lines and is referenced to the trailing edge of the VGA Vsync.

7-2 Reserved (0)

X-PANNING, LOW REGISTER (R49)

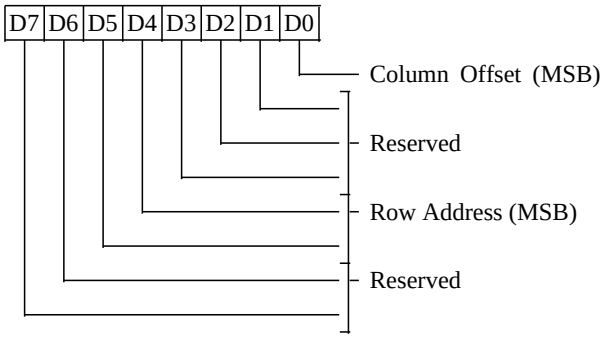
Read /Write
Index 49h



7-0 The eight low order bits of a 9-bit offset. This value defines the display buffer column address * 2 which is loaded during the data transfer cycle in the VRAMs. For 4:1:1 encoding, bit-0 of this register should be set to '0'.

X, Y - PANNING, HIGH REGISTER (R4B)

Read /Write
Index 4Bh



0 The MSB of the Column offset. See R49.

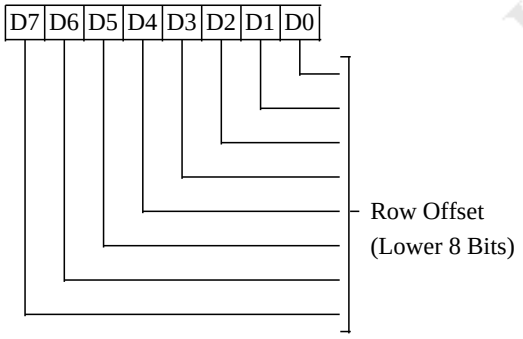
3-1 Reserved (0)

4-5 The two upper bits of the Row offset. See R4A.

7-6 Reserved (0)

Y-PANNING, LOW REGISTER (R4A)

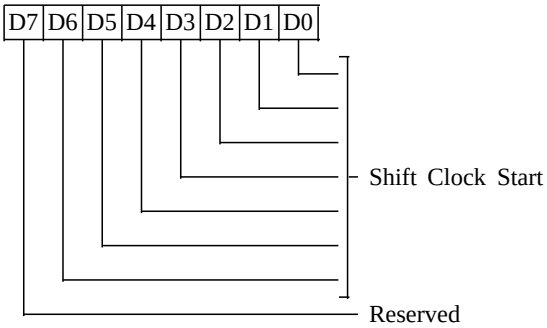
Read /Write
Index 4Ah



7-0 The eight low order bits of a 9-bit offset. This value defines the display buffer row which is loaded for the first active display line.

SHIFT CLOCK START REGISTER (R4C)

Read /Write
Index 4Ch

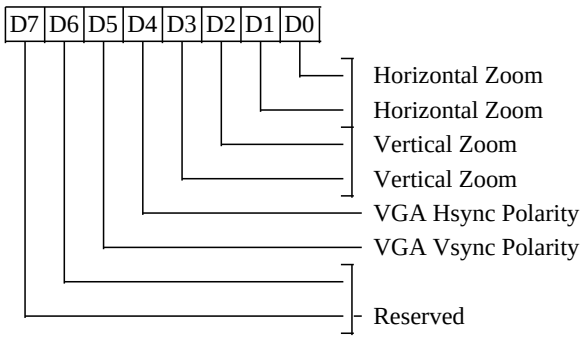


6-1 These bits define the end of the display blank relative to the VGA Hsync trailing edge. The shift clock skew is handled internally.

7 Reserved (0)

SYNC POLARITY REGISTER (R4D)

Read/Write
Index 4Dh



1-0 Horizontal Zoom

00 No Zoom
01 2X
10 4X
11 8X

3-2 Vertical Zoom

00 No Zoom
01 2X
10 4X
11 8X

4 VGA Hsync polarity

0 The VGA Hsync is active low
1 The VGA Hsync is active high

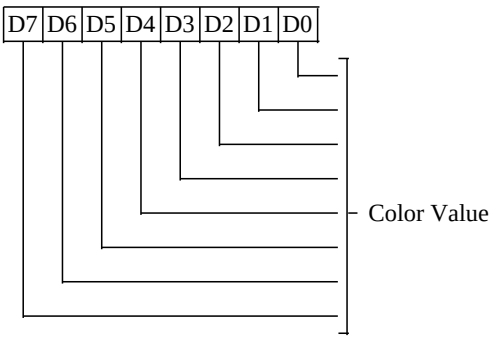
5 VGA Vsync polarity

0 The VGA Vsync is active low
1 The VGA Vsync is active high

7-6 Reserved (0)

COLOR COMPARE REGISTER (R4E)

Read /Write
Index 4Eh

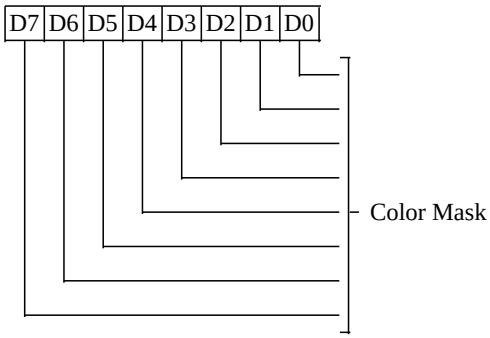


7-0 These bits define the values the VGA data must have for a color match to occur.

0 VGA data must be '0'
1 VGA data must be '1'

COLOR MASK REGISTER (R4F)

Read /Write
Index 4Fh

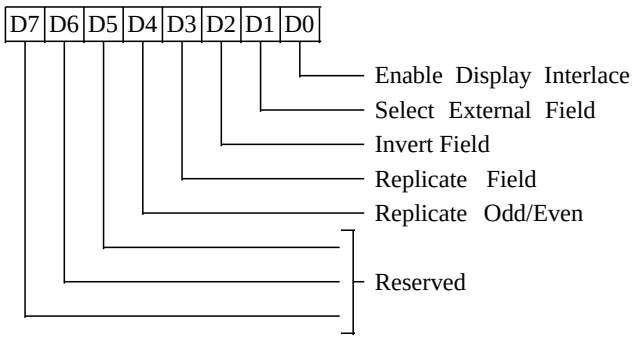


7-0 These bits define the bit position where the VGA and the color value that must match.

0 This bit position in the VGA data must match the color value.
1 This bit position in the VGA data is "don't care".

DISPLAY WINDOW INTERLACE CONTROL (R50)

Read /Write
Index 50h



0 Enable Display Interlace

- 0 Display Window is non-interlaced
- 1 Display Window is interlaced

1 Select External Field

- 0 Use internally generated field signal for display window
- 1 Select VFLD input for display window field signal

2 Invert Field

- 0 Do not modify field signal polarity
- 1 Invert display window field signal polarity

3 Replicate Field

- 0 Do not replicate field
- 1 Replicate even or odd field depending on Bit 4

4 Replicate Odd/Even

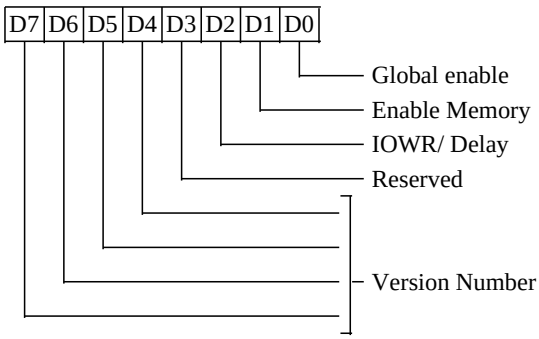
- 0 Replicate even field if Bit 3 is set
- 1 Replicate odd field if Bit 3 is set

7-5 Reserved (0)

Note: Bits 1-2 effective only if Bit 0 = '1'. If Bit 1 is '0' then internal logic will determine the field by sampling HSYNC level 4 PCLKs after the leading edge of VSYNC - Even field if HSYNC is low, Odd field if HSYNC is high.

CHIPS VERSION/ENABLE REGISTER (RFF)

Read /Write
Index FFh



0 PC Video Pro Global Enable. This bit must be set for access to any otherPC Video Pro registers. This bit is not readable.

- 0 All registers, except the Index and Global Enable registers, are disabled. The Index and Global Enabled registers are write only.
- 1 All registers, including the Index and Global Enable registers, are enabled for both read and write.

1 Enable Memory. This bit is not readable.

2 IOWR/Delay

- 0 IOWR/ input is delayed inside chip by 2 XCLK cycles.
- 1 IOWR/ input is not delayed.

3 Reserved (0)

7-4 These bits contain the version number for 69003. Values start at 0 and are incremented for every silicon step.

Electrical Specifications

ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Units
P_D	Power Dissipation	–	1	W
V_{CC}	Supply Voltage	–0.5	7	V
V_I	Input Voltage	–0.5	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	85	° C
T_{STG}	Storage Temperature	–40	125	° C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
T_A	Ambient Temperature	0	55	° C

DC CHARACTERISTICS

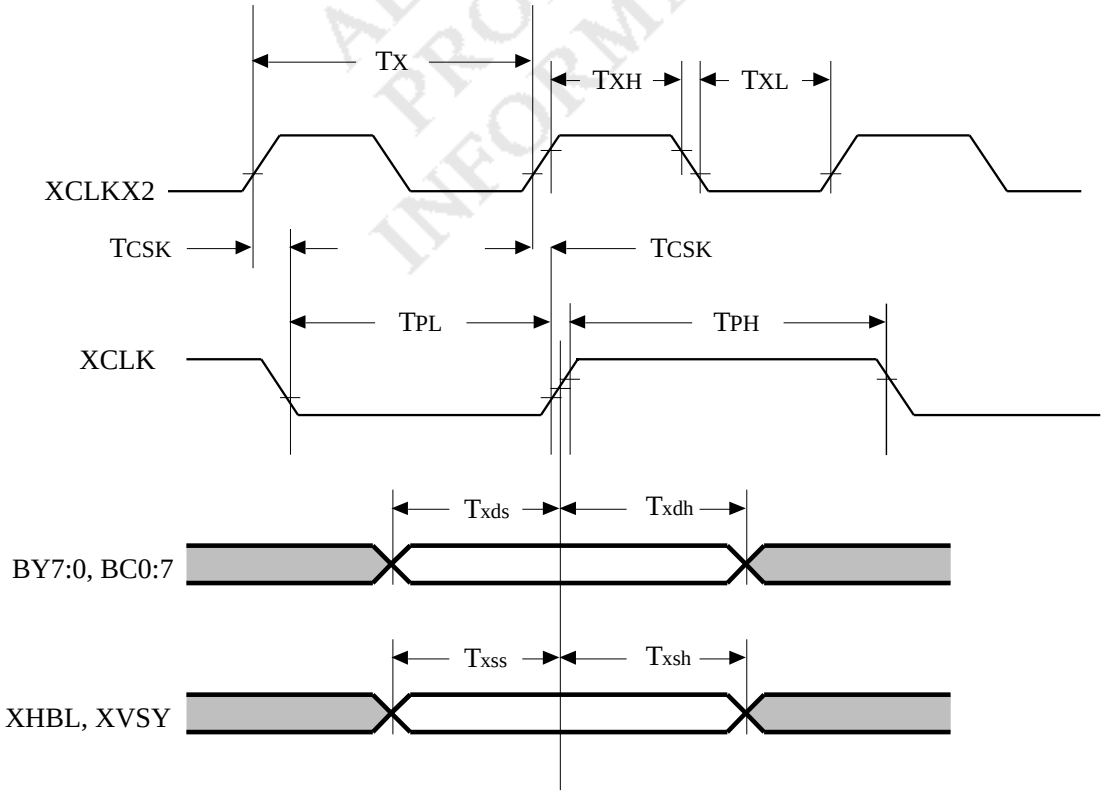
(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC1}	Power Supply Current	@27 MHz CLK, 0°C, 5.25V	–	100	mA
I_{IL}	Input Leakage Current		–10	+10	uA
I_{OZ}	Output Leakage Current	High Impedance	–10	+10	uA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL}=18mA (RDY, MEMCS16/)	–	0.45	V
		I_{OL} = 13.5 mA (I2CK, I2CO)	–	0.45	V
		I_{OL} = 9 mA (all other signals)	–	0.45	V
V_{OH}	Output High Voltage	I_{OH}=10mA (RDY, MEMSC16/)	2.4	–	V
V_{OH}	Output High Voltage	I_{OH} = 5.0 mA (all other signals)	2.4	–	V

Timing specifications are from simulation and not actually characterized. Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHARACTERISTICS - INPUT VIDEO TIMING

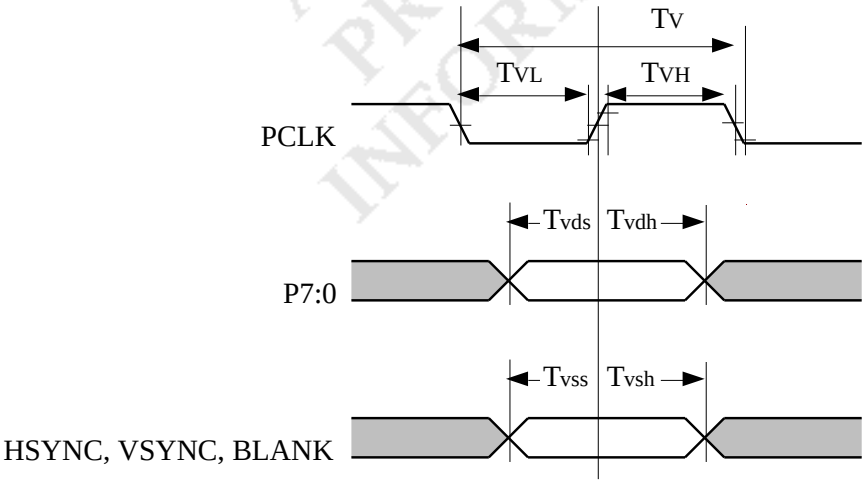
Symbol	Parameter	Notes	Min	Typ.	Max	Units
T_P	XCLK Period	13.5 MHz Typ	66	74	80	nS
T_{PH}	XCLK High Time		$0.45T_P$	–	$0.55T_P$	nS
T_{PL}	XCLK Low Time		$0.45T_P$	–	$0.55T_P$	nS
T_X	XCLKX2 Period	27.0 MHz Typ	T_P / 2	37	T_P / 2	nS
T_{XH}	XCLKX2 High Time		$0.45T_X$	–	$0.55T_X$	nS
T_{XL}	XCLKX2 Low Time		$0.45T_X$	–	$0.55T_X$	nS
Txss	XVSY setup to XCLK rising edge		12	–	–	nS
Txsh	XVSY hold from XCLK rising edge		0	–	–	nS
Txss	XHBL setup to XCLK rising edge		12	–	–	nS
Txsh	XHBL hold from XCLK rising edge		0	–	–	nS
Txds	BY 7:0, BC 7:0 setup to XCLK rising edge		10	–	–	nS
Txdh	BY 7:0, BC 7:0 setup to XCLK rising edge		0	–	–	nS
Tcsk	XCLKX2 to XCLK skew required		0	–	10	nS
Trst	Reset Pulse Width		$64T_X$	–	–	nS



PC Video Pro Input Video Timing

AC TIMING CHARACTERISTICS - VGA INPUT TIMING

Symbol	Parameter	Notes	Min	Typ.	Max	Units
T_V	PCLK Period		–	–	45	Mhz
T_{VH}	PCLK High Time		$0.45T_V$	–	$0.55T_V$	nS
T_{VL}	PCLK Low Time		$0.45T_V$	–	$0.55T_V$	nS
Tvss	HSYNC setup to XCLKX2 rising edge		6	–	–	nS
Tvsh	HSYNC hold from XCLKX2 rising edge		4	–	–	nS
Tvss	VSYNC setup to XCLKX2 rising edge		6	–	–	nS
Tvsh	VSYNC hold from XCLKX2 rising edge		4	–	–	nS
Tvss	BLANK setup to XCLKX2 rising edge		6	–	–	nS
Tvsh	BLANK hold from XCLKX2 rising edge		4	–	–	nS
Tvds	P7:0 setup to XCLKX2 rising edge		6	–	–	nS
Tvdh	P7:0 hold from XCLKX2 rising edge		4	–	–	nS
F vhmax	Maximum VGA HYSNC rate for stable NTSC Source		–	–	63	kHz
F vhmax	Maximum VGA HSYNC rate for stable PAL Source		–	–	63	kHz

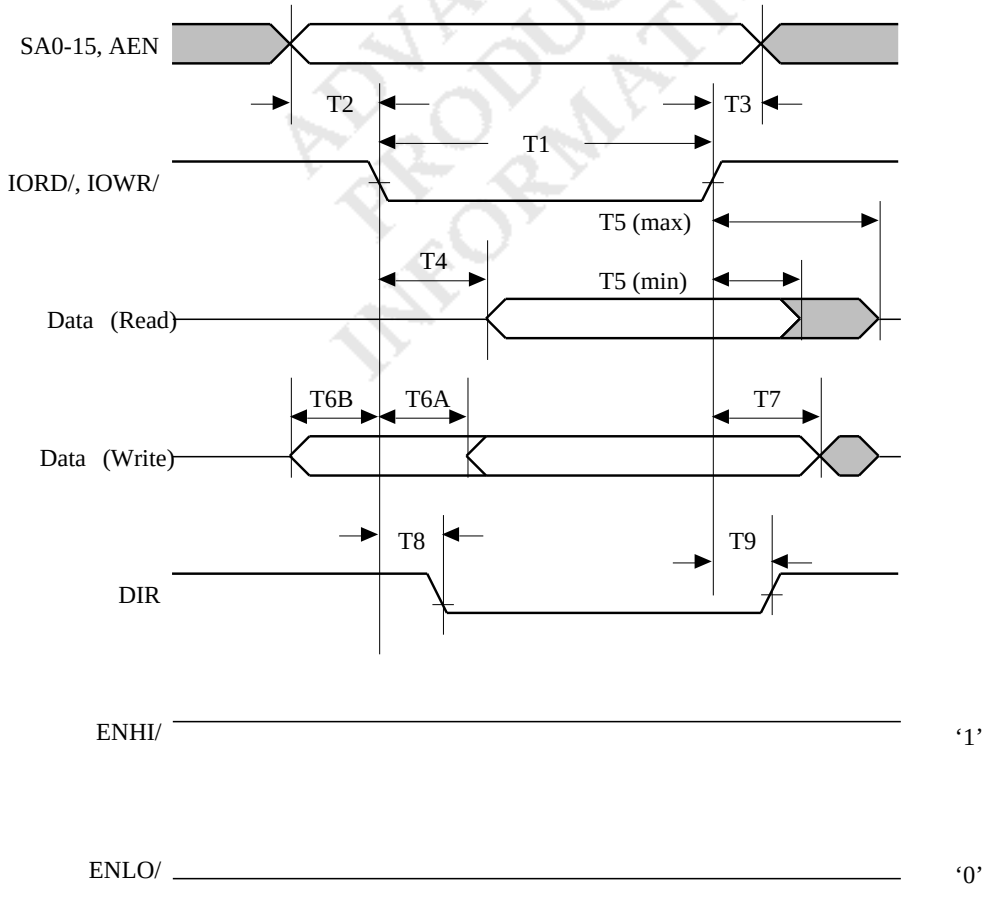


PC Video Pro VGA Input Timing

AC TIMING CHARACTERISTICS - ISA BUS I/O TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T1A	IORD/, IOWR/ Pulse Width (Reg. FF Bit 3 = '0')	Note 1	$2T_p$+ 20 ns	–	–	nS
T1B	IORD/, IOWR/ Pulse Width (Reg. FF Bit 3 = '1')	Note 1	175			
T2	Address setup to IORD, IOWR/		90	–	–	nS
T3	Address hold from IORD, IOWR/		0	–	–	nS
T4	I/O Read Data delay from IORD/		-	–	50	nS
T5	I/O Read Data hold from IORD/		0	–	30	nS
T6A	I/O Write Data setup to IOWR (Reg. FF Bit 3 = '0')	Note 1	$2T_p$	–	–	nS
T6B	I/O Write Data setup to IOWR (Reg. FF Bit 3 = '1')	Note 1	22	–	–	nS
T7	I/O Write Data hold from IOWR/		0	–	–	nS
T8	IORD/ falling to DIR valid		-	-	10	nS
T9	IORD/ rising to DIR valid		-	-	10	nS

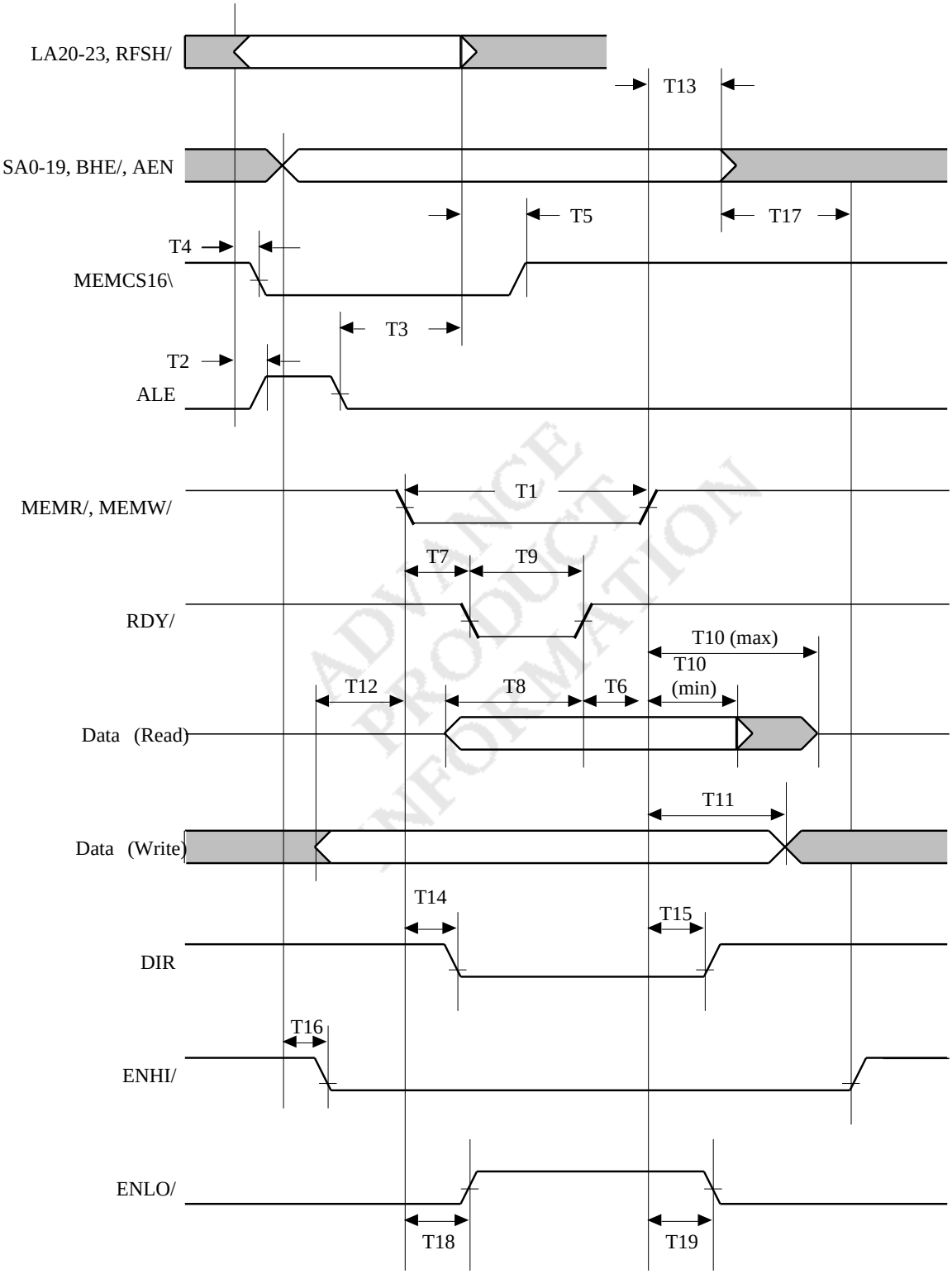
Note 1: See Register FF decription.



ISA Bus I/O Cycle Timing

AC TIMING CHARACTERISTICS - ISA BUS TIMING

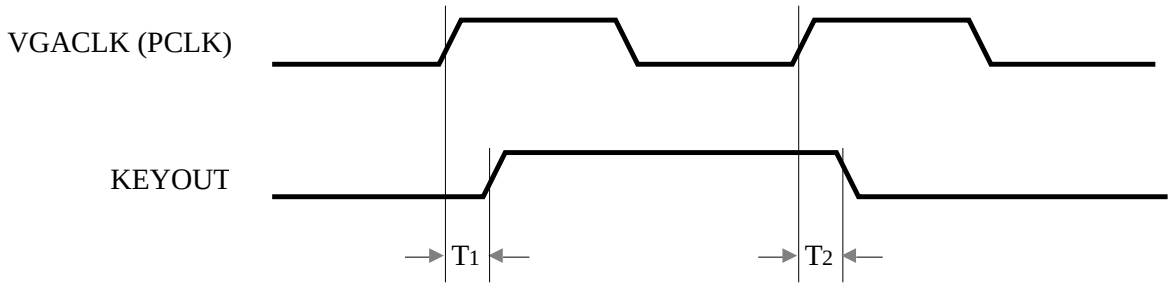
Symbol	Parameter	Notes	Min	Typ	Max	Units
T1	MEMR/, MEMW/ Pulse Width		175	–	–	nS
T2	Address setup to ALE		20	–	–	nS
T3	Address hold from ALE		0	–	–	nS
T6	MEMR/, MEMW/ hold from RDY (Memory)		0	–	-	nS
T10	Memory Read Data Holdfrom MEMR/		10	–	30	nS
T11	Memory Write Data Holdfrom MEMR/		0	–	–	nS
T7	MEMR/, MEMW/ to RDY Low Delay		-	–	25	nS
T8	Memory Read Data setup to RDY		25	-	-	nS
T9	RDY width		$8T_X$	-	$24T_X$	nS
T4	LA invalid to MEMCS16 Low Delay		-	-	20	nS
T5	LA invalid to MEMCS16 High Delay		-	-	20	nS
T12	Memory Write Data Setup to MEMW/		-40	-	-	nS
T13	SA Hold from MEmr/, MEMW/		20	-	-	nS
T14	MEMR/ falling to DIR valid		-	-	10	nS
T15	MEMR/ rising to DIR invalid		-	-	10	nS
T16	BHE falling to ENHI/ valid		-	-	10	nS
T17	BHE rising to ENHI/ invalid		-	-	10	nS
T18	MEMR/, MEMW/ to ENLO/ valid		-	-	10	nS
T19	MEMR/, MEMW/ to ENLO/ invalid		-	-	10	nS



ISA Bus Timing

AC TIMING CHARACTERISTICS - VGA Pixel Clock to KEYO Timing

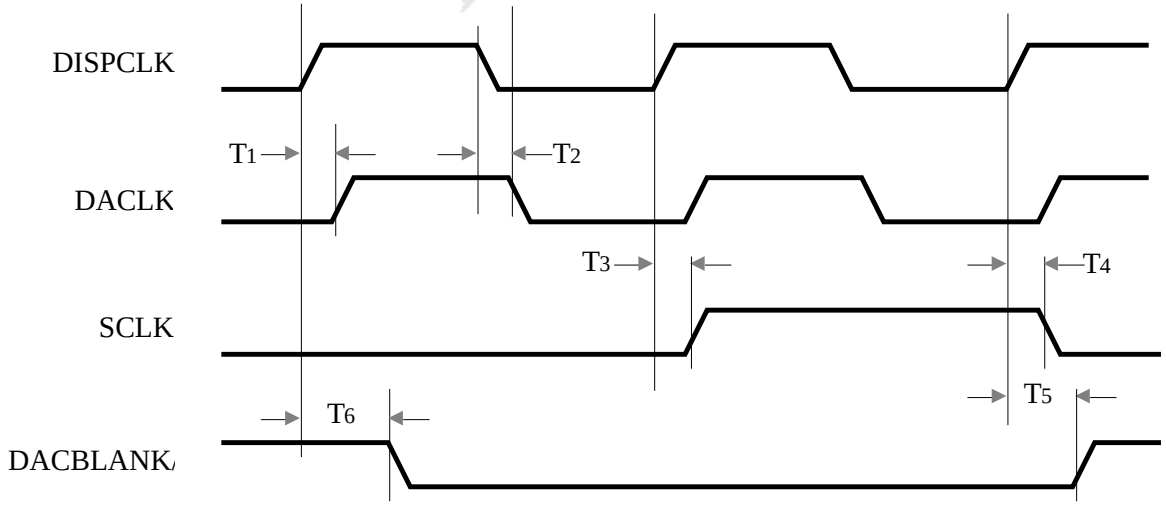
Symbol	Parameter	Notes	Min	Typ	Max	Units
T1	PCLK to KEYOUT Rising Delay		-	-	14	nS
T2	XCLKX2 to KEYOUT Falling Delay		-	-	18	nS



VGA Pixel Clock to KEYOUT (Analog Mux Control Timing)

AC TIMING CHARACTERISTICS - Display Clock to DAC Clock Timing

Symbol	Parameter	Notes	Min	Typ	Max	Units
T1	DISPCLK to DACLK Rising Delay		-	-	12	nS
T2	DISPCLK to DACLK Falling Delay		-	-	12	nS
T3	DISPCLK to SCLK Rising Delay		-	-	14	nS
T4	DISPCLK to SCLK Falling Delay		-	-	14	nS
T5	DISPCLK to DACBLANK/ Rising		-	-	25	nS
T6	DISPCLK to DACBLANK/ Falling		-	-	25	nS



Display Clock to DAC Clock, DAC Blank and VRAM Shift Clock Timing

AC TIMING CHARACTERISTICS - MEMORY CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_X	XCLKX2 (Note 1)	Note 1	–	T_P / 2	–	nS

Note 1: The 2 x Video Pixel Clock (XCLKX2) is used for memory timing. XCLKX2 is equal to twice the pixel input clock (XCLK). This clock is also used to generate timing for the random access port. DISPCLK is used to generate the Shift Clock (SCLK).

AC TIMING CHARACTERISTICS - VRAM ACCESS REQUIREMENTS

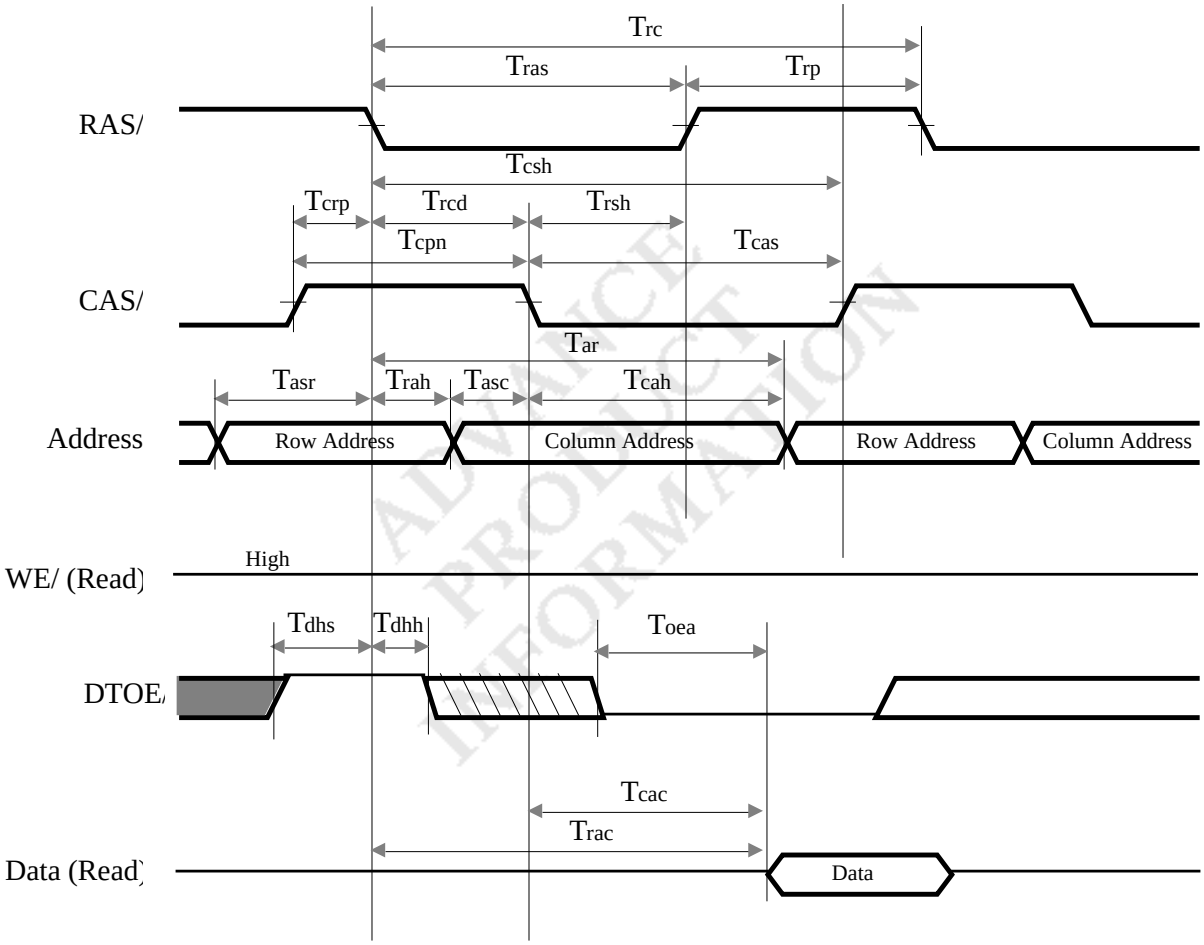
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RAC}	Data Access Time from RAS/		–	–	$4\ T_X$	nS
T_{CAC}	Data Access Time from CAS/		–	–	1_X	nS

AC TIMING CHARACTERISTICS - VRAM TIMING

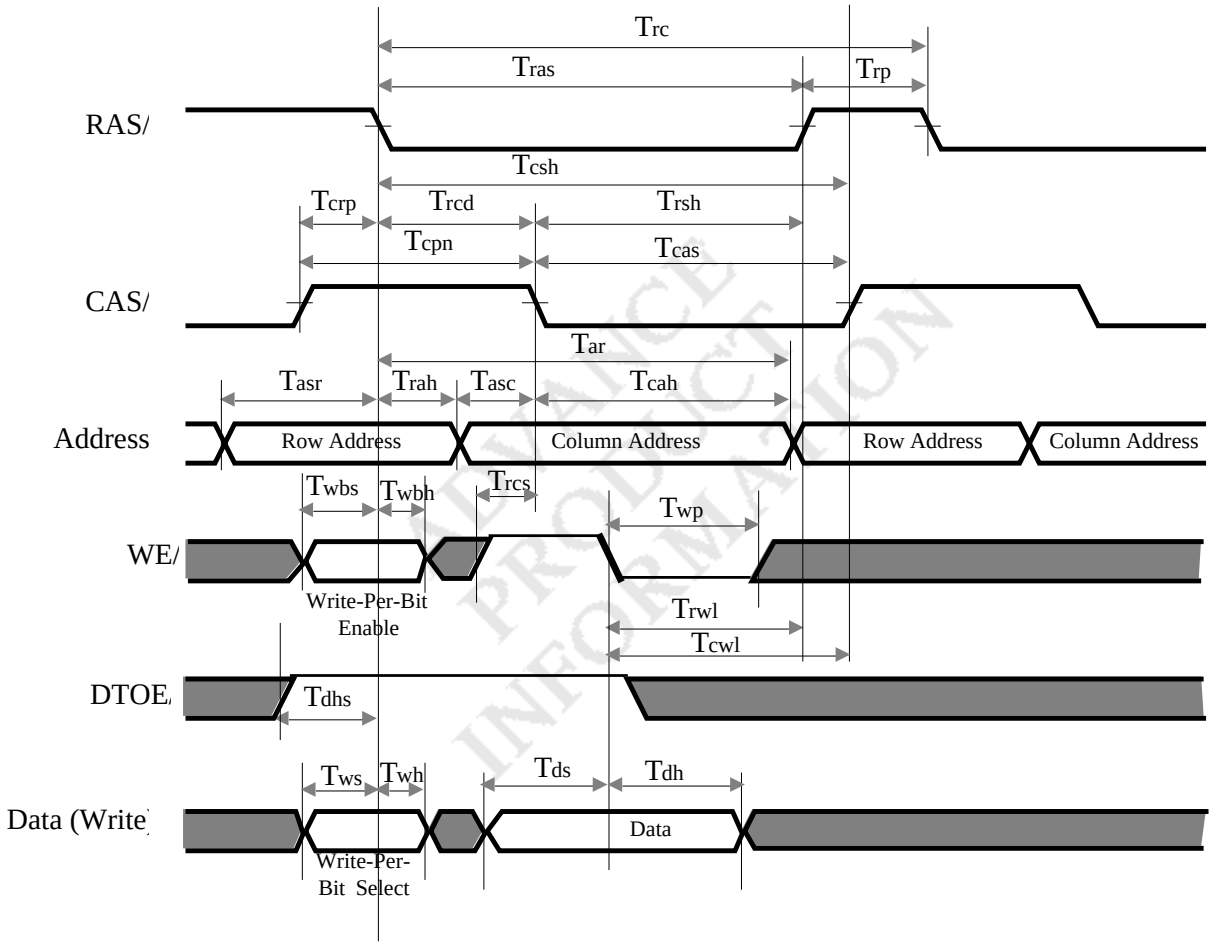
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RC}	Random read or write cycle time		$7T_X$	–	–	nS
T_{PC}	Fast-page cycle time		$4T_X$	–	–	nS
T_{RP}	RAS/ precharge		$3T_X$	–	–	nS
T_{RAS}	RAS/ pulse width		$4T_X$	–	–	nS
T_{RASP}	Fast-page RAS/ pulse width		$4T_X$	–	–	nS
T_{RSH}	RAS/ hold from CAS/		$2T_X$	–	–	nS
T_{CPN}	CAS/ precharge		$4T_X$	–	–	nS
T_{CP}	Fast-page CAS/ precharge time		$1T_X$	–	–	nS
T_{CAS}	CAS/ pulse width		$3T_X$	–	–	nS
T_{CAS1}	CAS/ pulse width (Fast Page Cycle)		$3T_X$	–	–	nS
T_{CAS2}	CAS/ pulse width (Fast Page Cycle)		$3T_X$	–	–	nS
T_{CSH}	CAS/ hold from RAS/		$5T_X$	–	–	nS
T_{RCD}	RAS/ to CAS/ delay		$1T_X$	–	–	nS
T_{CRP}	CAS/ high to RAS/ low precharge		$3T_X$	–	–	nS
T_{ASR}	Row Address setup time		$2T_X$	–	–	nS
T_{RAH}	Row Address hold time		$1T_X$	–	–	nS
T_{ASC}	Column Address setup to CAS/		$1T_X$	–	–	nS
T_{CAH}	Column Address hold time		$2T_X$	–	–	nS
T_{RAD}	RAS/ to Column Address delay time		$1T_X$	–	–	nS
T_{RAL}	Column Address to RAS/ lead time		$3T_X$	–	–	nS
T_{RCS}	Read command setup time		$5T_X$	–	–	nS
T_{WP1}	Write command pulse width(Fast Page Cycle)		$2T_X$	–	–	nS

AC TIMING CHARACTERISTICS - VRAM TIMING (Continued)

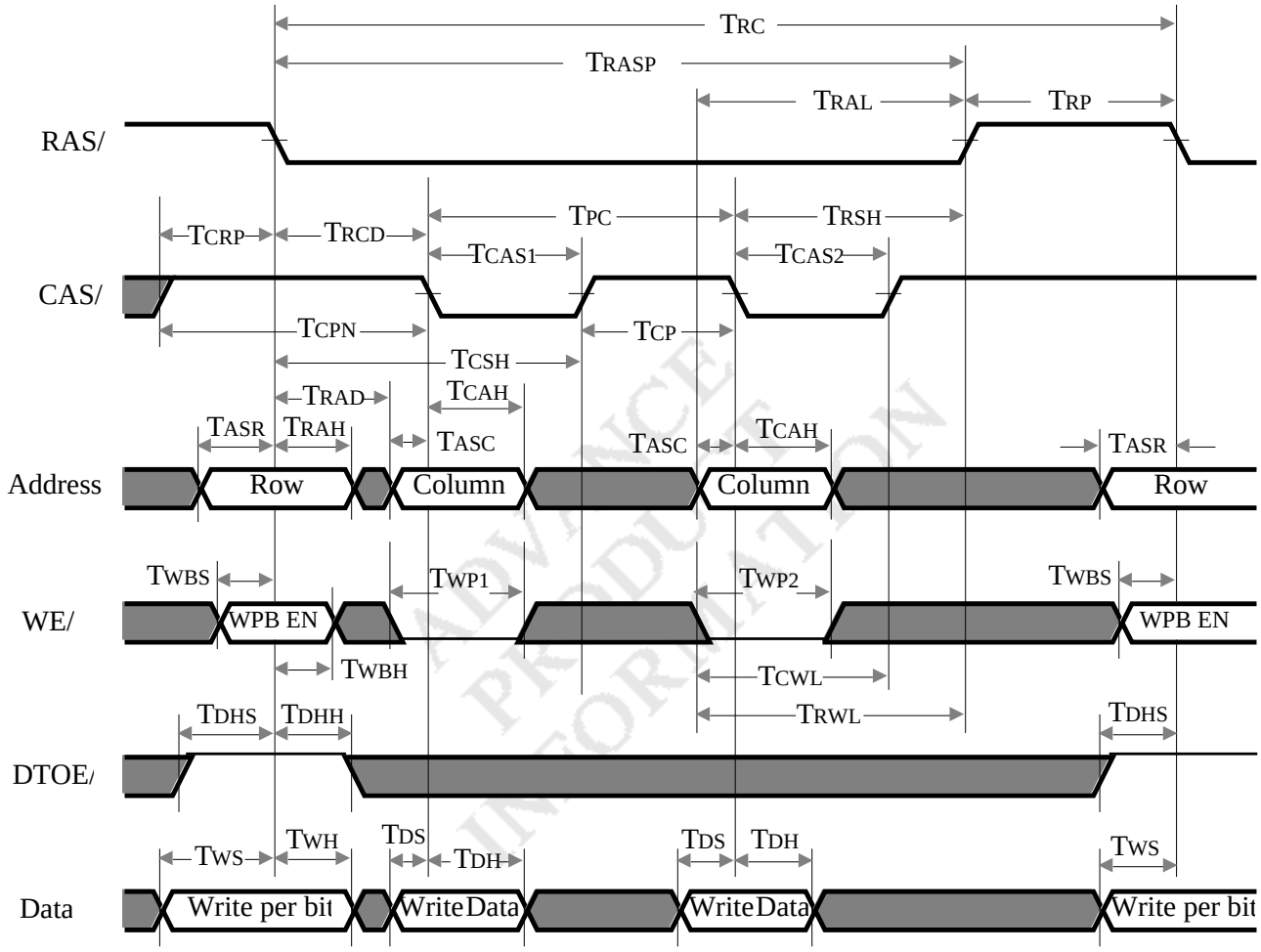
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{WP2}	Write command pulse width(Fast Page Cycle)		2 T_X	–	–	nS
T_{WP}	Write command pulse width		3 T_X	–	–	nS
T_{RWL}	Write command to RAS/ lead time		2 T_X	–	–	nS
T_{CWL}	Write command to CAS/ lead time		2 T_X	–	–	nS
T_{DS}	Data-in setup time		0.5 T_X	–	–	nS
T_{DH}	Data-in hold time		1_X	–	–	nS
T_{RPC}	RAS/ high to CAS/ low precharge time		$5T_X$	–	–	nS
T_{DLS}	DT/ low setup time		1 T_X	–	–	nS
T_{RDH}	DT/ low hold time after RAS/ low		3 T_X	–	–	nS
T_{CDH}	DT/ low hold time after CAS/ low		1_X	–	–	nS
T_{DHS}	DT/ high setup time		1_X	–	–	nS
T_{DHH}	DT/ high hold time		1_X	–	–	nS
T_{DTR}	DT/ high to RAS/ high delay		0_X	–	–	nS
T_{DTC}	DT/ high to CAS/ high delay		1 T_X	–	–	nS
T_{WBS}	Write-per-bit setup time		0.5 T_X	–	–	nS
T_{WBH}	Write-per-bit hold time		1_X	–	–	nS
T_{WS}	Write bit selection setup time		0.5 T_X	–	–	nS
T_{WH}	Write bit selection hold time		1_X	–	–	nS
T_{DTH}	DT/ high hold time after RAS/ high		2 T_X	–	–	nS



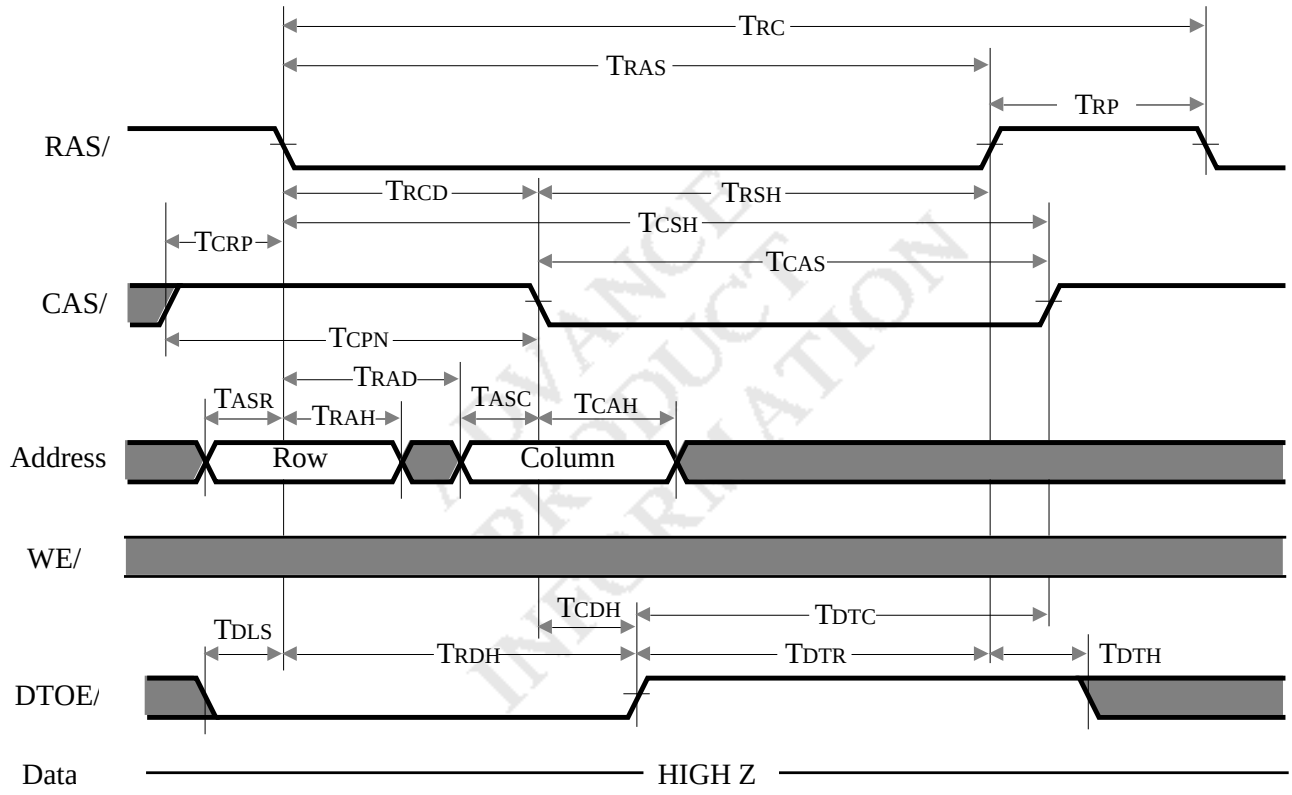
VRAM Random Read Cycle Timing



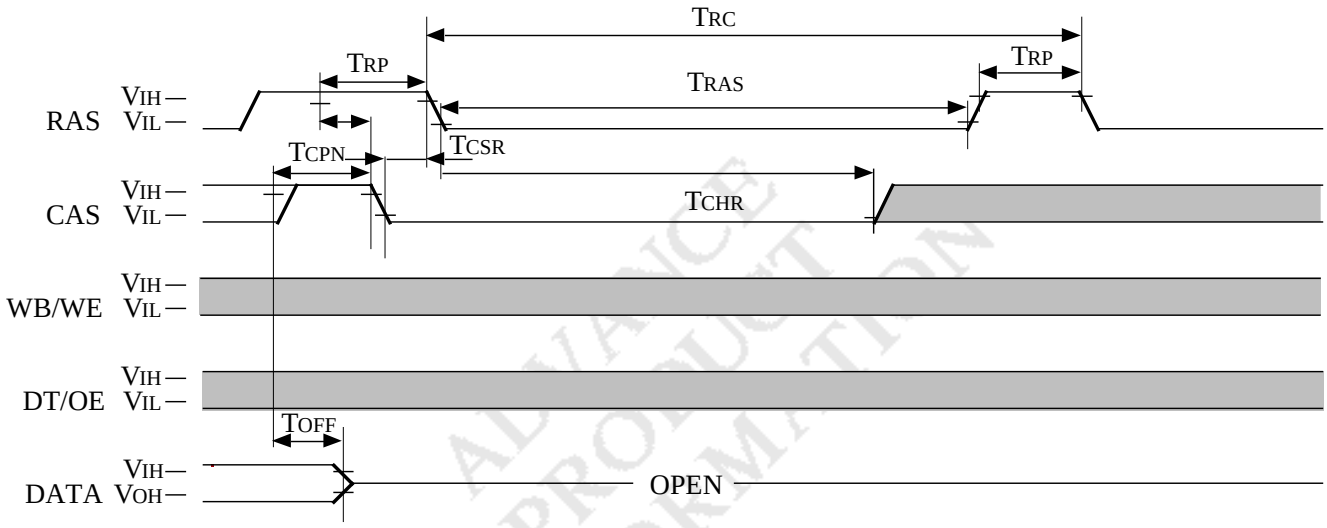
VRAM Random Write Cycle Timing



VRAM Fast-page Write Cycle Timing

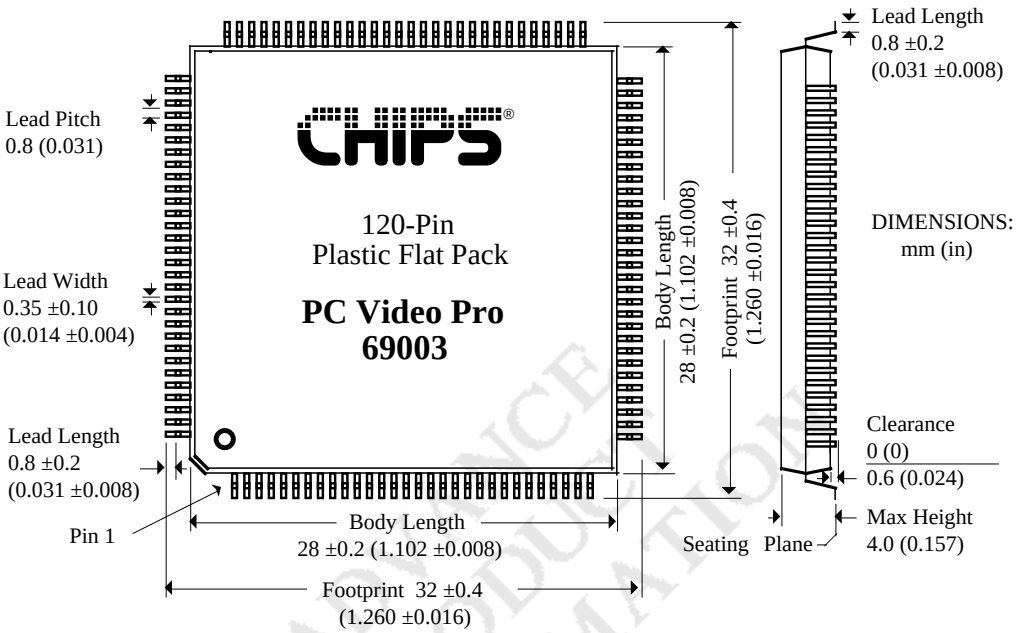


VRAM Data Transfer Cycle Timing

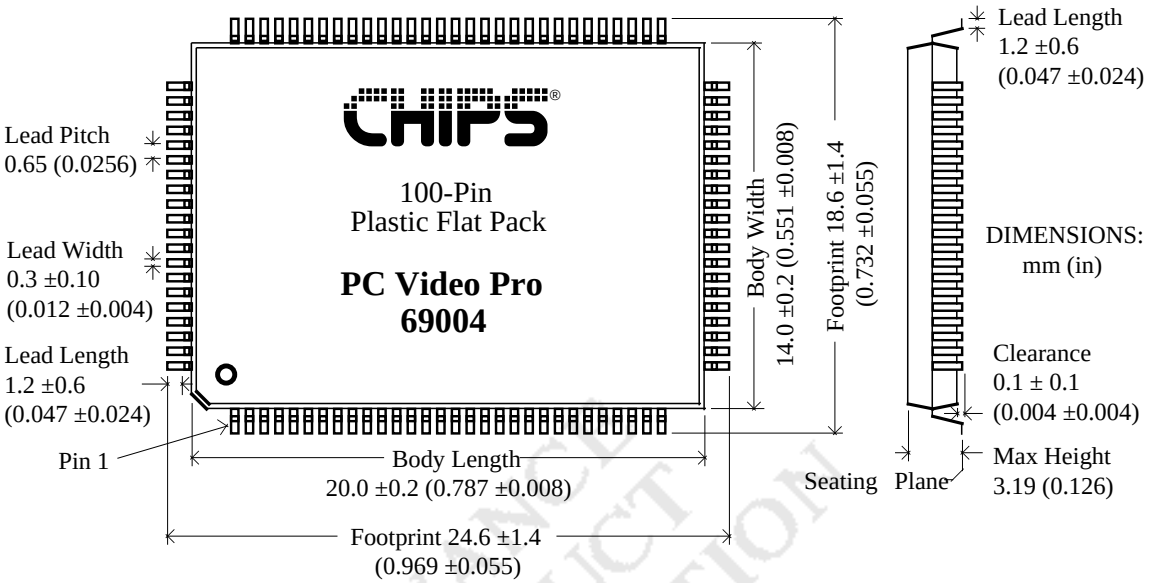


VRAM Refresh Cycle Timing

Mechanical Specifications



Mechanical Specifications



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