64201
(WinGlue)

High Performance
VGA Controller
Support Chip

Data Sheet

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P R E L I M I N A R Y

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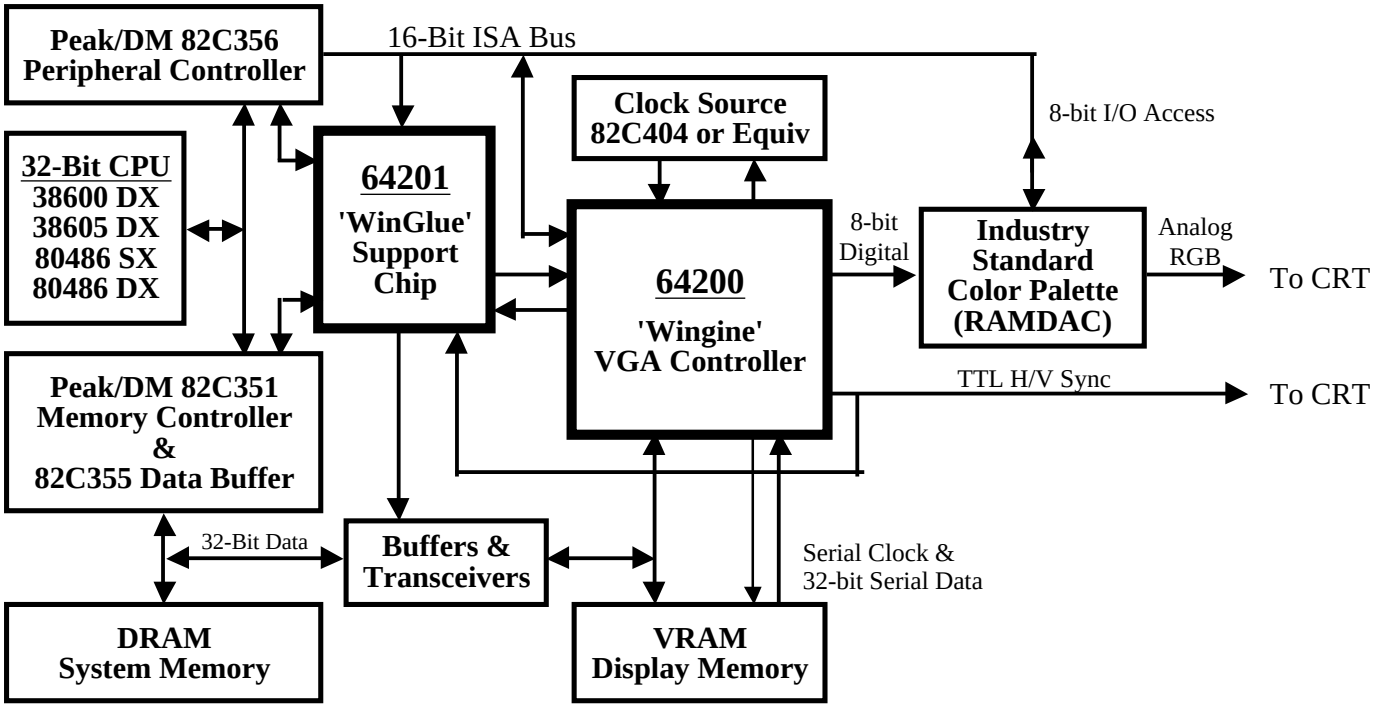
64201 (Winglue)
High Performance VGA Controller
Support Chip

- Provides interface logic for cost effective connection of the 64200 'Wingine™' Graphics Controller to PEAK/DM for high performance Windows™ operation in 386 and 486 systems
- Allows implementation of 1-bank (0.5 MB and 1MB) and 2-bank (2MB) display memory configurations
- Supports 16-bit (0.5 MB) display memory configuration in 32-bit systems
- Implements display memory using VRAMs for very high performance
- Supports split buffer transfers for support of 16bpp 800x600 mode in 1MB of display memory
- Supports interlaced or non-interlaced modes
- Small low-cost package: EIAJ-standard 68-pin PLCC



System Diagram

Revision History

Revision	Date	By	Comment
0.1	1/8/92	DH	Internal Review - Rough Draft and initial release
0.2	1/10/92	DH	Added Memory Connection Schematic Fixed pin list (added DTOE3/, changed drive on some pins, fixed typos)
0.3	9/14/92	VS	Added more details about Winglue operation

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Introduction

WINGINE WINDOWS ACCELERATOR

The 64200 Wingine Windows Accelerator is a 16-bit ISA-bus VGA with a backend 32-bit to 8-bit pixel serializer. This serializer allows display memory to be implemented with VRAMs for very high graphics performance, while still allowing use of a standard 8-bit RAMDAC for low cost. All VRAM shift-register support and backend pixel path logic is integrated into the Wingine chip.

The Wingine concept maps display memory VRAMs directly into the system CPU address space. The system memory controller is used to control VRAM access in 'Windows Acceleration' mode, while control of the VRAM array reverts to Wingine's internal VGA in 'VGA' mode for compatibility.

The Wingine VGA is designed to interface directly (i.e., with minimal external logic requirements) to CS4021 CHIPSet and future system logic chipsets from Chips & Technologies. The Wingine can also be interfaced to PEAK/DM chipset with the external 68-pin Winglue chip.

WINGLUE

The Winglue chip (64201) integrates all logic required for a PEAK/DM interface. The 64201 provides all the VRAM control functions which are not done by the PEAK/DM memory controller in a Wingine-based system. Winglue performs the following major functions:

1. Generate transfer cycles for screen refresh
2. Generate VRAM control signals
3. Arbitrate with the PEAK/DM memory controller to gain control of the memory bus during transfer cycles
4. Generate enable and direction signals for external buffers on the memory bus
5. Generate memory command strobes for VGA cycles
6. Disable video memory parity check

PEAK/DM

Peak/DM is a 386DX System Logic CHIPSet™ that can also be used with the 486SX or 486DX. The 82C351 Cache/Memory Controller includes page-interleaved memory operation that can accomodate a maximum of four 36-bit banks of DRAM. The four banks can be configured as a pair of banks operating page-interleaved with two additional banks operating in page mode but not page-interleaved. In a Wingine system, these two additional banks (normally numbered 2 and 3) can be populated with eight 256Kx4 VRAMs. Typically 1MB of VRAM will be included on the motherboard, allowing fast linear access for screen operations in a GUI environment such as Windows 3.x.

WINGLUE OPERATION

Winglue has two modes of operation based on the VGA input from Wingine.

VGA Mode: In this mode, Winglue tristates all the VRAM interface signals. Video memory is disconnected from the PEAK/DM memory controller. The 64200 Wingine chip controls video memory for screen updates and refreshes.

Wingine Mode: In this mode, display memory is accessed as part of system memory by PEAK/DM. Wingine tristates all of its memory interface signals. Winglue controls the external data and address buffers on the memory bus for video memory access. Winglue also performs transfer cycles into the VRAMs when requested by Wingine (when Wingine asserts XREQ/). Display timing and screen formats are determined by the HSYNC, VSYNC, and XREQ/ inputs.

Two types of VRAM operation occur in Wingine mode:

1. Video memory is accessed as part of system memory by the processor
2. Transfer cycles for display refresh are generated in response to XREQ/ from Wingine

Processor VRAM Access

Winglue generates enable and direction control signals for external buffers on the memory interface. There are two data tranceivers and two address buffers on the memory bus. One buffer is required for the memory control signals. In Wingine mode, Winglue asserts the VOE/ output to enable these external buffers allowing the PEAK/DM memory controller to access video memory directly. The 64201 also generates the MDINP/ signal for controlling the direction of the external data tranceivers.

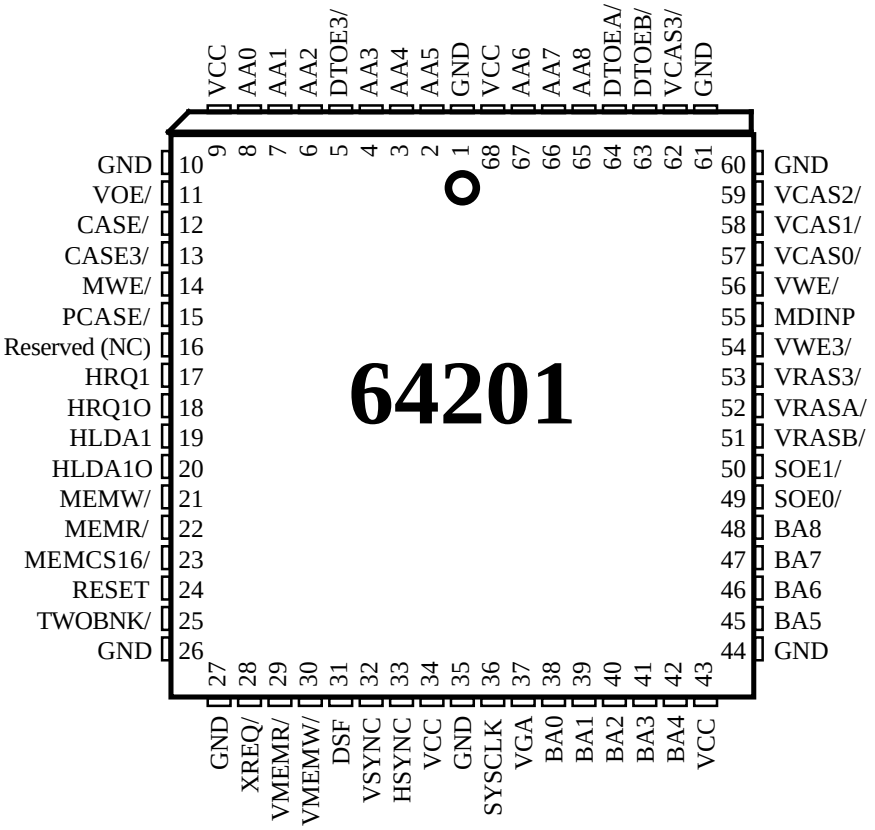
Display Transfer Cycles

Winglue performs transfer cycles to video memory by obtaining control of the memory bus from the PEAK/DM memory controller. The 64201 does all the necessary arbitration with PEAK/DM to gain control of the memory bus.

The Winglue transfer controller arbitrates in a similar manner to Bus Master and DMA devices. If both a Bus Master/DMA and Winglue attempt to acquire the local bus at the same time, they will be allowed to transfer concurrently.

Due to possible contention in display memory, a bus master/DMA cannot transfer data to/from display memory in Wingine mode. Bus master/DMA transfers to/from display memory are permitted in VGA mode.

Pinouts


64201
1 VCC
2 AA0
3 AA1
4 AA2
5 DTOE3/
6 AA3
7 AA4
8 AA5
9 GND
10 VCC
11 AA6
12 AA7
13 AA8
14 DTOEA/
15 DTOEB/
16 VCAS3/
17 GND
18 GND
19 VOE/
20 CASE/
21 CASE3/
22 MWE/
23 PCASE/
24 Reserved (NC)
25 HRQ1
26 HRQ1O
27 HLDA1
28 HLDA1O
29 MEMW/
30 MEMR/
31 MEMCS16/
32 RESET
33 TWOBNK/
34 GND
35 GND
36 XREQ/
37 VMEMR/
38 VMEMW/
39 DSF
40 VSYNC
41 HSYNC
42 VCC
43 GND
44 SYSCLK
45 VGA
46 BA0
47 BA1
48 BA2
49 BA3
50 BA4
51 VCC
52 GND
53 VCAS2/
54 VCAS1/
55 VCAS0/
56 VWE/
57 MDINP
58 VWE3/
59 VRAS3/
60 VRASA/
61 VRASB/
62 SOE1/
63 SOE0/
64 BA8
65 BA7
66 BA6
67 BA5
68 GND

Pin List

Pin Name	Pin #	Dir	Drive
AA0	8	I/O	4mA
AA1	7	I/O	4mA
AA2	6	I/O	4mA
AA3	4	I/O	4mA
AA4	3	I/O	4mA
AA5	2	I/O	4mA
AA6	67	I/O	4mA
AA7	66	I/O	4mA
AA8	65	I/O	4mA
BA0	38	Out	4mA
BA1	39	Out	4mA
BA2	40	Out	4mA
BA3	41	Out	4mA
BA4	42	Out	4mA
BA5	45	Out	4mA
BA6	46	Out	4mA
BA7	47	Out	4mA
BA8	48	Out	4mA
CASE/	12	In	--
CASE3/	13	In	--
DSF	31	Out	8mA
DTOEA/	64	Out	4mA
DTOEB/	63	Out	4mA
DTOE3/	5	Out	8mA
GND	1	--	--
GND	10	--	--
GND	26	--	--
GND	27	--	--
GND	35	--	--
GND	44	--	--
GND	60	--	--
GND	61	--	--
HLDA1	19	In	--
HLDA1O	20	Out	4mA
HRQ1	17	In	--
HRQ1O	18	Out	4mA
HSYNC	33	In	--
MEMCS16/	23	In	--

Pin Name	Pin #	Dir	Drive
MDINP	55	Out	4mA
MEMR/	22	In	--
MEMW/	21	In	--
MWE/	14	In	--
PCASE/	15	Out	4mA
RESET	24	In	--
SOE0/	49	Out	8mA
SOE1/	50	Out	8mA
SYSCLK	36	In	--
TWOBNK/	25	In	--
VCAS0/	57	Out	4mA
VCAS1/	58	Out	4mA
VCAS2/	59	Out	4mA
VCAS3/	62	Out	4mA
VCC	9	--	--
VCC	34	--	--
VCC	43	--	--
VCC	68	--	--
VGA	37	In	--
VMEMR/	29	Out	4mA
VMEMW/	30	Out	4mA
VOE/	11	Out	8mA
VRASA/	52	I/O	4mA
VRASB/	51	Out	4mA
VRAS3/	53	I/O	8mA
VSYNC	32	In	--
VWE/	56	Out	8mA
VWE3/	54	Out	8mA
XREQ/	28	In	--
Reserved (NC)	16	--	--

PIN DESCRIPTIONS

System Interface

Pin #	Pin Name	Type	Active	Description
36	SYSCLK	In	High	System clock. Used to synchronize internal operations and drive internal state machines. Can be asynchronous to VGA clocks or processor SYSCLK or CLK2. Should be the highest frequency available ≤40MHz (and ≥16MHz).
24	RESET	In	High	ISA bus reset. Used to initialize internal state.
25	TWOBNK/	In	Low	Two bank mode (static configuration input)
17	HRQ1	In	High	Hold request in (from PEAK/DM 82C356 pin 142)
18	HRQ1O	Out	High	Hold request out (to PEAK/DM 82C351 pin 74)
19	HLDA1	In	High	Hold acknowledge in (from PEAK/DM 82C351 pin 76)
20	HLDA1O	Out	High	Hold acknowledge out (to PEAK/DM 82C356 pin 66)
21	MEMW/	In	Low	ISA bus memory write strobe (from 82C356 pin 5)
22	MEMR/	In	Low	ISA bus memory read strobe (from 82C356 pin 6)
23	MEMCS16/	In	Low	Memory Select 16 from VGA address decode logic. Should be asserted when LA23-17 = 0000101 (binary), i.e., address space 0Axxxx and 0Bxxxx.
12	CASE/	In	Low	System memory column address strobe enable for first bank of VRAMs. Driven by the 82C351 RAS5/ output (pin 133).
13	CASE3/	In	Low	System memory column address strobe enable for second bank of VRAMs. Driven by the 82C351 RAS7/ output (pin 135).
14	MWE/	In	Low	System memory write enable. Driven by the 82C351 DWE/ output (pin 101), typically buffered since this same pin also drives multiple system memory inputs.
15	PCASE/	Out	Low	Parity CAS Enable. Used with one 74F32 package to gate CAS0-3/ from the 82C351 CPU/Cache/DRAM Controller pins 116-119 to the 82C355 Data Buffer pins 69-72. Used to disable parity checking for display memory VRAM array.

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS **Graphics Controller Interface**

Pin #	Pin Name	Type	Active	Description
29	VMEMR/	Out	Low	VGA memory read strobe (to 64200 pin 25)
30	VMEMW/	Out	Low	VGA memory write strobe (to 64200 pin 26)
37	VGA	In	High	Display mode input from 64200 pin 97. Controlled by 64200 Master Control register bit-0 (inverted). Active in VGA mode, inactive in Wingine mode.
28	XREQ/	In	Low	Transfer request from 64200 pin 74 (used to initiate VRAM data transfer cycles)
33	HSYNC	In	High	Horizontal sync input from 64200 pin 75 (used for odd/even field and interlace detection)
32	VSYNC	In	High	Vertical sync input from 64200 pin 76 (used for odd/even field and interlace detection and to reset the transfer address counter)

Note: HSYNC and VSYNC polarities are programmable via the VGA MSR (Miscellaneous Output Register) bits 6 and 7. In VGA 400-line modes (31.5KHz / 70 Hz monitor timing, typically used for VGA text modes), HSYNC is programmed to negative polarity. In VGA 480-line modes (31.5 KHz / 60 Hz monitor timing for 640x480 graphics modes), both sync signals become negitive polarity. Typically, VGA 800x600 modes also use negative polarity sync signals, but typical multisync monitors will work with either polarity. All high resolution modes (1024x768 and higher, interlace and non-interlace) use positive polarity syncs. The 64201 asssumes positive polarity sync signals in 'Wingine' mode (it ignores the sync signals in VGA modes).

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Power and Ground

Pin #	Pin Name	Type	Active	Description
9	VCC	In	n/a	+5V
34	VCC	In	n/a	
43	VCC	In	n/a	
68	VCC	In	n/a	
1	GND	In	n/a	Ground
10	GND	In	n/a	
26	GND	In	n/a	
27	GND	In	n/a	
35	GND	In	n/a	
44	GND	In	n/a	
60	GND	In	n/a	
61	GND	In	n/a	
16	Reserved (NC)	--	--	Reserved (do not connect)

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Display Memory Interface

Pin #	Pin Name		Type	Active	Description
8	AA0	(TST0)	I/O	High	Address bus for VRAM bytes 0 & 2 (also called VRAMs 'A' and 'C' in the application schematics). These pins are also used as test inputs. Note: Byte 0 (bits 0-7) = VRAM 'A' Byte 1 (bits 8-15) = VRAM 'B' Byte 2 (bits 16-23) = VRAM 'C' Byte 3 (bits 24-31) = VRAM 'D'
7	AA1	(TST1)	I/O	High	
6	AA2	(TST2)	I/O	High	
4	AA3	(TST3)	I/O	High	
3	AA4	(TST4)	I/O	High	
2	AA5	(TST5)	I/O	High	
67	AA6	(TST6)	I/O	High	
66	AA7	(TST7)	I/O	High	
65	AA8	(TST8)	I/O	High	
38	BA0		Out	High	Address bus for VRAM bytes 1 & 3 (also called VRAMs 'B' and 'D' in the application schematics) Note: VGA planes 0-1 are implemented in VRAM C and VGA planes 2-3 are implemented in VRAM D in 32-bit system configurations. VRAMs A and B are only accessible to the system in 32-bit 'Wingine' mode.
39	BA1		Out	High	
40	BA2		Out	High	
41	BA3		Out	High	
42	BA4		Out	High	
45	BA5		Out	High	
46	BA6		Out	High	
47	BA7		Out	High	
48	BA8		Out	High	
52	VRASA/		Out	Low	Row address strobe for VRAM bank 0 bytes 0 & 2
51	VRASB/		Out	Low	Row address strobe for VRAM bank 0 bytes 1 & 3
53	VRAS3/		Out	Low	Row address strobe for VRAM bank 1
57	VCAS0/		Out	Low	Column address strobe for VRAM byte 0 (VRAM A)
58	VCAS1/		Out	Low	Column address strobe for VRAM byte 1 (VRAM B)
59	VCAS2/		Out	Low	Column address strobe for VRAM byte 2 (VRAM C)
62	VCAS3/		Out	Low	Column address strobe for VRAM byte 3 (VRAM D)
56	VWE/		Out	Low	Write enable for VRAM bank 0 all bytes
54	VWE3/		Out	Low	Write enable for VRAM bank 1 all bytes
64	DTOEA/		Out	Low	Data transfer / output enable for bank 0 bytes 0 & 2
63	DTOEB/		Out	Low	Data transfer / output enable for bank 0 bytes 1 & 3
5	DTOE3/		Out	Low	Data transfer / output enable for VRAM bank 1
31	DSF		Out	High	VRAM Special Function (split-buffer transfer control)
49	SOE0/		Out	Low	Serial output enable for VRAM bank 0
50	SOE1/		Out	Low	Serial output enable for VRAM bank 1
11	VOE/		Out	Low	VRAM Output Enable. Deasserted in VGA mode or during data transfer cycles. Asserted in Wingine mode to allow the CPU to access the VRAMs as part of system memory. Connect this pin to the output enables of the 74F244/245 data/address/control signal isolation buffers (located between the VRAMs and the system to allow the 64200 to acccess the VRAMs in VGA mode).
55	MDINP		Out	High	VRAM Data Direction. High for memory reads, low for memory writes. Connect this pin to the direction control inputs of the 74F245 data isolation buffers.