PowerPC™

IBM

PowerPC EM603e and 603e

Microprocessors optimized for embedded applications

Highlights

PowerPC EM603e[*] and 603e family processors are 32-bit implementations of the PowerPC Reduced Instruction Set Computer (RISC) microprocessor family. They offer high clock frequency and efficient throughput driven by five execution units and the ability to issue and retire two instructions per clock. Although all models provide industry-leading value because of a low-cost manufacturing process, EM603e models can provide even greater value in applications which do not need floating-point functionality.

All PowerPC EM603e and 603e processors are price-positioned and functionally optimized for the high-end embedded market, making them ideal for networking and communications applications.

Summary of Features:

Power Management Unit
- Low-power design
- Dynamic power management
- Doze, nap, and sleep power savings modes
- 3.3V or 2.5V core power supply available

Instruction Fetching & Branch Unit
- 6-instruction prefetch queue
- Static branch prediction

Dispatch Unit
- Dispatches 2 instructions per cycle
- 4-stage pipeline: Fetch, Dispatch, Execute, and Complete

Load/Store Unit
- One cycle cache access
- Executes cache and TLB instructions
- Alignment and number denormalization
- Hit under reload instruction

Fixed-Point Execution Unit
- One cycle add, subtract, shift, or rotate
- Hardware multiply and divide
- Thirty-two, 32-bit General Purpose Registers

Floating-Point Execution Unit (PowerPC 603e only)
- Optimized for single-precision multiply/add
- IEEE-754 standard single-and double-precision floating point arithmetic
- Thirty-two, 64-bit Floating Point Registers

System Unit
- Executes condition register logical, special register transfer, and other system instructions
- Executes integer add/compare instructions

Memory Management Unit
- 52-bit virtual and 32-bit real addressing
- 8 Block Address Translation registers
- 64-entry, 2-way data and instruction TLB
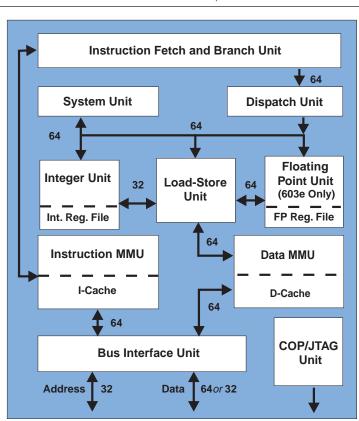- Fast-trap mechanism for software reload TLB

Cache Unit
- 16K, 4-way set associative instruction cache
- 16K, 4-way set associative data cache
- 3-state hardware coherency (MEI); compatible with four-state MESI protocol
- Physically tagged and addressed
- Copy-back data cache
- Hardware support for data coherency
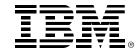
Bus Interface Unit
- General purpose interface for a wide range of system configurations
- 32-bit address and selectable 64- or 32-bit data bus
- Powerful diagnostic and test interface through the Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface
- Parity checking on bus
- Fast reset due to Level Sensitive Scan Design (LSSD)
- Bi-Endian operation

PowerPC EM603e and 603e Specifications

Processor Speed		100, 166 and 200 MHz
Technology	100 MHz	0.5μm/0.46μm L_{eff}, CMOS, 4 levels metal
	166 MHz	0.35μm/0.25μm L_{eff}, CMOS, 5 levels metal
	200 MHz	0.35μm/0.18μm L_{eff}, CMOS, 5 levels metal
Die Size	100 MHz	8.4 mm x 11.67 mm (98 mm^2)
	166/200 MHz	7.5 mm x 10.5 mm (79 mm^2)
Performance (est.)	100 MHz (603e)	120 SPECint92, 105 SPECfp92
	100 MHz (EM603e)	120 SPECint92, or 135 Dhrystone 2.1 MIPS
	166 MHz (603e)	4.1 SPECint95, 3.0 SPECfp95
	166 MHz (EM603e)	4.1 SPECint95, or 225 Dhrystone 2.1 MIPS
	200 MHz (603e)	5.1 SPECint95, 3.7 SPECfp95
	200 MHz (EM603e)	5.1 SPECint95, or 271 Dhrystone 2.1 MIPS
CPU Bus Ratio	100 MHz	1x, 1.5x, 2x, 2.5x, 3x, 3.5x, 4x
	166/200 MHz	2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x
Signal I/Os		165
Power Supply	100 MHz	3.3V +/- 5% I/O, 3.3V +/- 5% Core
	166/200 MHz	3.3V +/- 5% I/O, 2.5V +/- 5% Core
Power Dissipation (est.)	100 MHz	3.2W Typical
	166 MHz	3.0W Typical
	200 MHz	4.0W Typical
Temperature Range		0°C to 105°C
Packaging	100/166/200 MHz	255-pin CBGA
	100 MHz	240-pin PQFP

PowerPC EM603e and 603e Block Diagram

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