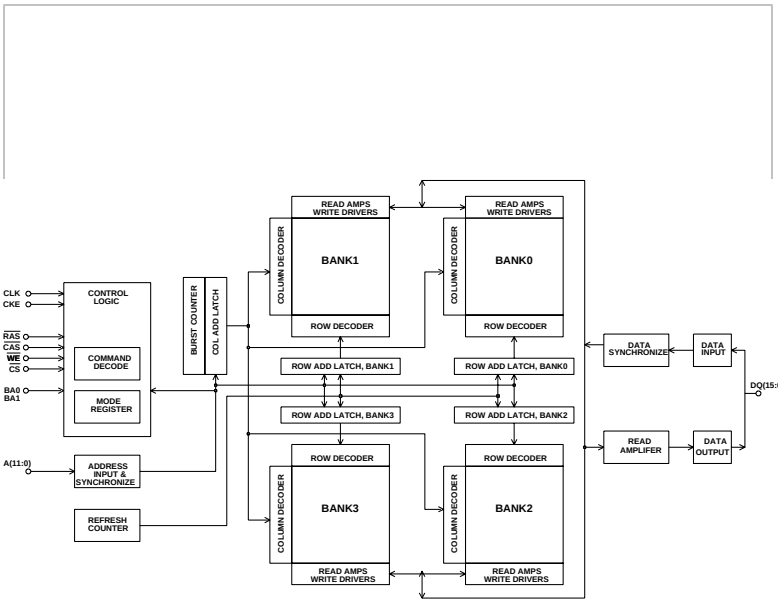
Features

- PC100 Compliant
- 3 Design Variations for Different I/O width
  - 4Bank x 4195024 x 4 bit
  - 4 Bank x 2097512 x 8 bit
  - 4 Bank x 1048576 x 16 bit
- LVTTL Input/Output Interface
- 3.3V Power Supply +/- 0.3V
- 66MHz/100MHz
- t_{AC}=6ns for CAS Latency=2,3
- Programmable Mode Register
  - CAS Latency (1,2,3)
  - Burst Length (1,2,4,8,Full Page)
  - Burst Type (Sequential, Interleaved)
- Refresh: 4096 cycle/64ms
- Burst Stop Functionality
- Auto-refresh, Self-refresh Capability
- Clock Suspend, Power Down Functionality
- Read and Write Mask Functionality
  - Write DQM Latency=0
  - Read DQM Latency=CAS Latency
- Pkg: 54 pin 400mil Plastic TSOP



Functional Block Diagram

General Description

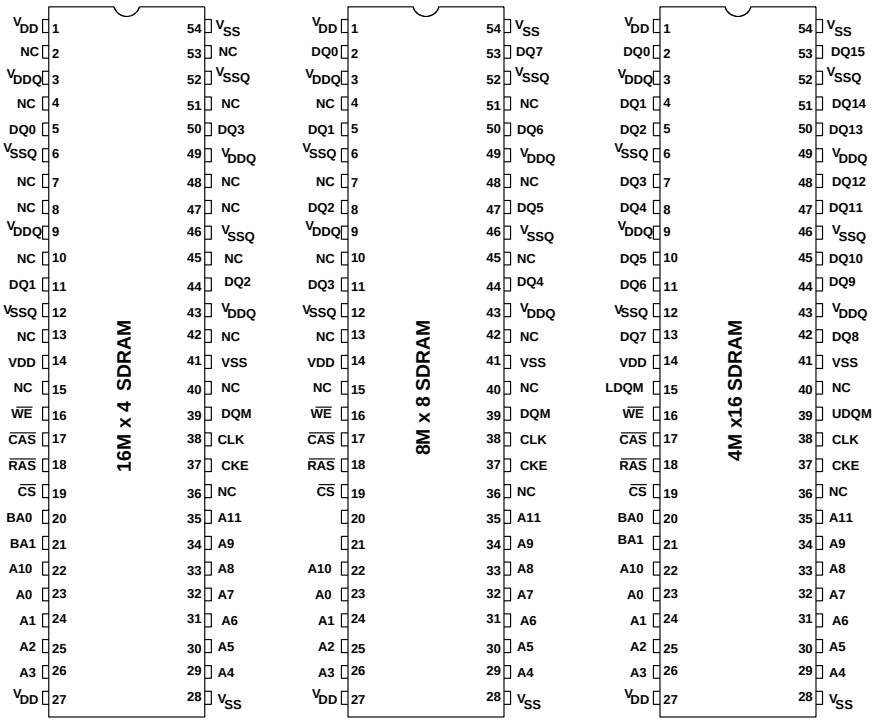
The 64MPC100SDRAM Synchronous DRAM is organized as four 16M banks. This part is designed with metal mask options for selecting the I/O word width. Options exist for a x4, x8 or x16 implementation.

The MOSAID 64M SDRAM conforms to JEDEC standards and Intel PC100 specifications. A mode register is included to allow the burst length, burst type and CAS latency to be programmed. The instructions do not have to follow the 2N-rule. Multi bank operation is supported. Power down and self-refresh modes are available. Burst stop functionality is supported for both read and write cycles.

A 3.3V external power supply is used in the periphery circuits. An internal voltage is available for the cells and sense amplifier circuitry. A VPP generator is also included to generate the above VDD voltage used for wordline access.

Test modes such as redundancy roll call and auto-refresh counter test are available.

Pin Configuration Diagram



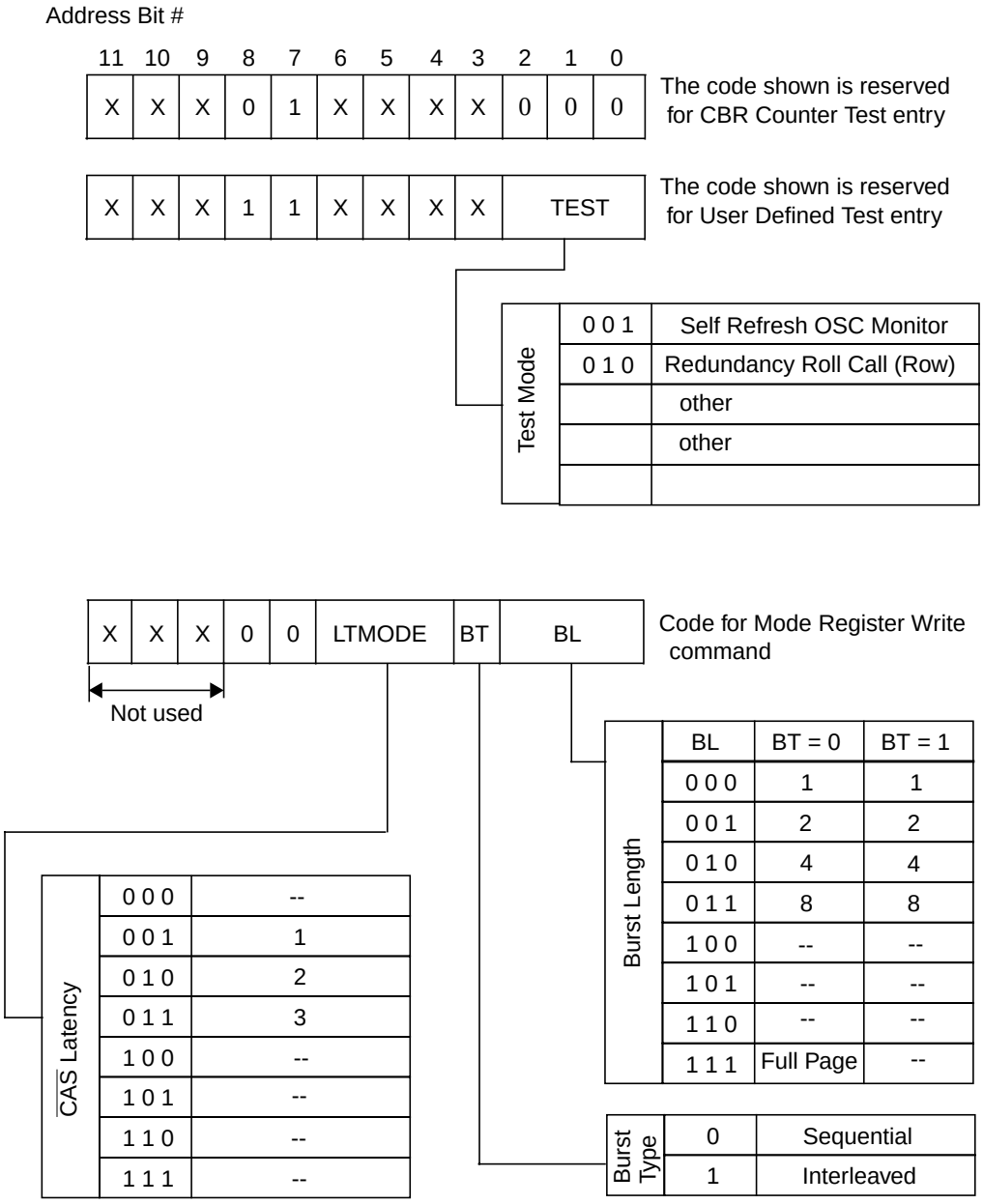
Pin Description Table

Pin Name	Type/Description
BA0,BA1	Bank Select Address Input
A0- A11	Address Inputs. A10 is the autoprecharge flag during column cycles, and the precharge all banks flag during precharge commands.
CLK	Clock Input
CKE	Clock Enable Input. Enables the clock internally when high. CKE low initiates power down, self-refresh or clock suspend modes.
$\overline{RAS}$	Row address Strobe. Used to decode command.
$\overline{CAS}$	Column Address Strobe. Used to decode command.
$\overline{WE}$	Write Enable. Used to decode command.
$\overline{CS}$	Chip Select. Enables the command decode.
DQM, LDQM, UDQM	Data Mask. High to mask the input data or disable the output drive.
DQ(N:0)	Data Input/Output
NC	No Connect
V_{DD},V_{SS}	Power and Ground Supplies
V_{DDQ},V_{SSQ}	Dedicated Power and Ground for the output drivers

Functional Description

Mode Register Programming

The mode register is used to program the desired mode of operation. The burst length, burst type and CAS latency are programmed here.This register must be initialized after power up since its contents are undefined after power up. The format of the register is shown below.



Command Truth Table

Command	CKE	DQM	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A10	A0-9	Function
DESL	H	X	H	X	X	X	X	X	X	DESeLect
NOP	H	X	L	H	H	X	X	X	X	No Operation
RD	H	X	L	H	L	H	V	L	V	Column Address & Read
RDA	H	X	L	H	L	H	V	H	V	Read with Auto precharge
WR	H	X	L	H	L	L	V	L	V	Column address & Write
WRA	H	X	L	H	L	L	V	H	V	Write with Auto Precharge
ACTV	H	X	L	L	H	H	V	V	V	Row Address and bank ActiVate
PRE	H	X	L	L	H	L	V	L	X	Precharge select bank
PALL	H	X	L	L	H	L	X	H	X	Precharge ALL banks
BST	H	X	L	H	H	L	X	X	X	Burst STop
REFR	H	X	L	L	L	H	X	X	X	Auto Refresh
MRS	H	X	L	L	L	L	L	L	V	Mode Register Set
SELF	L	X	L	L	L	H	X	X	X	Self Refresh entry
MASK	H	H	X	X	X	X	X	X	X	Data MASK/ Output Disable

SDRAM Functional Truth Table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	An	Command	Action
IDLE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA (1)	RD/RDA	ILLEGAL (3)
	L	H	L	L	BA, CA (1)	WR/WRA	ILLEGAL (3)
	L	L	H	H	BA, RA (1)	ACTV	Row Activating; Latch Row Address
	L	L	H	L	BA, AP	PRE/PALL	NOP (5)
	L	L	L	H	X	REFR/SELF	Auto Refresh(6)
	L	L	L	L	Op-code	MRS/MRR	Mode Register Access (6)
Row Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, AP	RD/RDA	READ; Latch CA; Determine AP
	L	H	L	L	BA, CA, AP	WR/WRA	WRITE; Latch CA; Determine AP
	L	L	H	H	BA, RA	ACTV	NOP(10)
	L	L	H	L	BA, AP	PRE/PALL	Precharge
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	ILLEGAL
READ	H	X	X	X	X	DESL	NOP (Continue burst to end; => Row Active)
	L	H	H	H	X	NOP	NOP (Continue burst to end; => Row Active)
	L	H	H	L	X	BST	Burst Stop
	L	H	L	H	BA, CA, AP	RD/RDA	Term Burst, New READ, Determine AP (4)
	L	H	L	L	BA, CA, AP	WR/WRA	Term Burst, New WRITE, Determine AP (4)
	L	L	H	H	BA, RA	ACTV	NOP(10)
	L	L	H	L	BA, AP	PRE/PALL	Term Burst, Precharge (4)
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	ILLEGAL
WRITE	H	X	X	X	X	DESL	NOP (Continue burst to end; => Row Active)
	L	H	H	H	X	NOP	NOP (Continue burst to end; => Row Active)
	L	H	H	L	X	BST	Burst Stop
	L	H	L	H	BA, CA, AP	RD/RDA	Term Burst, New READ, Determine AP (3)
	L	H	L	L	BA, CA, AP	WR/RA	Term Burst, New WRITE, Determine AP (3)
	L	L	H	H	BA, RA	ACTV	NOP(10)
	L	L	H	L	BA, AP	PRE/PALL	Term Burst, Precharge (4)
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	LLEGAL
READ with Auto Precharge (READA)	H	X	X	X	X	DESL	NOP (Continue burst to end; => Precharge)
	L	H	H	H	X	NOP	NOP (Continue burst to end; => Precharge)
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	RD/RDA	ILLEGAL (3)
	L	H	L	L	BA, CA, AP	WR/WRA	ILLEGAL (3)
	L	L	H	H	BA, RA	ACTV	NOP(10)
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL (3)
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	ILLEGAL
WRITE with Auto Precharge (WRITA)	H	X	X	X	X	DESL	NOP (Continue burst to end; => Precharge)
	L	H	H	H	X	NOP	NOP (Continue burst to end; => Precharge)
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	RD/RDA	ILLEGAL (3)
	L	H	L	L	BA, CA, AP	WR/WRA	ILLEGAL (3)
	L	L	H	H	BA, CA	ACTV	NOP(10)
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL (3)
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	An	Command	Action
Precharge	H	X	X	X	X	DESL	NOP => IDLE after t_{RP}
	L	H	H	H	X	NOP	NOP => IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, AP	RD/RDA	ILLEGAL (3)
	L	H	L	L	BA, CA, AP	WR/WRA	ILLEGAL (3)
	L	L	H	H	BA, RA	ACTV	NOP(10)
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL (3)
	L	L	L	H	X	REFR/SELF	ILLEGA
	L	L	L	L	X	MR/ MRR	ILLEGA
ROW Activating	H	X	X	X	X	DESL	NOP => Row Active after t_{RCD}
	L	H	H	H	X	NOP	NOP => Row Active after t_{RCD}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, AP	RD/RDA	ILLEGAL (3)
	L	H	L	L	BA, CA, AP	WR/WRA	ILLEGAL (3)
	L	L	H	H	BA, RA	ACTV	NOP(10)
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL (3)
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	ILLEGAL
WRITE Recover	H	X	X	X	X	DESL	NOP => Row Active after t_{WR}
	L	H	H	H	X	NOP	NOP => Row Active after t_{WR}
	L	H	H	L	X	BST	Burst Stop
	L	H	L	H	BA, CA, AP	RD/RDA	ILLEGAL (3)
	L	H	L	L	BA, CA, AP	WR/WRA	ILLEGAL (3)
	L	L	H	H	BA, RA	ACTV	NOP(10)
	L	L	H	L	BA, AP	PRE/PALL	Precharge
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	ILLEGAL
WRITA Recover	H	X	X	X	X	DESL	NOP => Precharge after t_{WR}
	L	H	H	H	X	NOP	NOP => Precharge after t_{WR}
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	RD/RDA	ILLEGAL (3)
	L	H	L	L	BA, CA, AP	WR/WRA	ILLEGAL (3)
	L	L	H	H	BA, RA	ACTV	NOP(10)
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	ILLEGAL
Auto Refresh	H	X	X	X	X	DESL	NOP => IDLE after t_{RC}
	L	H	H	H	X	NOP	NOP => IDLE after t_{RC}
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	X	X	RD/WR	ILLEGAL
	L	L	H	X	X	ACTV/PRE/PALL	ILLEGAL
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	ILLEGAL
Mode Register Access	H	X	X	X	X	DESL	NOP => IDLE after 4 clocks
	L	H	H	H	X	NOP	NOP => IDLE after 4 clocks
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	X	X	RD/WR	ILLEGAL
	L	L	H	X	X	ACTV/PRE/PALL	ILLEGAL
	L	L	L	H	X	REFR/SELF	ILLEGAL
	L	L	L	L	X	MRS/MRR	ILLEGAL

Current State	CKE_{n-1}	CKE_n	CS	RAS	CAS	$\overline{WE}$	An	Action
Self Refresh (7)	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh => ABI (1)
	L	H	L	H	H	H	X	Exit Self Refresh => ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
Power Down	H	H	H	X	X	X	X	INVALID
	L	H	L	H	H	H	X	Exit Power Down => ABI (1)
	L	H	H	X	X	X	X	Exit Power Down => ABI (1)
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	H	H	X	ILLEGAL
	L	H	L	L	H	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Power Down)
All Banks Idle (8)	H	H	X	X	X	X	X	Refer to Table 3
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	LLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to operation Table 3
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle (9)
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle (9)
	L	L	X	X	X	X	X	Maintain Clock Suspend

Notes:

1. Abbreviations:
   RA = Row Address; BA = Bank Address; Term = Terminate; ABI = All Banks Idle
   CA = Column Address; AP = Auto Precharge; NOP = No Operation
2. All entries assume that CKE was active (HIGH) during the preceding clock cycle and the current cycle.
3. Illegal to bank in state specified in Current State column; function may be legal in the bank indicated by BA, depending on the state of the bank.
4. Must satisfy the 2N rule, bus contention, bus turn around, and/or write recovery requirements.
5. NOP to bank precharging or idle state. May precharge bank(s) indicated by BA (and A10).
6. Illegal if any bank is not idle.
   ILLEGAL = Device operation and/or data-integrity is not guaranteed.
7. CKE Low-to-High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
8. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
9. Must be legal command.
10. The JEDEC standard states that this is ‘ILLEGAL (3)’, however in this part is NOP.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{ss}	-0.5	4.5	V	
V_{DD},V_{DDQ}	Voltage on supply pins relative to V_{ss}	-0.5	4.5	V	
Ts	Storage Temperature	-55	150	°C	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions listed in the operational sections of this datasheet. Exposure to maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics and Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	
V_{DDQ}	Output Driver Supply Voltage	3.0	3.3	3.6	V	
V_{OH}	Output High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	
I_{IL}	Input Leakage Current	-1		1	uA	
I_{OL}	Output Leakage Current	-1		1	uA	
V_{IL}	Low Input Voltage	-0.5		0.8	V	
V_{IH}	High Input Voltage	2.0		V_{DDQ}+0.5	V	
T_A	Ambient Temperature	0	27	70	°C	

Note: All voltages referenced to VSS.

Capacitance

Symbol	Parameter	Min	Max	Units	Notes
C_{IN}	Input Pin Capacitance		5	pF	
C_{OUT}	I/O Pin Capacitance		6.5	pF	

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Notes
I_{CC1S}	Operating Current (Single Bank)		110	mA	t_{CLK}=min, t_{RC}=min, no burst
I_{CC1D}	Operating Current (Double Bank)		160	mA	t_{CLK}=min, t_{RC}=min, no burst
I_{CC2}	Standby Current		30	mA	CKE≥ V_{IH}
I_{CC3}	Clock Suspend Current		3	mA	CKE≤V_{IL}
I_{CC4}	Burst Mode Current		140	mA	
I_{CC5}	Auto Refresh Current		110	mA	t_{RC}=min
I_{CC6}	Self Refresh Current		0.6	mA	CKE≤V_{IL}
I_{CC7}	Power Down Current		2	mA	CKE≤V_{IL}

Note: All voltages referenced to VSS.
ICC specifications tested after proper initialization.
V_{DD}/V_{DDQ}=3.3V +/-0.3V, Ta=0 to 70°C
I_{CC} measurements are for outputs with no load.

AC Characteristics

Symbol	Parameter	66MHz		100MHz			
		Min	Max	Min	Max	Units	Notes
t_{CLK}	Clock Period		15		10	ns	
t_{CL}	Clock Low Time	5		3		ns	
t_{CH}	Clock High Time	5		3		ns	
t_{AC}	Output Valid From Clock(CL=3)		9		6	ns	
	Output Valid From Clock (CL=2)		9		6	ns	
t_{SI}	Input Setup Time	3		2		ns	
t_{HI}	Input Hold TIme	1.5		1		ns	
t_{OH}	Output Hold Time	3		3		ns	
t_{OHZ}	Output Valid to Hiz Time	3	12	3	9	ns	
t_{RC}	Row Cycle Time	120		80		ns	$8*t_{CLK}$
t_{RP}	Row Precharge Time	45		30		ns	$3*t_{CLK}$
t_{RAS}	Row Active Time	75		50		ns	$5*t_{CLK}$
t_{RCD}	Row Activate to Command Delay	30		20		ns	$2*t_{CLK}$
t_{RRD}	RAS to RAS Bank Activate Delay	30		20		ns	$2*t_{CLK}$
t_{WR}	Write Recovery Time	15		10		ns	$1*t_{CLK}$
t_{MRD}	Mode Register Set to Row Activate Delay	45		30		ns	$3*t_{CLK}$
t_{DQD}	DQM to Input Data Delay	0		0		ns	
t_{DWD}	Write Command to Input Data Delay	0		0		ns	
t_{ROH}	Precharge to Output in HiZ (CL=3)	CL		CL		ns	
t_{DQZ}	DQM to Data Output in HiZ	30		20		ns	$2*t_{CLK}$
t_{DPL}	Data In to Precharge Command	30		20		ns	$2*t_{CLK}$
t_{DAL}	Data In (Autoprecharge cycle) to Activate Command	75		50		ns	$5*t_{CLK}$
t_{SB}	Power Down Entry Time	15		10		ns	$1*t_{CLK}$
t_{SRX}	Self Refresh Exit Time	10		10		ns	
t_{PDE}	Power Down Exit Time	15		10		ns	$1*t_{CLK}$
t_T	Edge Transition Time	0.5		0.5		ns	

Note:

1.An initial pause of 500us is required after power-up before proper device operation is achieved. During this time both the CKE and DQM must be high. After the 500us delay, all banks must be precharged using the Precharge ALL banks command. After precharge is completed and the minimum tRP is satisfied, the mode register can be programmed.

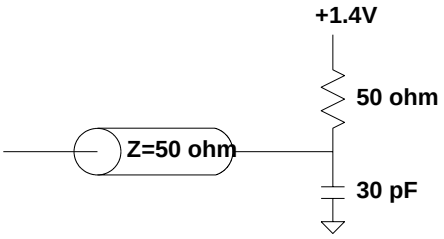
2. V_{DD}/V_{DDQ}=3.3V +/-0.3V, Ta=0 to 70°C

AC Operating Test Conditions

Symbol	Parameter	Value	Units	Notes
V_{IL}, V_{IH}	Input Levels	2.4/0.4	V	
	Input Timing Reference Level	1.4	V	
t_R	Input Rise Time	1	ns	
t_F	Output Rise Time	1	ns	
	Output Timing Reference Level	1.4	V	

Note: V_{DD}=3.3V +/-0.3V, Ta=0 to 70°C

AC Test Output Load



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