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TMS320FLEX Family

Messaging System Solutions With Alphanumeric Roaming Decoder

Design Manual

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TMS320FLEX Family Messaging System Solutions With Alphanumeric Roaming Decoder Design Manual

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Preface

Read This First

About This Manual

The Texas Instruments (TI™) *TMS320FLEX Family Messaging System Solutions With Alphanumeric Roaming Decoder Design Manual* describes the products that can be used to design embedded messaging functionality into computers, automobiles, and smart home electronics. This manual is part of a set of three manuals developed for this purpose (see *Related Documentation*).

This set of documents provides detailed information on the TLV5590 decoder and the analog-to-digital converters that enable you to develop embedded messaging functions that implement the FLEX protocol. Interfacing these components to your existing receivers and microcontrollers means that your application will required little, if any, hardware redesign.

The following decoders can be used with either the TLV5590 or TLV5592 converter to create a customized application.

- TLV5591BVF Alphanumeric Decoder
- TLV5594VF Numeric
- TLV5593VF Alphanumeric Roaming

Common features of the three decoders include:

- FLEX messaging protocol signal processor
- Decoding at 1600, 3200, or 6400 bits per second (bps)
- Real-time clock time base
- Low battery indication (external detector)
- Standard serial peripheral interface (SPI) in slave mode
- Highly programmable receiver control
- Compatible with synthesized receivers
- Low-current STOP mode operation of host processor

Features specific to each decoder include:

- TLV5591BVF Alphanumeric Decoder
  - 16 programmable user-address words
  - 16 fixed-temporary addresses
  - Any-phase decoding
- TLV5594VF Numeric
  - 4 programmable user-address words
  - Single-phase decoding
- TLV5593VF Alphanumeric Roaming
  - 16 programmable user-address words
  - 16 fixed temporary addresses
  - 16 operator messaging addresses
  - Any-phase or single-phase decoding
  - FLEX fragmentation and group messaging support
  - Real-time clock over-the-air update support
  - Simulcast system identifier (SSID) and network ID (NID) roaming support
  - 28 used pins (32-pin thin quad flatpack (TQFP) standard)
  - Pin-compatible with all other FLEX decoder signal processors

See Appendix C, *Mechanical Data*, for the package diagram that applies to each of the decoders.

How to Use This Manual

This manual contains the following chapters:

Chapter 1 Introduction
Presents an overview of FLEX™ messaging protocol and a general description of the TMS320FLEX Family chipset

Chapter 2 FLEX Signal Structure
Describes the TLV5593VF FLEX signal structure

Chapter 3 TLV5593VF FLEX Decoder
Describes the TLV5593VF FLEX decoder

Appendix A TLV5590 Data Sheet
Presents a complete TLV5590 converter data sheet with its own page numbering

Appendix B Timing Diagrams
Presents the timing diagrams for the TLV5593VF decoder

Appendix C Mechanical Data
Presents the mechanical data for the TLV5593VF decoder

Related Documentation From Texas Instruments

The following books describe the TMS320FLEX Family Decoders and related tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

TMS320FLEX1 Messaging System Solutions Design Manual (literature number SPRA086)

TMS320FLEX Family Messaging System Solutions With Numeric Decoder Design Manual (literature number SPRA183)

TMS320FLEX Family Messaging System Solutions With Alphanumeric Roaming Decoder Design Manual (literature number SPRA193)

Trademarks

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Chapter 1

Introduction

The Texas Instruments (TI™) TMS320FLEX Family Chipset With Alphanumeric Roaming Decoder simplifies implementation of the FLEX™ protocol in a messaging application by interfacing directly with most popular off-the-shelf messaging receivers and microcontrollers. You can quickly and easily develop a FLEX-compliant product by interfacing the TLV5590 converter and the TLV5593VF decoder to your existing receivers and microcontrollers with virtually no hardware redesign.

Purchase of the TMS320FLEX Family Chipset With Alphanumeric Roaming Decoder satisfies all licensing requirements for the FLEX protocol. No separate license agreement with Motorola is required.

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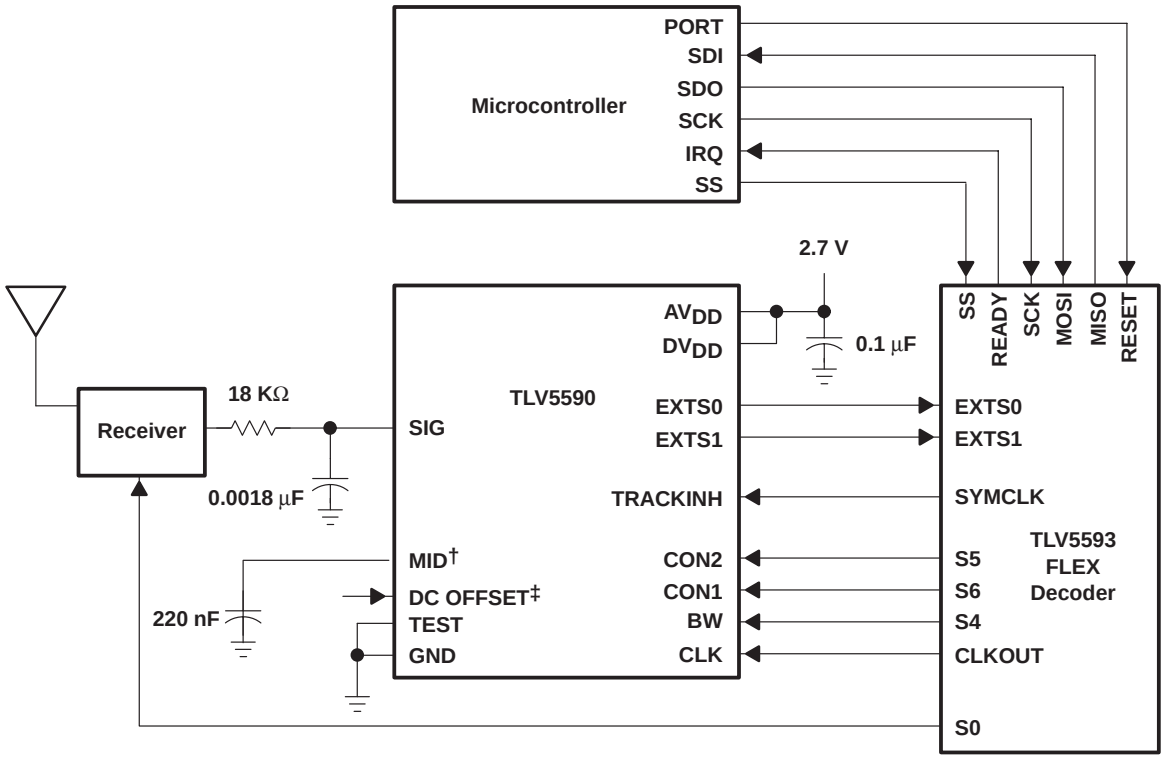
1.1 FLEX Messaging Overview

FLEX messaging protocol was developed by Motorola to provide a robust form of text and data messaging not previously available. Figure 1–1 shows a block diagram of a FLEX messaging device. The FLEX protocol brings new levels of functionality and service to pagers while providing you with the following benefits:

- ❑ Longer battery life than existing standards
- ❑ Support for numeric and alphanumeric messages
- ❑ High signal integrity for error protection and positive message termination
- ❑ Advanced features, such as group pages between systems
- ❑ Support for 1600-, 3200-, or 6400-bps transmissions
- ❑ Low upgrade costs by allowing gradual migration from FLEX 1600 to FLEX 3200 to FLEX 6400
- ❑ Increased number of subscribers per channel, thereby reducing infrastructure costs

Figure 1–1. FLEX Messaging Device



† The voltage on the MID terminal is nominally $AV_{DD}/2$.
‡ The voltage applied to the DC OFFSET terminal is set to the dc offset voltage of the input signal applied to the SIG terminal.

1.2 Chipset Description

The TMS320FLEX Family Chipset with Numeric Decoder consists of a TLV5593VF signal processor that decodes the FLEX messaging protocol transmission and the TLV5590 analog-to-digital (A/D) converter that converts the analog signal from the receiver into a digital signal for decoding by the TLV5593VF. FLEXstack™ system software to facilitate application development is also included. This software runs on a host processor and is specifically designed to support the TLV5593VF FLEX roaming decoder. It handles communications with the TLV5590 converter and interprets the code words passed to the host from the TLV5593VF decoder.

The flexible architecture of the TMS320FLEX chipset offers a variety of possibilities in application design.

1.2.1 TLV5593VF FLEX Roaming Decoder

The TLV5593VF FLEX roaming decoder has the following features:

- ❑ FLEX messaging protocol signal processor
- ❑ 16 programmable user-address words
- ❑ 16 fixed temporary addresses
- ❑ 16 operator messaging addresses
- ❑ Decoding at 1600, 3200, or 6400 bps
- ❑ Any-phase or single-phase decoding
- ❑ Standard serial peripheral interface (SPI) in slave mode
- ❑ Low-current STOP mode operation of host processor
- ❑ Highly programmable receiver control
- ❑ Real-time clock time base
- ❑ FLEX fragmentation and group messaging support
- ❑ Real-time clock over-the-air update support
- ❑ Compatibility with synthesized receivers
- ❑ SSID and NID roaming support
- ❑ Low battery indication (external detector)
- ❑ 28 used pins (32-pin package standard)
- ❑ Pin-compatible with all other FLEX decoder signal processors

1.2.2 TLV5590 A/D Converter

The TLV5590 A/D converter has the following features:

- ❑ Selectable dual-bandwidth audio filter
  - ■ Three-pole Butterworth low-pass
  - ■ BW 1 = 1 KHz +/–5% (–3 db)
  - ■ BW 2 = 2 KHz +/–5% (–3 db)
- ❑ Peak and valley detectors
- ❑ Two-bit A/D converter
- ❑ Four modes of operation: fast track, slow track, hold, and standby
- ❑ Operation at 2.7-V to 3.3-V with a single power supply

See Appendix A, *TLV5590 Data Sheet*, for more information.

Chapter 2

FLEX Signal Structure

The FLEX signal transmitted on the radio channel consists of a series of four-minute cycles, each cycle having 128 frames at 1.875 seconds per frame. A pager may be assigned to process any number of the frames. Battery saving is performed for frames that are not assigned. The FLEX signal can assign additional frames to the pager using collapse, fragmentation, temporary addressing, or carry-on information within the FLEX signal. This chapter discusses the FLEX signal structure.

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2.1 Synchronization

Figure 2–1 shows the FLEX signal structure.

Each FLEX frame has a synchronization portion followed by an 11-block data portion, each block lasting 160 milliseconds. The synchronization portion indicates the rate at which the data portion is transmitted, 1600, 3200, or 6400 bits per second (bps). The 1600 bps rate is transmitted at 1600 symbols per second (sps) using 2-level frequency shift key (FSK) modulation and consists of a single phase of information at 1600 bps called *phase A.* The 3200 bps rate is transmitted at either 1600 sps using 4-level FSK modulation or 3200 sps using 2-level FSK modulation and consists of two concurrent phases of information at 1600 bps called *phase A* and *phase B*. The 6400 bps rate is transmitted at 3200 sps using 4-level FSK modulation and consists of four concurrent phases of information at 1600 bps called *phase A*, *phase B*, *phase C*, and *phase D*.

Each block has eight interleaved words per phase; there are eighty-eight words, numbered 0 – 87, per phase in every frame. Each word has information contained within an error correcting code that allows for bit error correction and detection. The eighty-eight words in each phase are organized into a block information field, an address field, a vector field, a message field, and an idle field. The boundaries between the fields are independent of the block boundaries. Furthermore, at 3200 and 6400 bps, the information in one phase is independent of the information in a concurrent phase, and the boundaries between the fields of one phase are unrelated to the boundaries between the fields in a concurrent phase.

The synchronization portion consists of a first sync signal at 1600 bps; a Frame Information Word having the Frame Number 0 – 127 (7 bits) and the Cycle Number 0 – 14 (4 bits); and a second sync signal at the data rate of the interleaved portion.

2.1.1 Block Information Field

The block information field may contain block information words for determining time and date information and certain paging system information.

2.1.2 Address Field

The address field contains addresses assigned to paging devices. Addresses are used to identify information sent to individual paging devices and/or groups of paging devices. An address may be either a short one-word address or a long two-word address. Information in the FLEX signal may indicate that an address is a priority address. An address may be a *tone-only* address in which case there is no additional information associated with the address. If an address is not a tone-only address, then there is an associated vector word in the vector field. Information in the FLEX signal indicates the location of the vector word in the vector field associated with the address. Short addresses have one associated vector word, and long addresses have two associated vector words. A pager may battery save at the end of the address field when its address is not detected.

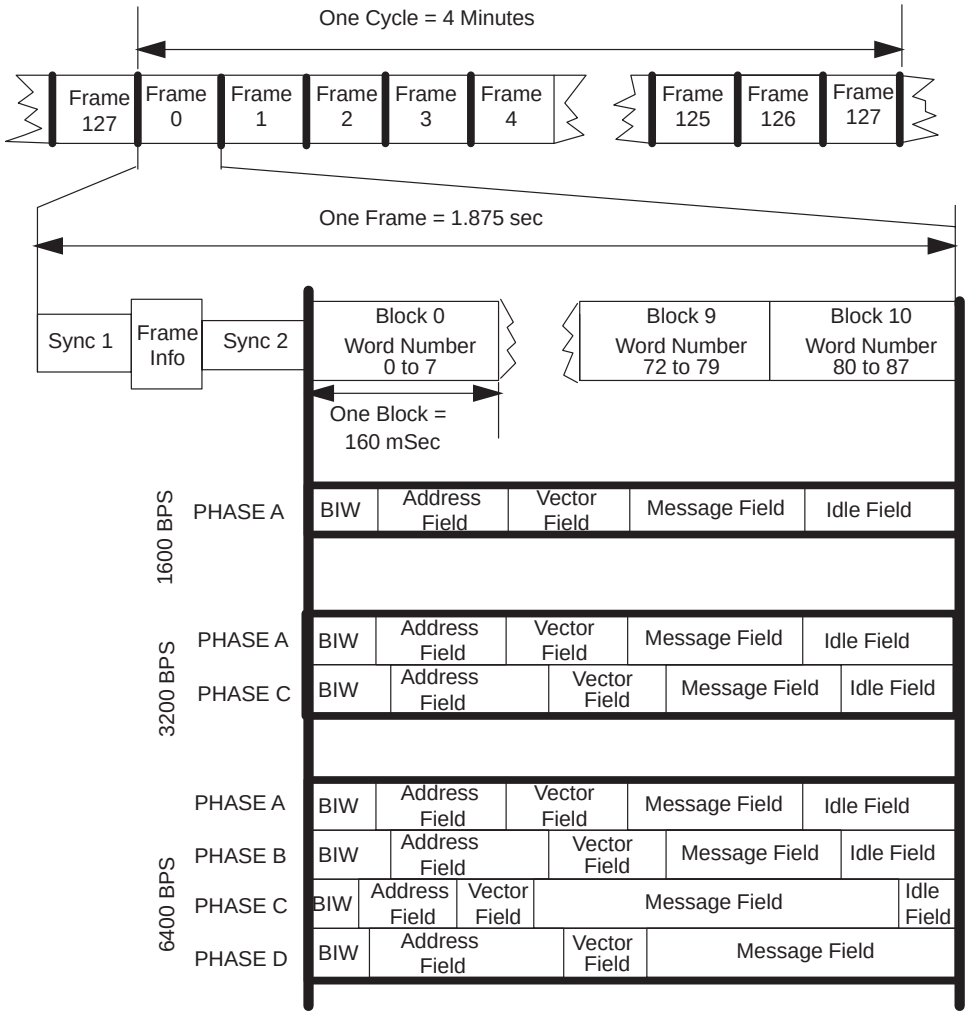
2.1.3 Vector Field

The vector field consists of a series of vector words. Depending upon the type of message, a vector word (or words in the case of a long address) may either contain all of the information necessary for the message, or indicate the location of message words in the message field comprising the message information.

2.1.4 Message Field

The message field consists of a series of information words containing message information. The message information may be formatted in ASCII, binary coded decimal (BCD), or binary, depending upon the message type.

Figure 2–1. FLEX Signal Structure



2.2 FLEX Message Word Definitions

FLEX message word definitions are discussed in this section.

2.2.1 Numeric Data Message

Table 2–1 and Table 2–2 describe the bit format of the numeric messages. The 4-bit numeric characters of the message are designated as lowercase letters a, b, c, d, etc.

Table 2–1. Standard (V = 011) or Special (V = 100) Format: 4, 10, 15, 20, 25, 31, 36, or 41 Characters

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e2
2nd	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3
3rd	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0
4th	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1
5th	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2
6th	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3
7th	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0
8th	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	T_0	T_1	T_2	T_3	U_0	U_1

Table 2–2. Numbered (V = 111) Format: 2, 8, 13, 18, 23, 29, 34, or 39 Numeric Characters

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	N_0	N_1	N_2	N_3	N_4	N_5	R_0	S_0	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2
2nd	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3
3rd	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0
4th	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1
5th	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2
6th	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3
7th	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V
8th	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1

2.2.2 Bit Definitions

K: 6-bit Message Check Character (First 4 bits are in the vector word). This check character is calculated by initializing the message check character (K) to zero and summing the information bits of each code word in the message, (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: bits i_0 through i_7, bits i_8 through i_{15}, and bits i_{16} through i_{20}. Bits i_0, i_8 and i_{16} are the LSBs of each group. The binary sum is calculated and the result is shortened to the 8 least significant bits. The 2 most significant bits are shifted right 6 bits and summed with the least significant 6 bits to form a new sum. This resultant sum is 1's complemented with the 6 LSBs of the result being transmitted as the message check character.

N: Message Number: When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing to a maximum of 63 in consecutive order. The actual maximum roll-over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) by allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (Message Retrieval Flag is equal to 0), it is not included in the missed message calculation.

R: Message Retrieval Flag: When this bit is set to 1, the pager expects to see messages numbered in order (each address numbered separately). Detection of a missing number indicates a missed message. A message received with R = 0 is allowed to be out of order and does not cause the pager to indicate that a message has been missed.

S: Special Format: In the numbered message format, this bit set to 1 indicates that a special display format should be used.

2.2.3 Message Fill Rules

For numeric messages of 36 characters or less (34 characters if numbered), fewer than 8 code words on the channel are required. Only code words containing the numeric message can be transmitted. The space character (hexadecimal C) should be used to fill any unused 4-bit characters in the last word, and zeros should be read to fill any remaining partial characters. The check sum is correspondingly shortened to include only the code words comprising the shortened message along with the space and fill characters used to fill in the last word.

2.2.4 Special Format Numeric

Spaces and dashes as specified by the host are inserted into the received message. This feature in certain markets saves the transmission of an additional word on the channel. For example, in the U.S. market a 10-character format (area code plus telephone number) fits into two message words. If the dashes or parentheses are included in the message, three message words on the channel are required. The actual placement can be programmed into the paging device and can vary between markets.

2.3 Hex/Binary Message

Table 2–3 and Table 2–4 describe the bit format of the Hex/Binary messages. The data of the message is designated as lowercase letters a, b, c, d, etc. Hex/Binary messages can be sent as fragments. The service provider has the option of dividing the message into several pieces and sending the separate pieces at any time within a given time period.

Table 2–3. Vector Type V = 110, First Only Fragment

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	R_0	M_0	D_0	H_0	B_0	B_1	B_2	B_3	s_0	s_1	s_2	s_3	s_4	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
3rd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
4th	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
5th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
6th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 2–4. Vector Type V = 110, All Other Fragments

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
3rd	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
4th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
5th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

2.3.1 Bit Definitions

K: 12-bit Fragment Check Sum. This Check Sum is calculated by initializing the Fragment Check Sum field (K) to zero and calculating a sum over the information bits of each code word in the message fragment (including control information and termination characters/bits in the last fragment word). This sum requires that the information bits of each word be broken into three groups: the first is the 8 bits comprising i_0 through i_7, the second group comprises bits i_8 through i_{15}, and the third group comprises bits i_{16} through i_{20}. Bits i_0, i_8 and i_{16} are the LSBs of each group. The binary sum is calculated over all code words in the fragment, the 1's complement of the sum is determined, and the 12 LSBs of the result is placed into the Fragment Check Sum field to be transmitted at the beginning of the fragment.

C: 1-bit Message Continued Flag. When set to 1, indicates fragments of this message are to be expected in any or possibly all of the following frames until a fragment with **C** = 0 is found. The longest message which will fit into a frame is 84 code words total. Three alpha characters per word yields a maximum message of 252 characters in a frame, assuming no other traffic. Messages longer than this value must be sent as several fragments.

F: 2-bit Message Fragment Number. This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. The initial fragment starts at 11 and each following fragment is incremented by 1 modulo 3. (11, 00, 01, 10, 00, 01, 10, 00 etc.). The 11 state (after the initial fragment) is skipped in this process to avoid confusion with the single fragment of a non-continued message. The final fragment is indicated by the Message Continued Flag being reset to 0.

N: Message Number. When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in consecutive order. The actual maximum rollover number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag is equal to 0), it is not to be included in the missed message calculation. This number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers. An exception to this rule is the header message tied to a transparent message each with the same message number.

R: Message Retrieval Flag. When this bit is set to 1, the pager expects to see messages numbered in order (each address numbered separately). Detection of a missing number indicates a missed message. A message received with R = 0 is allowed to be out of order and does not cause the pager to indicate that a message has been missed.

M: 1-bit Mail Drop Flag. When set to 1, indicates the message is to be stored in a special area in memory. It automatically writes over existing data in that memory space.

D: 1-bit Display Direction Field. D = 0 – Display left to right, D = 1 – Display right to left (valid only when data is sent as characters, i.e., Blocking Length not equal 0001).

H: 1-bit Header Message. H = 1 Indicates that this message is a header to a following transparent message of the same message number. H = 0 implies message is not a header.

B: 4-bit Blocking Length. Indicates bits per character. $B_3B_2B_1B_0$ = 0001 = 1 bit per character (binary/transparent data), 1111 =15 bits per character, 0000 =16 bits per character. Data with blocking length other than 1 is assumed to be displayed on a character by character basis. (default value = 0001). Note that the above figures show B = 4-bit blocking length.

s: 5-bit Field Reserved for future use. Default value = 00000

S: 8-bit Signature Field. The signature is defined to be the 1's complement of the binary sum over the total message taken 8 bits at a time prior to formatting into fragments. It would be equivalent to a binary sum starting with the first 8 bits directly following the signature field ($b_3b_2b_1b_0a_3a_2a_1a_0$ + $d_3d_2d_1d_0c_3c_2c_1c_0$ and so on.) and continuing all the way to the last valid data bit in the last word of the last fragment. The 8 least significant bits of the result are inverted (1's complement) and transmitted as the message signature. (Note: This sum does not include any termination bits and should be calculated directly on the message as received by the terminal. The device generating the signature should be able to calculate this sum before the fragmenting boundaries are determined.)

Fields R through S are only transmitted in the first fragment of a message. The fields K through N make up the first word of every fragment in a long message.

2.3.2 Message Content

Starting with the first character of the third word in the message (second word in the remaining fragments), each 4-bit field represents 1 of any of the 16 possible combinations with no restrictions (data may be binary).

2.3.3 Fragment Termination

Unused bits in the last message word of a fragment are filled with all 0's or all 1's depending on the last valid data bit. This choice is always the opposite polarity of the last valid data bit. For first fragments and inner fragments of a multifragment message, the message is interrupted (stopped) on the last full character boundary in the last code word in the fragment. Any unused bits follow this rule. The final fragment follows the above rules except when the last character is all 1's or all 0's and it exactly fills the last code word. In this case, an additional word must be sent of opposite polarity of all 1's or all 0's to signify the position of the last character thus allowing that last character to be an all 1's or an all 0's character pattern. (This is always the case when a binary message ends in the last bit of the last word.)

2.3.4 Message Header

A message header is designated by setting the H bit to 1. This is a displayable tag associated with a transparent/non-displayable data message. The tag and the associated message are complete in themselves. The pager associates the header message with the data file based on the two having the same message number and being sent in sequence (header first followed by data file).

2.4 Alphanumeric Message

Table 2–5 and Table 2–6 describe the bit format of the alphanumeric messages. The 7-bit characters of the message are designated as lowercase letters a, b, c, d, etc. Alphanumeric Messages can be sent as fragments. The service provider has the option of dividing the message into several pieces and sending the separate pieces at any time within a given time period.

Table 2–5. Vector Type V = 101, First Only Fragment

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	R_0	M_0
2nd	S_0	S_1	S_2	S_3	S_4	S_5	S_6	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6
3rd	c_0	c_1	c_2	c_3	c_4	c_5	c_6	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6
4th	f_0	f_1	f_2	f_3	f_4	f_5	f_6	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6
5th	i_0	i_1	i_2	i_3	i_4	i_5	i_6	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 2–6. Vector Type V = 101, Other Fragment

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	U_0	V_0
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

2.4.1 Bit Definitions

K: 10-bit Fragment Check Character. This check character is calculated by initializing the fragment check character (K) to zero and summing the information bits of each code word in the message fragment (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: the first is the 8 bits comprising i_0 through i_7, the second group comprises bits i_8 through i_{15}, and the third group comprises bits i_{16} through i_{20}. Bits i_0, i_8, and i_{16} are the LSBs of each group. The binary sum is calculated, the 1's complement of the sum is determined and the 10 LSBs of the result is transmitted as the message check character.

C: 1-bit Message Continued Flag. When set (= 1) indicates fragments of this message are to be expected in following frames. The longest message which will fit into a frame is 84 code words total. Three alpha characters per word yields a maximum message of 252 characters in a frame assuming no other traffic. Messages longer than this value must be sent as several fragments.

F: 2-bit Message Fragment Number. This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. Initial fragments start at 11 and increment 1 for each successive fragment. The 11 state (after the start fragment) is skipped in this process to avoid confusion with an initial fragment of a non-continued message. The final fragment is indicated by Message Continued Flag being reset (= 0).

N: Message Number. When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in consecutive order. The actual maximum rollover number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag is equal to 0), it is not to be included in the missed message calculation. This number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.

R: Message Retrieval Flag. When this bit is set to 1, the pager expects to see messages numbered in order (each address numbered separately). Detection of a missing number indicates a missed message. A message received with R = 0 is allowed to be out of order and does not cause the pager to indicate that a message has been missed.

M: 1-bit Mail Drop Flag. When set (= 1) indicates the message is to be stored in a special area in memory. It automatically writes over existing data in that memory space.

S: 7-bit Signature Field. The signature is defined to be the 1's complement of the binary sum over the total message (all fragments) taken 7 bits at a time (on alpha character boundary) starting with the first 7 bits directly following the signature field ($a_6a_5a_4a_3a_2a_1a_0$, $b_6b_5b_4b_3b_2b_1b_0$, etc.). The 7 least significant bits of the result is transmitted as the message signature.

U, **V**: Fragmentation Control Bits. This field exists in all fragments except the first fragment. It is used to support character position tracking in each fragment when symbolic characters (characters made up of 1, 2, or 3 ASCII characters) are transmitted using the Alphanumeric message type. The default value is 0,0. See subsection 2.4.5, *Enhanced Fragmentation Rules,* for more information.

2.4.2 Message Content

Starting with the second character of the second word in the message (first character of the second word in all remaining fragments), each 7-bit field represents Standard ASCII (ISO 646–1983E) characters with options for certain International characters.

2.4.3 Message Termination

The ASCII character ETX (03) should be used to fill any unused 7-bit characters in a word. In the case where symbolic characters are being transmitted special rules for fragment and message termination are defined in 2.4.4, *Alphanumeric Message Rules for Symbolic Characters Sets*.

2.4.4 Alphanumeric Message Rules for Symbolic Characters Sets

In the past, paging protocols have supported symbolic characters like Chinese, Kanji, etc., using a 7-bit ASCII protocol. When the FLEX alphanumeric mode is used to carry this same signaling format, special fragmenting rules are required to maintain character boundaries so performance is optimized under poor signal conditions. The following rules allow character positions within a fragment to be determined when prior fragments are missing.

2.4.5 Enhanced Fragmentation Rules

- The pager must recognize <NUL> characters only at the end of fragments where they are used as fill characters. The pager must remove these characters so that the displayed message is not affected. In all other positions the NUL character must be considered a result of channel errors. (This provides a method to end each fragment with a complete character and does not disrupt the pager, which is not capable of following all of the EF (Enhanced Fragmenting) rules.)

- The last fragment is to be completed by filling unused character positions with <ETX> characters or <NUL> characters. (Original FLEX alphanumeric message definition (<ETX>) plus the new <NUL> requirement. When message ends exactly in the last character position in the last BCH code word, no additional <ETX> is required).

- The U and V bits in the message header are available in all fragments following the initial fragment to aid in decoding. In the first fragment, the pager must assume the message starts in the default character mode. For the second and remaining fragments, the definition of the (U,V) field is as shown in Table 2–7.

Table 2–7. Vector Type V = 101, Other Fragment

U_0	V_0	Definition
0	0	EF not supported in controller
0	1	Reserved (for a second alternate character mode)
1	0	Default Character Mode – start position 1
1	1	Alternate Character Mode – start position 1

When the EF field is 0 0, the pager decodes messages, allowing characters to be split between fragments. When the U,V field is not 0 0, each fragment starts on a character boundary with the character mode defined by the above table.

2.5 Secure Message

Table 2–8 describes the bit format of the secure messages. The 7-bit characters of the message are designated as lowercase letters a, b, c, d, etc. Secure Messages can be sent as fragments. The service provider has the option of dividing the message into several pieces and sending the separate pieces at any time within a given time period.

Table 2–8. Vector Type V = 000, All Fragments

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	s_0	s_1
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

2.5.1 Bit Definitions

K: 10-bit Fragment Check Character. This check character is calculated by initializing the fragment check character (K) to zero and summing the information bits of each code word in the message fragment (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: the first is the 8 bits comprising i_0 through i_7, the second group comprises bits i_8 through i_{15}, and the third group comprises bits i_{16} through i_{20}. Bits i_0, i_8, and i_{16} are the LSBs of each group. The binary sum is calculated, the 1's complement of the sum is determined, and the 10 LSBs of the result are transmitted as the message check character.

C: 1-bit Message Continued Flag. When set (= 1) indicates fragments of this message are to be expected in following frames. The longest message which will fit into a frame is 84 code words total. Three alpha characters per word yields a maximum message of 252 characters in a frame, assuming no other traffic. Messages longer than this value must be sent as several fragments.

F: 2-bit Message Fragment Number. This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. Initial fragments start at 11 and increment 1 for each successive fragment. The 11 state (after the start fragment) is skipped in this process to avoid confusion with an initial fragment of a non-continued message. The final fragment is indicated by Message Continued Flag being reset (= 0).

N: Message Number. When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in consecutive order. The actual maximum rollover number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume that a message has been missed. The subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag is equal to 0), it is not to be included in the missed message calculation. This number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.

s: Spare bit not used and set to 0.

2.5.2 Message Content

Starting with the first character of the second word in the message (and first character of all remaining fragments), each 7-bit field represents Standard ASCII (ISO 646–1983E) characters with options for certain international characters.

2.5.3 Message Termination

The ASCII character ETX (03) should be used to fill any unused 7-bit characters in a word.

2.6 FLEX Encoding and Decoding Rules

The encoding and decoding rules identify the minimum requirements that must be met by the paging device, paging terminal, or other encoding equipment to properly format a FLEX data stream for radio frequency (RF) transmission and to successfully decode it. The encoding and decoding rules explained in this section pertain to the FLEX messaging capabilities of the alphanumeric FLEX roaming decoder.

2.6.1 FLEX Encoding Rules

- The stability of the encoder clock used to establish time positions of FLEX frames must be no worse than +/–25 ppm (including worst-case temperature and aging effects).
- A maximum of two occurrences of an identical individual or radio group address is allowed in any frame for unfragmented messages. This rule applies across all phases in a multi-phase frame. For example, for paging devices that support any-phase addressing, an any-phase address may appear only once in two different phases, in a single phase of a single multi-phase frame.
- Once an individual or radio group address is used to begin transmitting a fragmented message, that same address must not be used to start a new fragmented transmission until the first fragmented transmission has been completed.
- For the duration of time that an individual or radio group address is being used to send a fragmented message, that same address must not appear more than once in any frame to send an unfragmented message.
- Once a specific dynamic group address (temporary address) is assigned to a group, it must not be reused until its associated message has been transmitted in its entirety. Given this constraint, the same dynamic group address can only appear once in any frame.
- A dynamic group address cannot be used to set up a second dynamic group.
- Messages using any of the three defined numeric vectors ($V_2V_1V_0$ = 011, 100, and 111) cannot be fragmented, and thus must be completely contained in a single frame.
- Fragments of the same message must be sent at a frequency of at least 1 every 32 frames (at least once a minute) or 1 every 128 frames (at least once every 4 minutes) as specified by the service provider.
- Enhanced message fragmenting for symbolic character transmission requires that the encoder track character boundaries within each fragment to avoid character splitting.
- Message numbering as an optional feature is offered by some carriers and available on an individual subscriber basis.

- ❏ Message numbers must be assigned sequentially in ascending order.
- ❏ Message number sequences must be separately maintained for each individual and radio group address.
- ❏ Message numbers are not used (retrieval message number disabled) in conjunction with a dynamic group address.
- ❏ When a missed page is retransmitted from message retrieval storage, the message must have R = 0 to avoid creating an out-of-sequence message that may cause the pager to indicate a missed message.

2.6.2 FLEX Decoding Rules

- ❏ FLEX decoding devices may implement either single-phase addressing or any-phase addressing.
- ❏ FLEX decoding devices that support the numeric vector type ($V_2V_1V_0$ = 011) must also support the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00.
- ❏ FLEX decoding devices that support the alphanumeric vector type ($V_2V_1V_0$ = 101) must support the numeric vector type ($V_2V_1V_0$ = 011) and the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00. FLEX paging devices that implement any-phase addressing and support the alphanumeric vector type ($V_2V_1V_0$ = 101) must also support the short instruction vector ($V_2V_1V_0$ = 001) with the instruction type ($i_2i_1i_0$) set to 000.
- ❏ FLEX decoding devices must be capable of decoding frames at all of the following combinations of data rate and modulation mode: 1600 bps, 2 level; 3200 bps, 2 level; 3200 bps, 4 level; 6400 bps, 4 level.
- ❏ FLEX decoding devices must be designed to tolerate 4-minute fragment separation times.

2.7 FLEX Character Sets and Rules

The alphanumeric and numeric character sets are discussed in this section.

2.7.1 Alphanumeric Character Set

Table 2–9 defines the characters to be displayed in the FLEX alphanumeric message mode. Control characters that are not acted upon by the pager are ignored in the display process (do not require display space) but are stored in memory for possible download to an external device.

Table 2–9. Alphanumeric Character Set

Least Significant 4 Bits of Character	Most Significant 3 Bits of Character							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	NUL	DLE	SP	0	@	P	‘	p
1	SOH	DC1	!	1	a	q	a	q
2	STX	DC2	“	2	b	r	b	r
3	ETX	DC3	#	3	c	s	c	s
4	EOT	DC4	$	4	d	t	d	t
5	ENQ	NAK	%	5	e	u	e	u
6	ACK	SYN	&	6	f	v	f	v
7	BEL	ETB	’	7	g	w	g	w
8	BS	CAN	(	8	h	x	h	x
9	TAB	EM	)	9	i	y	i	y
A	LF	SUB	*	:	j	z	j	z
B	VT	ESC	+	;	k	[	k	{
C	FF	FS	,	<	l	\	l	|
D	CR	GS	–	=	m	]	m	}
E	SO	RS	.	>	n	^	n	~
F	SI	US	/	?	o	_	o	DEL

2.7.2 Numeric Character Set

Table 2–10 and Table 2–11 define the characters to be displayed in the FLEX numeric message mode.

Table 2–10. Standard Character Set (Peoples Republic of China Option Off)

Character	B_3	B_2	B_1	B_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
Spare	1	0	1	0
U	1	0	1	1
Space	1	1	0	0
–	1	1	0	1
]	1	1	1	0
[	1	1	1	1

Table 2–11. Alternate Character Set (Peoples Republic of China Option On)

Character	B_3	B_2	B_1	B_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
Space	1	1	0	0
C	1	1	0	1
D	1	1	1	0
E	1	1	1	1

2.8 FLEX Local Time and Date

The FLEX protocol allows for systems to transmit time information in its Block Information Field. When a system provider supports local time transmissions, the system provider is required, at a minimum, to transmit at least one time-related block information word (BIW) in each phase transmitted in frame 0, cycle 0. The time transmitted is the local time for the transmitted time zone and refers to the actual time at the leading edge of the first bit of Sync 1 of Frame 0 of the current cycle. The information carried in the **s** bits of the block information word depend on the value of the **f** bits of the block information word. Table 2–12, Table 2–13, and Table 2–14 describe the bit definitions of the time-related block information words.

2.8.1 Month/Day/Year

Table 2–12. Month/Day/Year Block Information Word Definition

$f_2f_1f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	Description
001	m_3 m_2, m_1 m_0 d_4 d_3 d_2 d_1 d_0 Y_4 Y_3 Y_2 Y_1 Y_0	Month/Day/Year

m: Month field. 0001 through 1100 (binary) correspond to January through December, respectively.

d: Day field. 00001 through 11111 (binary) correspond to 1 through 31, respectively.

Y: Year field. This represents the year with modulo arithmetic (00000 through 11111 (binary), representing 1994 through 2025, 2026 through 2057, etc.

2.8.2 Second/Minute/Hour

Table 2–13. Second/Minute/Hour Block Information Word Definition

$f_2f_1f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	Description
010	S_5 S_4 S_3 M_5 M_4 m_3 M_2 M_1 M_0 H_4 H_3 H_2 H_1 H_0	Second/Minute/Hour

S: Second field. This represents a coarse value of the seconds field. These bits represent the seconds in 1/8 of a minute (7.5 second) increments. 000 through 111 (binary) correspond to 0 through 52.5 seconds, respectively.

M: Minute field. 000000 through 111011 (binary) correspond to 0 through 59, respectively.

H: Hour field. 00000 through 10111 (binary) correspond to 0 through 23, respectively.

2.8.3 Accurate Seconds/Daylight Savings Time/Time Zone

Table 2–14. System Message Block Information Word Definition

$f_2f_1f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	Description
101	S_2 S_1 S_0 x L_0 z_4 z_3 z_2 z_1 z_0 0 1 0 X	System Message

Note: When the s3 s2 s1 s0 field is set to 0100 or 0101, the other s4 through s13 are defined as above. The system messages with the s3 s2 s1 s0 field set to some other value do not contain time-related information.

S: Accurate Seconds. This field provides a more accurate seconds reference and can be used to adjust the seconds to within 1 second. This field represents how much time should be added to the coarse seconds in 1/64-of-a-minute increments.

L: Daylight Savings Time. When this bit is set, the time being transmitted is Local Standard Time. When it is clear, the time being transmitted is Daylight Savings Time.

Z: Time Zone. These bits indicate the time zone for which the time is being transmitted. The offset from GMT is the offset for local standard time. Table 2–15 describes the values for z.

Table 2–15. Time Zone Values

$z_4z_3z_2z_1z_0$	Time Zone
00000	GMT
00001	GMT+0100
00010	GMT+0200
00011	GMT+0300
00100	GMT+0400
00101	GMT+0500
00110	GMT+0600
00111	GMT+0700
01000	GMT+0800
01001	GMT+0900
01010	GMT+1000

$z_4z_3z_2z_1z_0$	Time Zone
01011	GMT+1100
01100	GMT+1200
01101	GMT+0330
01110	GMT+0430
01111	GMT+0530
10000	RESERVED
10001	GMT+0545
10010	GMT+0630
10011	GMT+0930
10100	GMT–0330
10101	GMT–1100

$z_4z_3z_2z_1z_0$	Time Zone
10110	GMT–1000
10111	GMT–0900
11000	GMT–0800
11001	GMT–0700
11010	GMT–0600
11011	GMT–0500
11100	GMT–0400
11101	GMT–0300
11110	GMT–0200
11111	GMT–0100

2.9 FLEX CAPCODE

To send messages to a FLEX decoding device, the FLEX service provider must know the *device address*, *address type* (single-phase, any-phase, or all-phase), *address assigned phase*, *address assigned frame*, and the *address battery cycle*. This information is typically included in a FLEX CAPCODE. The assignment of CAPCODEs is regulated to prevent duplication of addresses on a system. Check with your FLEX service provider or other appropriate regulatory body for FLEX CAPCODE assignments. This section defines the FLEX CAPCODE parameters.

The device address consists of one or two 21-bit words. A one-word address is called a short address, and a two-word address is called a long address. Address words are separated into ranges according to Table 2–16.

Table 2–16. Address Word Range Definitions

Type	Hexadecimal Value
Idle Word (Illegal Address)	000000
Long Address 1	000001 through 008000
Short Address	008001 through 1E0000
Long Address 3	1E0001 through 1E8000
Long Address 4	1E8001 through 1F0000
Short Address (Reserved)	1F0001 through 1F27FF
Information Service Address	1F2800 through 1F67FF
Network Address	1F6800 through 1F77FF
Temporary Address	1F7800 through 1F780F
Operator Messaging Address	1F7810 through 1F781F
Short Address (Reserved)	1F7820 through 1F7FFE
Long Address 2	1F7FFF through 1FFFFE
Idle Word (Illegal Address)	1FFFFF

Long addresses are grouped into sets, as shown in Table 2–17.

Table 2–17. Long Address Sets

Long Address Set	First Word	Second Word
1–2	Long Address 1	Long Address 2
1–3	Long Address 1	Long Address 3
1–4	Long Address 1	Long Address 4
2–3	Long Address 2	Long Address 3
2–4	Long Address 2	Long Address 4

The address type indicates how messages on a particular address can be delivered in multi-phase FLEX frames. Messages sent on single-phase addresses can only be delivered in a particular phase (a, b, c, or d). Messages sent on any-phase addresses can be delivered in any phase, but a single message is limited to a single phase per frame. Messages sent on all-phase addresses can be delivered in any phase, and a single message can be spread across multiple phases in a single frame. All-phase messaging is a future feature of FLEX and has not been completely defined.

The address assigned phase is required only for single-phase devices. It determines the phase (a, b, c, or d) in which the messages are sent.

The address assigned to the frame and battery cycle determines the frames in which the decoding device typically looks for messages (other system factors can cause the decoding device to look in other frames in addition to the typical frames).

The address battery cycle is a number between 0 and 7 that defines how often the decoding device looks for messages on the FLEX channel. For a given battery cycle, b, the decoding device looks in every 2^b frame. Thus, an address with an assigned frame of 3 and a battery cycle of 5 typically looks for messages in frame 3 and every 32 frames thereafter (i.e., frames 3, 35, 67, and 99).

The FLEX CAPCODE is defined to represent either a Short or a Long address. The short address is defined in the FLEX protocol as one code word on the RF channel and is represented by a 7-digit decimal field. The long address is defined in the FLEX protocol as two code words on the RF channel and is represented by a 9- or 10-digit decimal field. The long addresses in set 1–2 are represented by a 9-digit decimal field. The long addresses in sets 1–3, 1–4, 2–3, and 2–4 are represented by a 10-digit decimal field. An alphabetic character known as the *CAPCODE type* always precedes the 7-, 9-, or 10-digit decimal address field. The CAPCODE type indicates the type of address and distinguishes FLEX CAPCODEs from CAPCODEs of other paging protocols.

2.9.1 CAPCODE Type

Example CAPCODE types are shown in Table 2–18. The CAPCODE type can be any of A through L or U through Z. The CAPCODE types A through L indicate that the standard rules are used to derive the assigned frame and phase information from the address field (See subsection *2.9.2, Standard Frame and Phase Embedding Rule*). For these CAPCODE types, the battery cycle (indicated as a b in example 1) is indicated by a single decimal digit, 0 through 7, preceding the CAPCODE type. When the FLEX standard battery cycle of 4 (16 frame cycle) is used, the battery cycle digit is not required (see example 2).

The CAPCODE types U through Z indicate that the standard frame and phase embedding rules were not used and additional information is required. The phase assignment can be derived from the CAPCODE type as described in Table 2–18. The 3-digit decimal frame assignment, 000 through 127 (indicated by fff in example 3), may precede this CAPCODE type. The frame and battery

cycle fields are not required. When they are not included (see example 4), the paging device or the subscriber database must be accessed to determine the assigned frame and battery cycle.

The extended CAPCODE is a regular CAPCODE with a 10-digit address field preceded by an extra alphabetic character, P through S. These CAPCODEs are used to provide additional information required for roaming devices.

Table 2–18. FLEX CAPCODE Examples

Example	Short	Long	Extended
1	bA1234567	bA123456789	RbA1234567890
2	A1234567	A123456789	RA1234567890
3	fffbU1234567	fffbU123456789	RffffbU1234567890
4	U1234567	U123456789	RU1234567890

By using the convention of 7 digits to represent short addresses, 9 digits to represent some of the long addresses in set 1–2, and 10 digits to represent the balance of long addresses, it is possible to differentiate between the different types of addresses. The range of the decimal address field consists of the numbers 1 through 5,370,810,366 where short and other single code word addresses fall below 2,031,615, and long addresses are above 2,101,248.

The goal in displaying a CAPCODE is to use the shortest form possible. Even though the nonstandard form could represent a standard assignment, the standard form is chosen to indicate that it is a standard assignment. All CAPCODE forms, except example 4 in Table 2–18, contain the information required to send a message to a subscriber unit.

2.9.2 Standard Frame and Phase Embedding Rule

Maximum battery life in a FLEX decoding device is achieved when all of the addresses assigned to a device are in the same frame. For single-phase decoding devices, all assigned addresses are required to be in the same phase.

Typically, it is desirable to spread the population of FLEX subscriber units on a system across all four phases of all 128 frames. Frame and phase spreading can be performed automatically as addresses are assigned sequentially by embedding that information into the 7-, 9-, and 10-digit decimal FLEX address.

The standard procedure for deriving the phase and frame values from the CAPCODE starts by separating the 7-, 9-, or 10-digit decimal address portion (field to the right of the CAPCODE type) and performing a decimal-to-binary conversion. The least significant bit (LSB) is labeled bit 0. The following bits, 2 and 3 in order, specify phases 00, 01, 10, or 11 for phase 0,1,2,3 (a,b,c,d), and bits 4 through 10 represent frames 000 through 127.

The frame and phase can also be derived from the 7-, 9-, or 10-digit decimal address by using modulo arithmetic (base 10) where:

Phase = (Integer (Addr/4)) Modulo 4

Frame = (Integer (Addr/16)) Modulo 128

When these rules are used and addresses assigned in order, the phase increments after 4 consecutive addresses are assigned; the frame is incremented after 16 addresses are assigned.

2.9.3 CAPCODE Alpha Character Definition

The alpha character in the FLEX CAPCODE indicates the type of decoding device to which the address is assigned. Table 2–19 defines the alpha character codes. The types include single-phase, any-phase, or all-phase. It also indicates if the address is the first, second, third, or fourth address in the subscriber unit (when addresses are assigned in order following standard rules), and specifies the rules for determining in which phase and frame the address is active.

Table 2–19. Alpha Character Codes

Standard Rules	No Rules (Nonstandard Form)
A – Single-phase, subtract 0	U – Single-phase, phase 0
B – Single-phase, subtract 1	V – Single-phase, phase 1
C – Single-phase, subtract 2	W – Single-phase, phase 2
D – Single-phase, subtract 3	X – Single-phase, phase 3
E – Any-phase, subtract 0	Y – Any-phase
F – Any-phase, subtract 1	
G – Any-phase, subtract 2	
H – Any-phase, subtract 3	
I – All-phase, subtract 0	Z – All-phase
J – All-phase, subtract 1	
K – All-phase, subtract 2	
L – All-phase, subtract 3	

The character A represents a single-phase subscriber unit using the standard rules for embedding phase and frame. The character B is similar to A except 1 is subtracted from the CAPCODE before the standard rule is applied. Likewise, the characters C and D indicate that 2 or 3 is to be subtracted before the rule is applied. Using these CAPCODE characters ensures that sequentially numbered CAPCODEs are assigned to a common phase and frame. These procedures modify the standard rules and are intended to simplify the order entry process for multiple address subscriber units. When addresses are assigned in order, the subtraction of 1, 2, or 3 ensures that the calculation for each additional address in a decoding device is referenced to the first address. Thus, all A, B, C, and D addresses are assigned to the same frame and phase.

Characters E through H and I through L represent any-phase and all-phase subscriber units where the subtract rule is modified to ensure that all addresses of a multiple address subscriber unit are in the same frame.

For the cases where no rule is defined, the letters U through X indicate single-phase subscriber units assigned to phases 0 through 3 (phases A through D) with the frame and battery cycle explicitly displayed. Y and Z indicate nonstandard addresses for any-phase and all-phase subscriber units.

If the subscriber unit contains only a single individual address and you are content with the recommended 30-second battery cycle, then the letter A, E, or I is added as a prefix to the 7-, 9- or 10-digit address where:

A = Single-phase unit
E = Any-phase unit
I = All-phase unit

If the unit is a two-address unit where both addresses are individual addresses, then A,E, or I would preface the address field of the first address. The B, F, or J would preface the second address. The B, F, or J indicates that the address is a second address and it is to have the properties of the first address. This rule eliminates the need for an administrative operator or a salesperson to calculate a starting address, which would allow standard rules to always apply.

In other cases, especially when a group address is to be included, it is advisable to use the U through Z forms of the CAPCODE so that the frame can be explicitly chosen to provide best battery life, and the required *same phase* operation can be met in the case of the single-phase units.

2.9.4 CAPCODE to Binary Conversion

Short CAPCODE – To convert a short address CAPCODE, the number 32,768 is added to the 7-digit decimal CAPCODE address (or to any CAPCODE less than 2,031,615). The resultant number is then converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air.

Long CAPCODE 2,101,249 to 1,075,843,072 – Long address set 1–2 is in this range. To convert a long address CAPCODE, the number 2,068,481 is subtracted from the CAPCODE address. The resultant number is then divided by 32,768 with the remainder, incremented by 1, being the first word of the long address. This is the same as calculating the ((CAPCODE–2,068,481) modulo 32768) +1. This value is converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air as the first address word.

The second word of the long address is determined by first calculating the integer portion of the (CAPCODE–2,068,481) divided by 32,768. This value is then subtracted from 2,097,151 (equivalent to 1's complement of the value in binary), and converted to a 21-bit binary number, which becomes the information bits in the (31,21) BCH code word transmitted over the air as the second address word.

Long CAPCODE 1,075,843,073 to 3,223,326,720 – Long address sets 1–3 and 1–4 are in this range. The first word of the long address is calculated following the same rules for the long address sets 1–2. The second long address word is determined by subtracting 2,068,481 from the CAPCODE. The resultant number is divided by 32,768 with the integer portion added to 1,933,312. This value is converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air as the second address word.

Long CAPCODE 3,223,326,721 to 4,297,068,542 – Long address set 2–3 is in this range. The first word is determined by subtracting 2,068,479 from the CAPCODE. The resultant number is divided by 32,768 and is retained (Modulo 32,768). This value is then added to 2,064,383 with the result converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air as the first address word.

The second word of the long address is determined by subtracting 2,068,479 from the CAPCODE and finding the integer portion after dividing by 32,768. This value is then added to 1,867,776 and converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air as the second address word.

2.9.5 Binary to CAPCODE Conversion

With the address code word values that are transmitted over the air, the CAPCODE can be calculated by performing the inverse of the process specified previously. As an example, the short address code word is converted to decimal and the number 32,768 is subtracted to arrive at the 7-digit address portion of the CAPCODE. For the two-word long address set 1–2, the address word 1 is first converted from binary to decimal. The address word 2 is then complemented, (or subtracted from 2,097,151 decimal) and converted to a decimal. This value is multiplied by 32,768, added to 2,068,480 and then added to address word 1. The result is the address portion of the FLEX CAPCODE.

2.9.6 CAPCODE Assignments

Table 2–20 defines the address usage assignment. Addresses not listed in this table are not defined and not reserved for future use.

Table 2–20. CAPCODE Assignments

CAPCODE Address Value	Description
0,000,000,000	Illegal
0,000,000,001 to 0,001,933,312	Short Addresses
0,001,933,313 to 0,001,998,848	Illegal
0,001,998,849 to 0,002,009,087	Reserved for Future Use
0,002,009,088 to 0,002,025,471	Information Service Addresses
0,002,025,472 to 0,002,029,567	Network Addresses
0,002,029,568 to 0,002,029,583	Temporary Addresses
0,002,029,584 to 0,002,029,599	Operator Messaging Addresses
0,002,029,600 to 0,002,031,614	Reserved for Future Use
0,002,031,615 to 0,002,101,248	Illegal
0,002,101,249 to 0,102,101,250	Long Address Set 1–2 Uncoordinated
0,102,101,251 to 0,402,101,250	Long Address Set 1–2 by Country†
0,402,101,251 to 1,075,843,072	Long Address Set 1–2 Global‡
1,075,843,073 to 2,149,584,896	Long Address Set 1–3 Global‡
2,149,584,897 to 3,223,326,720	Long Address Set 1–4 Global‡
3,223,326,721 to 3,923,326,750	Long Address Set 2–3 by Country†
3,923,326,751 to 4,280,000,000	Long Address Set 2–3 Reserved
4,280,000,001 to 4,285,000,000	Long Address Set 2–3 Information Service§ Global‡
4,285,000,001 to 4,290,000,000	Long Address Set 2–3 Information Service§ by Country
4,290,000,001 to 4,291,000,000	Long Address Set 2–3 Information Service§ World-Wide Use¶
4,291,000,001 to 4,297,068,542	Reserved for Future Use

† By country: The addresses are coordinated within each country and with countries along borders.
‡ Global: Address is coordinated to be unique worldwide.
§ Information service: Rules governing the use of these addresses are not currently defined.
¶ Worldwide use: 1000 addresses are assigned to each country for worldwide use.

Chapter 3

TLV5593VF FLEX Decoder

The TLV5593VF FLEX™ decoder simplifies implementation of a FLEX paging device by interfacing with any of several off-the-shelf paging receivers and any of several off-the-shelf host microcontroller/microprocessors. Its primary function is to process information received and demodulated from a FLEX radio paging channel, select messages addressed to the paging device and communicate the message information to the host. The host's function is to interpret the message information in an appropriate manner (numeric, alphanumeric, binary, etc.). The FLEX decoder also operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low-power mode when message information for the paging device is not being received.

Topic **Page**

3.1 Features

- FLEX messaging protocol signal processor
- Decoding at 1600, 3200, or 6400 bits per second (bps)
- Real-time clock time base
- Low battery indication (external detector)
- Standard serial peripheral interface (SPI) in slave mode
- Highly programmable receiver control
- Compatible with synthesized receivers
- Low-current STOP mode operation of host processor
- 16 programmable user-address words
- 16 fixed temporary addresses
- 16 operator messaging addresses
- Any-phase or single-phase decoding
- FLEX fragmentation and group messaging support
- Real-time clock over-the-air update support
- Simulcast System Identifier (SSID) and Network ID (NID) roaming support
- 28 used pins (32-pin TQFP standard)
- Pin-compatible with all other FLEX decoder signal processors

3.1.1 Support

FLEX system software from Motorola™ is a family of software components for building world-class products incorporating messaging capabilities. FLEXstack™ roaming software is specifically designed to support the FLEX roaming decoder. FLEXstack roaming software runs on a product's host processor and takes care of communicating with the FLEX decoder and fully interpreting the code words that are passed to the host from the FLEX decoder.

The TLV5590, produced by Texas Instruments (TI), converts an audio signal from an off-the-shelf receiver to a two-bit digital output for processing by the FLEX decoder.

3.1.2 Functional Description

Figure 3–1 shows the FLEX decoder functional block diagram. The FLEX decoder connects to a receiver capable of converting a 4-level audio signal into a 2-bit digital signal. The FLEX decoder has eight receiver control lines used to warm up and shut down a receiver in stages. The FLEX decoder has dual bandwidth control signals for two post-detection filter bandwidths to receive the two symbol rates of the FLEX signal. The FLEX decoder can detect a low battery signal during the receiver control sequences. It interfaces to a host microcontroller unit (MCU) through a standard SPI. It has a 38.4-kHz clock output capable of driving other devices. It has a one-minute timer that offers low-power support for time of day function on the host.

Figure 3–1. Functional Block Diagram

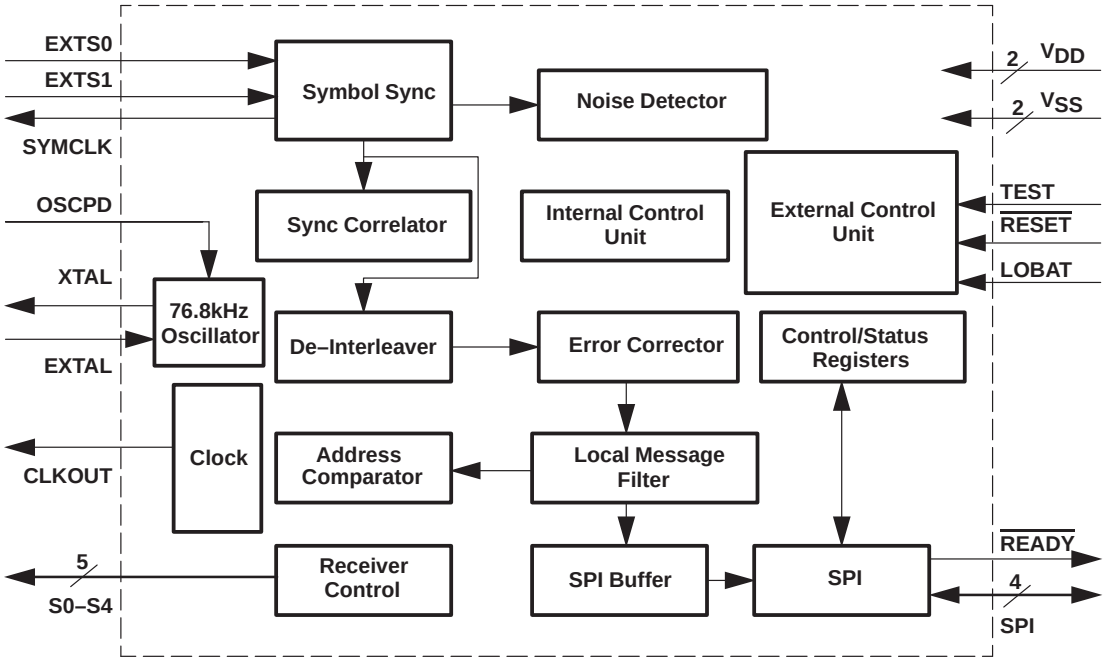
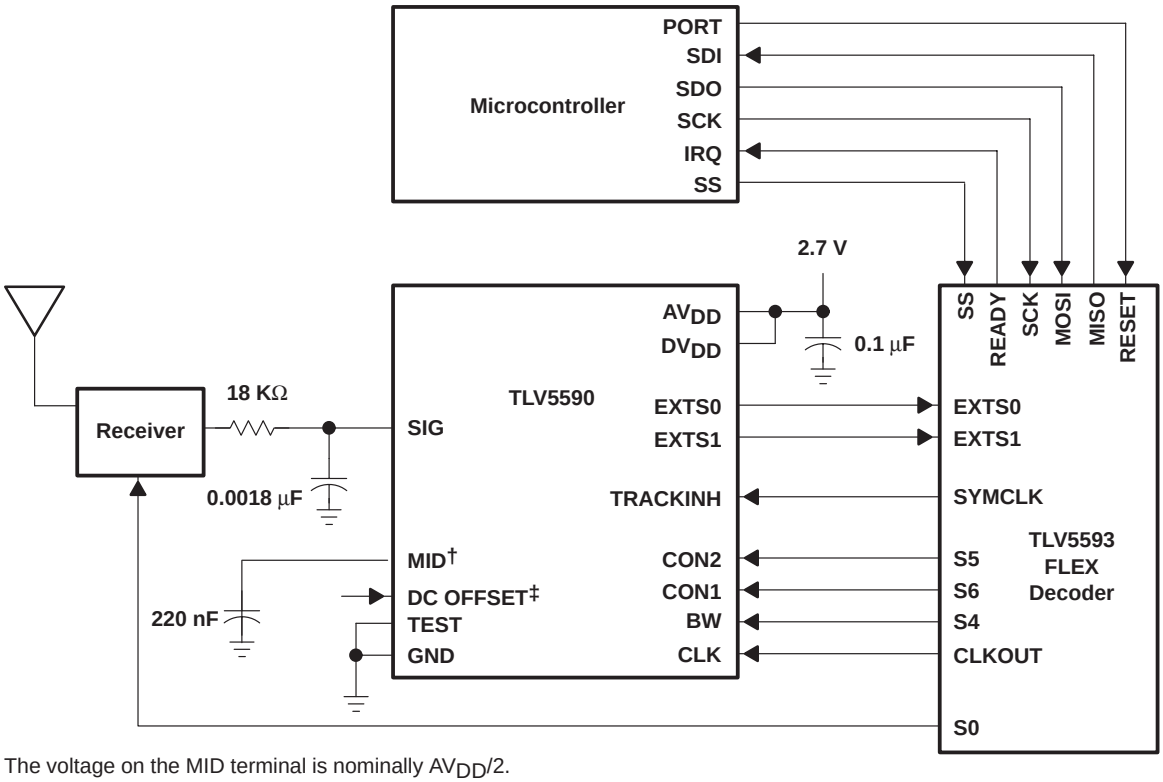


Figure 3–2 shows a system diagram of the FLEX decoder.

Figure 3–2. System Diagram



† The voltage on the MID terminal is nominally $AV_{DD}/2$.
‡ The voltage applied to the DC OFFSET terminal is set to the dc offset voltage of the input signal applied to the SIG terminal.

3.1.3 Powerdown

To ensure proper operation, the FLEX decoder must be in asynchronous mode when turned off.

The FLEXstack one-way API (application programming interface) has been modified to ensure that the FLEX decoder is in asynchronous mode when turned off. If you are using FLEXstack, be sure to download V1.2 or later, which is available as of 10/5/96.

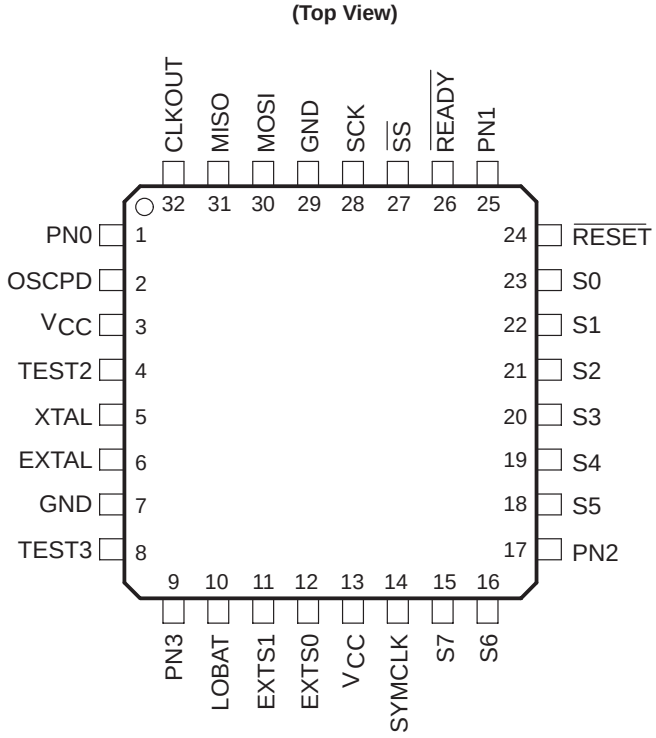
If you are not using FLEXstack, sending a Control Packet with the ON bit cleared does not guarantee the asynchronous mode. To ensure that you are in asynchronous mode, follow this sequence:

1) Turn off the FLEX decoder by sending a Control Packet with the ON bit cleared.
2) Turn on the FLEX decoder by sending a Control Packet with the ON bit set.
3) Turn off the FLEX decoder by sending a Control Packet with the ON bit cleared.

Timing between these steps is measured from the positive edge of the last clock of one packet to the positive edge of the last clock of the next packet. The minimum time between any of the steps should be 2 milliseconds. There is no maximum time between steps 1 and 2. The time between steps 2 and 3 should not exceed the programmed warm-up time or 95 milliseconds, whichever is smaller. The programmed warm-up time is the sum of the times programmed in the selected Receiver Warm-up Settings Packets.

Figure 3–3 shows terminal assignments for the FLEX decoder.

Figure 3–3. Terminal Assignments



3.1.4 Terminal Functions

Table 3–1 shows the terminal functions of the FLEX decoder.

Table 3–1. Terminal Functions

Terminal		I/O	Description
NAME	NO.		
CLKOUT	32	O	38.4-kHz clock output (derived from 76.8-kHz oscillator). May also be used to clock other functions of the pager circuitry.
EXTAL	6	I	76.8-kHz crystal oscillator input or external input
EXTS1	11	I	Most significant bit pair of the FLEX 4-level symbol currently being decoded
EXTS0	12	I	Least significant bit pair of the FLEX 4-level symbol currently being decoded
LOBAT	10	I	Used to test a low battery voltage input signal
MISO	31	O	3-state data output for SPI communications
MOSI	30	I	Data input for SPI communications
OSCPD	2	I	Internal oscillator powerdown Connected to VSS when using internal oscillator Connected to VDD when using an external source
$\overline{\text{READY}}$	26	O	Driven low when the TLV5593VF is ready for an SPI packet
$\overline{\text{RESET}}$	24	I	Active low reset to the TLV5593VF
S0	23	O	Eight 3-state receiver control ports
S1	22	O	
S2	21	O	
S3	20	O	
S4	19	O	
S5	18	O	
S6	17	O	
S7	16	O	
SCK	28	I	Serial clock. Used to clock synchronous data for SPI communications.
$\overline{\text{SS}}$	27	I	Active low slave select. Used to select the TLV5593VF decoder SPI for data transfer.
SYMCLK	14	O	Recovery symbol clock
TEST2	4	I	Manufacturing test mode terminals. During normal operation, the TEST terminals are connected to VSS.
TEST3	8	I	Manufacturing test mode terminals. During normal operation, the TEST terminals are connected to VSS.
VDD	3, 13	Power	Supply voltage
VSS	7, 29	Ground	Ground
XTAL	5	O	76.8-kHz clock output

Note: Pin numbers shown are for 32-pin TQFP devices.

3.2 SPI Packets

All data communicated between the FLEX decoder and the host MCU is transmitted on the SPI in 32-bit packets. Each packet consists of an 8-bit ID followed by 24 bits of information. The FLEX decoder uses the SPI bus in full duplex mode. In other words, whenever a packet communication occurs, the data in both directions is valid packet data.

The SPI interface consists of a $\overline{\text{READY}}$ pin and four SPI pins ($\overline{\text{SS}}$, SCK, MOSI, and MISO).The $\overline{\text{SS}}$ is used as a chip select for the FLEX decoder. The SCK is a clock supplied by the host MCU. The data from the host is transmitted on the MOSI line. The data from the FLEX decoder is transmitted on the MISO line.

3.2.1 Packet Communication Initiated by the Host

When the host sends a packet to the FLEX decoder, it performs the following steps (see Figure 3–4):

1) Selects the FLEX decoder by driving the $\overline{\text{SS}}$ pin low.

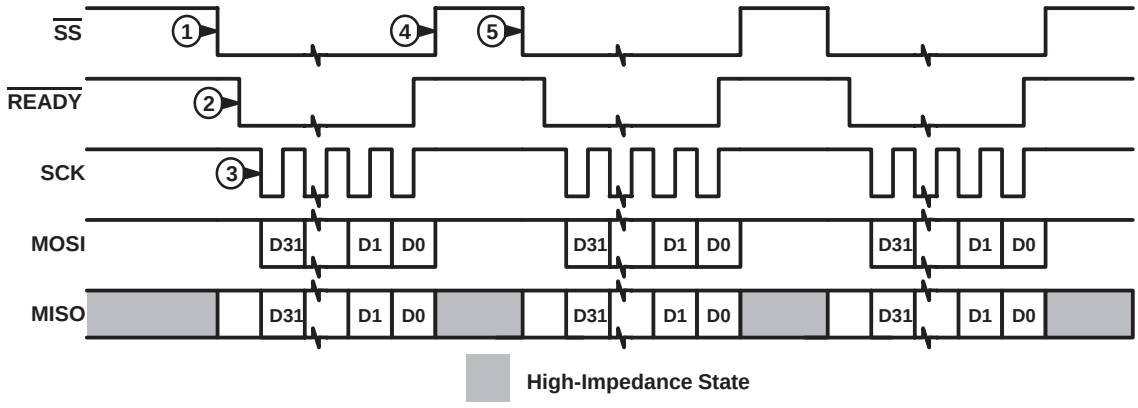
2) Waits for the FLEX decoder to drive the $\overline{\text{READY}}$ pin low.

3) Sends the 32-bit packet.

4) Deselects the FLEX decoder by driving the $\overline{\text{SS}}$ pin high.

5) Repeats steps 1 through 4 for each additional packet.

Figure 3–4. Typical Multiple Packet Communications Initiated by the Host



When the host sends a packet, it also receives a valid packet from the FLEX decoder. If the FLEX decoder is enabled (see subsection 3.3.1, *Checksum Packet*) and has no other packets waiting to be sent, the decoder will send a status packet.

The host must transition the $\overline{\text{SS}}$ pin from high to low to begin each 32-bit packet. The FLEX decoder must see a negative transition on the $\overline{\text{SS}}$ pin in order for the host to initiate each packet communication.

3.2.2 Packet Communication Initiated by the FLEX Decoder

When the FLEX decoder has a packet for the host to read, the following events occur (see Figure 3–5):

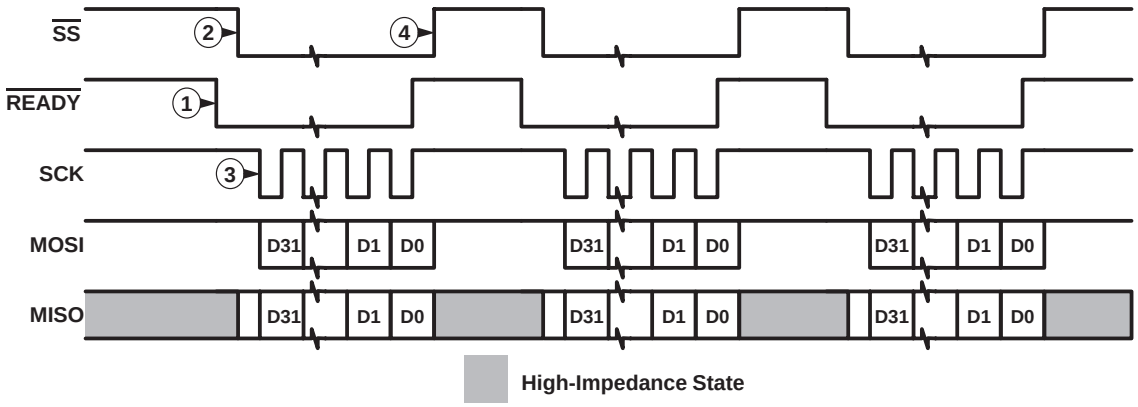
1) The FLEX decoder drives the $\overline{\text{READY}}$ pin low.

2) If the FLEX decoder is not already selected, the host selects the FLEX decoder by driving the $\overline{\text{SS}}$ pin low.

3) The host receives (and sends) a 32-bit packet.

4) The host deselects the FLEX decoder by driving the $\overline{\text{SS}}$ pin high (optional).

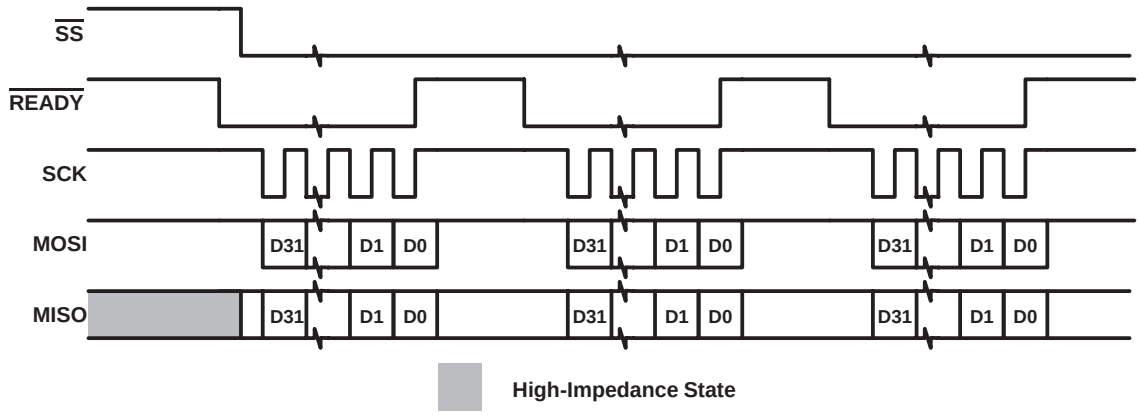
Figure 3–5. Typical Multiple Packet Communications Initiated by the FLEX Decoder



When the host reads a packet from the FLEX decoder, it must send a valid packet to the FLEX decoder. If the host has no data to send, TI suggests that the host send a checksum packet with all of the data bits set to 0 to avoid disabling the FLEX decoder (see subsection 3.3.1, *Checksum Packet*).

Figure 3–6 illustrates that it is not necessary to deselect the FLEX decoder between packets when the packets are initiated by the FLEX decoder.

Figure 3–6. Multiple Packet Communications Initiated by the FLEX Decoder With No Deselect



3.2.3 Host-To-Decoder Packet Map

The upper 8 bits of a packet comprise the packet ID. Table 3–2 describes the packet IDs for all of the packets that can be sent to the FLEX decoder from the host.

Table 3–2. Host-To-Decoder Packet ID Map

Packet ID (Hexadecimal)	Packet Type
00	Checksum
01	Configuration
02	Control
03	All frame mode
04	Operator message address enable
05	Roaming control packet
06	Timing control packet
07 – 0E	Reserved (host should never send)
0F	Receiver line control
10	Receiver control configuration (off setting)
11	Receiver control configuration (warm up 1 setting)
12	Receiver control configuration (warm up 2 setting)
13	Receiver control configuration (warm up 3 setting)
14	Receiver control configuration (warm up 4 setting)
15	Receiver control configuration (warm up 5 setting)
16	Receiver control configuration (3200 sps sync setting)
17	Receiver control configuration (1600 sps sync setting)
18	Receiver control configuration (3200 sps data setting)
19	Receiver control configuration (1600 sps data setting)
1A	Receiver control configuration (shutdown 1 setting)
1B	Receiver control configuration (shutdown 2 setting)
1C – 1F	Special (ignored by FLEX decoder)
20	Frame assignment (frames 112 through 127)
21	Frame assignment (frames 96 through 111)
22	Frame assignment (frames 80 through 95)
23	Frame assignment (frames 64 through 79)
24	Frame assignment (frames 48 through 63)
25	Frame assignment (frames 32 through 47)
26	Frame assignment (frames 16 through 31)
27	Frame assignment (frames 0 through 15)
28 – 77	Reserved (host should never send)
78	User address enable
79 – 7F	Reserved (host should never send)

Table 3–2. Host-To-Decoder Packet ID Map (Continued)

Packet ID (Hexadecimal)	Packet Type
80	User address assignment (user address 0)
81	User address assignment (user address 1)
82	User address assignment (user address 2)
83	User address assignment (user address 3)
84	User address assignment (user address 4)
85	User address assignment (user address 5)
86	User address assignment (user address 6)
87	User address assignment (user address 7)
88	User address assignment (user address 8)
89	User address assignment (user address 9)
8A	User address assignment (user address 10)
8B	User address assignment (user address 11)
8C	User address assignment (user address 12)
8D	User address assignment (user address 13)
8E	User address assignment (user address 14)
8F	User address assignment (user address 15)
90 – FF	Reserved (host should never send)

3.2.4 Decoder-To-Host Packet Map

Table 3–3 describes the packet IDs for all of the packets that can be sent to the host from the FLEX decoder.

Table 3–3. Decoder-To-Host Packet ID Map

Packet ID (Hexadecimal)	Packet Type
00	Block Information Word (BIW)
01	Address
02 – 57	Vector or Message (ID is word number in frame)
58 – 5F	Reserved
60	Roaming Status Packet
61 – 7D	Reserved
7E	Receiver Shutdown
7F	Status
80 – FE	Reserved
FF	Part ID

3.3 Host-To-Decoder Packet Descriptions

The following sections describe the packets of information sent from the host to the FLEX decoder. In all cases the packets should be sent most significant bit (MSB) first (bit 7 of byte 3 = bit 31 of the packet = MSB).

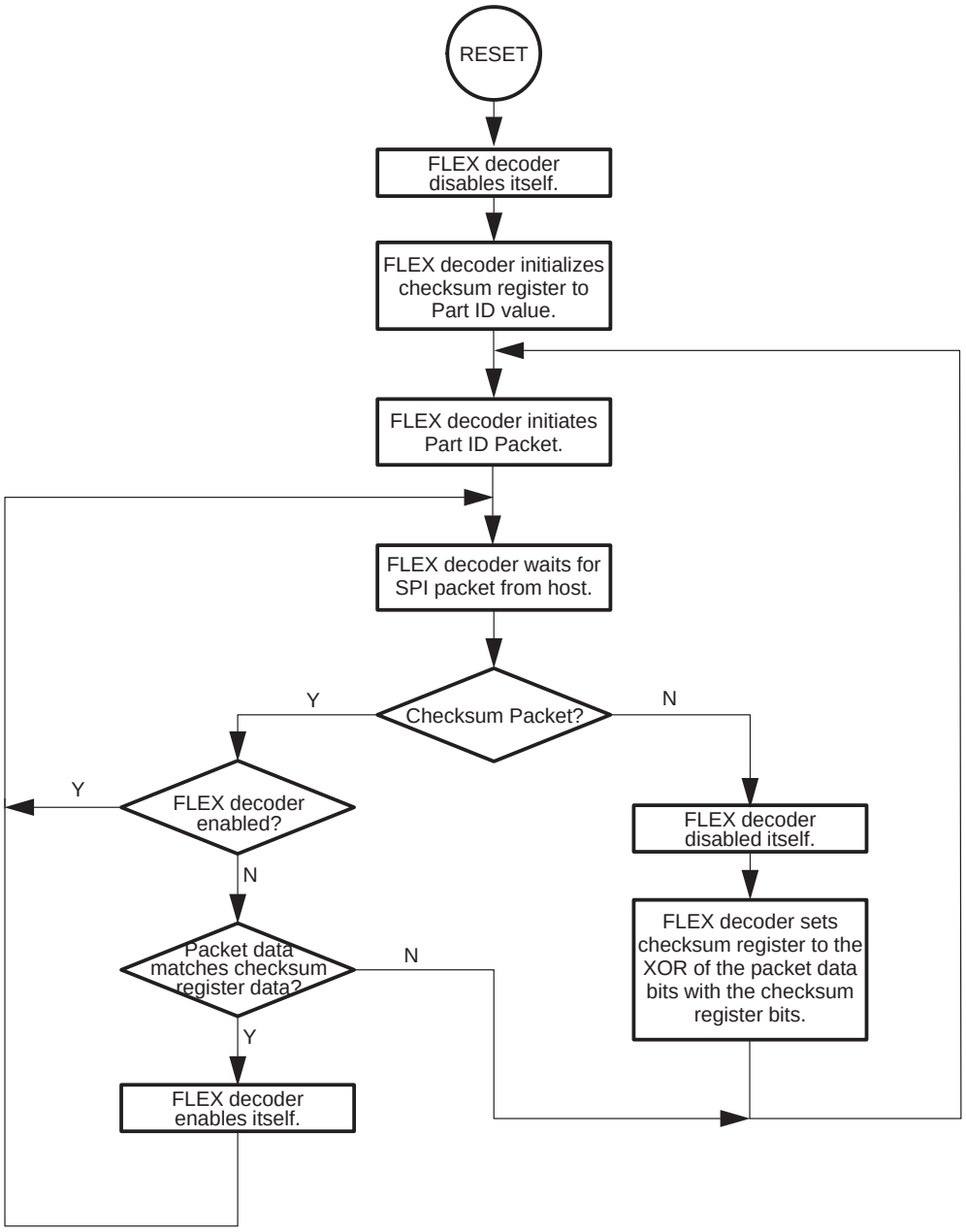
3.3.1 Checksum Packet

The Checksum Packet ensures proper communication between the host and the FLEX decoder. The FLEX decoder exclusive-ORs the 24 data bits of every packet it receives (except the Checksum Packet and the special packet IDs, 1C through 1F hexadecimal) with an internal checksum register. Upon reset and whenever the host writes a packet to the FLEX decoder, the FLEX decoder is disabled from sending any information to the host processor until the host processor sends a Checksum Packet with the proper checksum value (CV) to the FLEX decoder. When the FLEX decoder is disabled in this way, it prompts the host to read the Part ID Packet. Note that all other operation continues normally when the FLEX decoder is disabled. The FLEX decoder is only disabled in the sense that the data from the FLEX decoder cannot be read; all other operations continue to function.

When the FLEX decoder is reset, it is disabled and the internal checksum register is initialized to the 24-bit part ID defined in the Part ID Packet (see subsection 3.4.8, *Part ID Packet*). Every time a packet (other than the Checksum Packet and the special packets 1C through 1F) is sent to the decoder, the value sent in the 24 information bits is exclusive-ORed with the internal checksum register, the result is stored back to the checksum register, and the FLEX decoder is disabled. If a Checksum Packet is sent and the CV bits match the bits in the checksum register, the FLEX decoder is enabled. If a Checksum Packet is sent when the FLEX decoder is already enabled, the packet is ignored by the FLEX decoder and a null packet with the ID and data bits set to 0 is suggested. If a packet other than the Checksum Packet is sent when the FLEX decoder is enabled, the decoder is disabled until a Checksum Packet is sent with the correct CV bits.

Figure 3–7 shows the FLEX decoder checksum flow chart.

Figure 3–7. FLEX Decoder Checksum Flow Chart



When the host reads a packet out of the FLEX decoder but has no data to send, the Checksum Packet (see Table 3–4) should be sent so the FLEX decoder is not disabled. The data in the Checksum Packet could be a null packet, 32-bit stream of all zeros, because a Checksum Packet does not disable the FLEX decoder. When the host reconfigures the FLEX decoder, the FLEX decoder is disabled from sending any packets other than the Part ID Packet until the FLEX decoder is enabled with a Checksum Packet having the proper data. The ID of the Checksum Packet is 0.

Table 3–4. Checksum Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	0
Byte 2	CV_{23}	CV_{22}	CV_{21}	CV_{20}	CV_{19}	CV_{18}	CV_{17}	CV_{16}
Byte 1	CV_{15}	CV_{14}	CV_{13}	CV_{12}	CV_{11}	CV_{10}	CV_9	CV_8
Byte 0	CV_7	CV_6	CV_5	CV_4	CV_3	CV_2	CV_1	CV_0

CV: Checksum Value.

3.3.2 Configuration Packet

The Configuration Packet (see Table 3–5) defines a number of different configuration options for the FLEX decoder. To ensure proper operation, do not change these settings when decoding is enabled (i.e., the ON bit in the Control Packet is set). The ID of the Configuration Packet is 1.

Table 3–5. Configuration Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	1
Byte 2	0	0	0	0	0	0	OFD_1	OFD_0
Byte 1	0	0	0	0	0	0	SP_1	SP_0
Byte 0	SME	MOT	COD	MTE	LBP	0	0	0

OFD: Oscillator Frequency Difference (see Table 3–6). These bits describe the maximum difference in the frequency of the 76.8-kHz oscillator crystal with respect to the frequency of the transmitter. These limits should be the worst-case difference in frequency due to all conditions including but not limited to aging, temperature, and manufacturing tolerance. Using a smaller frequency difference in this packet results in lower power consumption due to higher receiver battery save ratios. Note that this value is not the absolute error of the oscillator frequency provided to the FLEX decoder. The absolute error of the clock used by the FLEX transmitter must be taken into account. (e.g., If the transmitter tolerance is +/–25 ppm and the 76.8-KHz oscillator tolerance is +/–140 ppm, the oscillator frequency difference is +/–165 ppm and OFD should be set to 0.)(value after reset = 0)

Table 3–6. Oscillator Frequency Difference

OFD_1	OFD_0	Frequency Difference
0	0	+/– 300 ppm
0	1	+/– 150 ppm
1	0	+/– 75 ppm
1	1	+/– 0 ppm

SP: Signal Polarity (Table 3–7). These bits set the polarity of EXTS1 and EXTS0 input signals. (value after reset = 0) The polarity of the EXTS0 and EXTS1 bits are determined by the receiver design.

Table 3–7. Signal Polarity

SP_1	SP_0	Signal Polarity EXTS1	EXTS0		FSK Modulation @ SP = 0,0	EXTS1	EXTS0
0	0	Normal	Normal		+ 4800 Hz	1	0
0	1	Normal	Inverted		+1600 Hz	1	1
1	0	Inverted	Normal		– 1600 Hz	0	1
1	1	Inverted	Inverted		– 4800 Hz	0	0

SME: Synchronous Mode Enable. When this bit is set, a Status Packet is automatically sent whenever the SMU (synchronous mode update) bit in the Status Packet is set. The host can use the SM (synchronous mode) bit in the Status Packet as an in-range/out-of-range indication. (value after reset = 0)

MOT: Maximum Off Time. This bit has no effect if AST in the Timing Control Packet is non-zero. When AST = 0 and MOT = 0, asynchronous A-word searches time out in 4 minutes. When AST = 0 and MOT = 1, asynchronous A-word searches time out in 1 minute. (value after reset = 0)

COD: Clock Output Disable. When this bit is clear, a 38.4-kHz signal is output on the CLKOUT pin. When this bit is set, the CLKOUT pin is driven low. Note that setting and clearing this bit can cause pulses on the CLKOUT pin that are less than one half the 38.4-kHz period. Also note that when the clock output is enabled, the CLKOUT pin always outputs the 38.4-kHz signal even when the FLEX decoder is in reset (as long as the FLEX decoder oscillator is recognizing clocks). (value after reset = 0)

MTE: Minute Timer Enable. When this bit is set, a Status Packet is sent at one-minute intervals with the minute time-out (MT) bit in the Status Packet set. When this bit is clear, the internal one-minute timer stops counting. The internal one-minute timer is reset when this bit is changed from 0 to 1 or when the minute timer clear (MTC) bit in the Control Packet is set. (value after reset = 0)

LBP: Low Battery Polarity. This bit defines the polarity of the FLEX decoder LOBAT pin. The low battery (LB) bit in the Status Packet is initialized to the inverse value of this bit when the FLEX decoder is turned on (by setting the ON bit in the Control Packet). When the FLEX decoder is turned on, the first low battery update in the Status Packet is sent to the host when a low battery condition is detected on the LOBAT pin. Setting this bit means that a high on the LOBAT pin indicates a low-voltage condition. (value after reset = 0)

3.3.3 Control Packet

The Control Packet defines a number of different control bits for the FLEX decoder (see Table 3–8). The ID of the Control Packet is 2.

Table 3–8. Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	1	0
Byte 2	FF_7	FF_6	FF_5	FF_4	FF_3	FF_2	FF_1	FF_0
Byte 1	0	SPM	PS_1	PS_0	0	0	0	0
Byte 0	0	SBI	0	MTC	0	0	EAE	ON

FF: Force Frame 0–7. These bits enable and disable, forcing the FLEX decoder to look in frames 0 through 7. When an FF bit is set, the FLEX decoder decodes the corresponding frame. Unlike the AF bits in the Frame Assignment Packets, the system collapse of a FLEX system does not affect frames assigned using the FF bits (e.g., whereas, setting AF_0 to 1 when the system collapse is 5 causes the decoder to decode frames 0, 32, 64, and 96; setting FF_0 to 1 when the system collapse is 5 only causes the decoder to decode frame 0). This may be useful for acquiring transmitted time information. (value after reset = 0)

SPM: Single-Phase Mode. When this bit is set, the FLEX decoder decodes only one phase of the transmitted data. When this bit is clear, the FLEX decoder decodes all of the phases it receives. A change to this bit while the FLEX decoder is on does not take effect until the next block 0 of a frame. (value after reset = 0)

PS: Phase Select. When the SPM bit is set, these bits define what phase the FLEX decoder should decode, as shown in Table 3–9. This value is determined by the service provider. A change to these bits while the FLEX decoder is on does not take effect until the next block 0 of a frame. (value after reset = 0)

Table 3–9. Phase Select

PS Value		Phase Decoded (based on FLEX Data Rate)		
PS_1	PS_0	1600bps	3200bps	6400bps
0	0	a	a	a
0	1	a	a	b
1	0	a	c	c
1	1	a	c	d

SBI: Send Block Information words 2 – 4. When this bit is set, any errors or time-related block information words 2–4 are sent to the host. (value after reset = 0)

MTC: Minute Timer Clear. Setting this bit causes the one-minute timer to restart from 0.

EAE: End of Address Enable. When this bit is set, the EA bit in the Status Packet is set immediately after the FLEX decoder decodes the last address word in the frame (if there was an address detected in the frame). When this bit is cleared, the EA bit is never set.

ON: Turn On Decoder. Set this bit if the FLEX decoder should be decoding FLEX signals. Clear if signal processing should be off (very-low power mode). If the ON bit is changed twice and the control packets making the changes are received within 2 ms of each other, the FLEX decoder may ignore the double change and stay in its original state (e.g., if it is turned off and on again within 2 ms, it may stay on and ignore the off pulse). Therefore, TI recommends that the host ensure a minimum of 2 ms between changes in the ON bit. (value after reset = 0)

Note:

To properly turn off the decoder, the following steps must occur:

1) Turn off the FLEX decoder by sending a Control Packet with the ON bit cleared.
2) Turn on the FLEX decoder by sending a Control Packet with the ON bit set.
3) Turn off the FLEX decoder by sending a Control Packet with the ON bit cleared.

Timing between these steps is specified below and is measured from the positive edge of the last clock of one packet to the positive edge of the last clock of the next packet:

- ❑ The minimum time between steps 1 and 2 is 2 ms or the programmed shutdown time, whichever is greater. The programmed shutdown time is the sum of all the times programmed in the used Receiver Shutdown Settings Packet.
- ❑ There is no maximum time between steps 1 and 2.
- ❑ The minimum time between steps 2 and 3 is 2 ms.
- ❑ The maximum time between steps 2 and 3 is the programmed warm-up time minus 2 ms. The programmed warm-up time is the sum of all the times programmed in the used Receiver Warm Up Settings Packet.

See subsection 3.1.3, *Powerdown*, for more information on the powerdown cycle.

3.3.4 All Frame Mode Packet

The All Frame Mode Packet (see Table 3–10) is used to decrement temporary address enable counters by one, decrement the all frame mode counter by one, and/or enable or disable the forcing of all frame mode. If all frame mode is enabled, the FLEX decoder attempts to decode every frame and sends a Status Packet with the EOF (end-of-frame) bit set at the end of every frame. All frame mode is enabled if any temporary address enable counter is non-zero OR if the all frame mode counter is non-zero OR if the force all frame mode bit is set. Both the all frame mode counter and the temporary address enable counters can only be incremented internally by the FLEX decoder and can only be decremented by the host. The FLEX decoder increments a temporary address enable counter whenever a short instruction vector is received assigning the corresponding temporary address. The FLEX decoder increments the all frame mode counter whenever an Alphanumeric, Hex/Binary, or Secure Vector is received. When the host determines that a message associated with a temporary address or a fragmented message has ended, the appropriate temporary address counter or all frame mode counter should be decremented by writing an All Frame Mode Packet to the FLEX decoder to exit the all frame mode, thereby improving battery life. See Section 3.8, *Building a Fragmented Message,* for details. Neither the temporary address enable counters nor the all frame mode counter can be incremented past the value 127 (i.e., it does not roll over) or decremented past the value 0. The temporary address enable counters and the all frame mode counter are initialized to 0 at reset and when the decoder is turned off. The ID of the All Frame Mode Packet is 3.

Table 3–10. All Frame Mode Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	1	1
Byte 2	DAF	FAF	0	0	0	0	0	0
Byte 1	DTA_{15}	DTA_{14}	DTA_{13}	DTA_{12}	DTA_{11}	DTA_{10}	DTA_{9}	DTA_{8}
Byte 0	DTA_{7}	DTA_{6}	DTA_{5}	DTA_{4}	DTA_{3}	DTA_{2}	DTA_{1}	DTA_{0}

DAF: Decrement All Frame counter. Setting this bit decrements the all frame mode counter by one. If a packet is sent with this bit clear, the all frame mode counter is not affected. (value after reset = 0)

FAF: Force All Frame mode. Setting this bit forces the FLEX decoder to enter all frame mode. If this bit is clear, the FLEX decoder may or may not be in all frame mode, depending on the status of the all frame mode counter and the temporary address enable counters. This may be useful in acquiring transmitted time information. (value after reset = 0)

DTA: Decrement Temporary Address enable counter. When a bit in this word is set, the corresponding temporary address enable counter is decremented by one. When a bit is cleared, the corresponding temporary address enable counter is not affected. When a temporary address enable counter reaches zero, the temporary address is disabled.(value after reset = 0)

3.3.5 Operator Messaging Address Enable Packet

The operator messaging address enable packet is used to enable and disable the built-in FLEX operator messaging addresses. Enabling and disabling operator messaging addresses does not affect what frames the decoder IC decodes. To decode the proper frames, the host must modify the FF bits in the Control Packet or the AF bits in the Frame Assignment Packets. The ID of the operator messaging address enable packet is 4.

Table 3–11. System Address Enable Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	1	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	OAE_{15}	OAE_{14}	OAE_{13}	OAE_{12}	OAE_{11}	OAE_{10}	OAE_{9}	OAE_{8}
Byte 0	OAE_{7}	OAE_{6}	OAE_{5}	OAE_{4}	OAE_{3}	OAE_{2}	OAE_{1}	OAE_{0}

OAE: Operator messaging Address Enable. When a bit is set, the corresponding operator messaging address is enabled. When it is cleared, the corresponding operator messaging address is disabled. OAE_0 through OAE_{15} corresponds to the hexadecimal operator messaging address values of 1F7810 through 1F781F, respectively. (value after reset=0)

3.3.6 Roaming Control Packet

The roaming control packet controls the features of the Roaming FLEX decoder that allow implementation of a roaming device. The ID of the roaming control packet is 5.

Table 3–12. Roaming Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	1	0	1
Byte 2	IRS	NBC	MCM	IS1	SDF	RSP	SND	CND
Byte 1	RND	ABI	SAS	DAS	0	0	0	0
Byte 0	0	0	MFC_1	MFC_0	0	0	MCO1	MCO_0

IRS: Ignore Resynchronization Signal. When this bit is set, the FLEX decoder does not go asynchronous when detecting an Ar or $\overline{Ar}$ signal during searches for A-words. It reports that the resynchronization signal was received by setting RSR to 1 in the Roaming Status Packet. This allows the host to decide what to do when the paging device is synchronous to more than one channel and only one channel is sending the resynchronization signal. It also prevents the FLEX decoder from losing synchronization when it detects the resynchronization signal while the paging device is checking an unknown channel. This bit is set and cleared by the host. (value after reset=0)

NBC: Network Bit Check. Setting this bit enables reporting the received network bit value (NBU and n) in the Roaming Status Packet. Setting this bit also makes the FLEX decoder abandon a frame after the Frame Information Word without synchronizing to the frame if the Frame Information Word is uncorrectable or if the n bit in the Frame Information Word is not set. If the FLEX decoder was in synchronous mode when this occurred (probably due to synchronizing to a second channel), it maintains synchronization with the original channel. If the FLEX decoder was in asynchronous mode when this occurred, it stays in asynchronous mode and ends the A-word search. This is done to avoid synchronizing to a nonroaming channel when searching for roaming channels. This bit is set and cleared by the host. (value after reset=0)

MCM: Manual Collapse Mode. When this bit is set, the FLEX decoder behaves as if the system collapse was 7. The FLEX decoder does not apply the received system collapse to the AF bits. When this bit is set, the received system collapse is reported to the host via SCU and RSC in the Roaming Status Packet so the host can modify the AF bits based on the system collapse of the channel. This bit is set and cleared by the host. (value after reset=0)

IS1: Invert EXTS1. Setting this bit inverts the expected polarity of the EXTS1 pin from the way it is configured by SP_1 in the Configuration Packet (e.g., if both IS1 and SP_1 are set, the polarity of the EXTS1 pin is untouched). This bit must be changed when a change in a channel changes the polarity of the received signal. This bit is set and cleared by the host. (value after reset=0)

SDF: Stop Decoding Frame. Setting this bit causes the FLEX decoder to stop decoding a frame without losing frame synchronization. This bit is set by the host, and cleared by FLEX decoder when it has been processed. The packet with the SDF bit must be sent after receiving the status packet with EA bit set. It must be sent within 40 ms of the end of block in which FLEX decoder sets the EA bit. (value after reset=0)

RSP: Receiver Shutdown Packet enable. When this bit is set, a Receiver Shutdown Packet is sent whenever the receiver is shut down. The Receiver Shutdown Packet informs the host of the receiver shutdown and the amount of time needed for the FLEX decoder to automatically warm up the receiver again. (value after reset=0)

SND: Start Noise Detect. Setting this bit while the FLEX decoder is battery saving causes it to warm up the receiver, run noise detection, and report the result of the noise detection via NDR in the Roaming Status Packet. This bit is set by the host and cleared by the FLEX decoder when it has been processed. If the time comes for the FLEX decoder to warm up automatically, or if the SAS bit is set while an SND is being processed, the noise detection is abandoned and the abandoned noise detection result (NDR = 01) is sent in the Roaming Status Packet. (value after reset=0)

CND: Continuous Noise Detect. Setting this bit causes the FLEX decoder to do continuous noise detections during the decoded block data of a frame. The results of the noise detections are reported only if noise is detected (NDR = 11). Only one noise detection (NDR =11) is sent per block. If the FLEX decoder has not completed a noise detection when it shuts down for the frame, the noise detection in progress is abandoned, but no abandon result (NDR = 01) is sent. This bit is set and cleared by the host. (value after reset=0)

RND: Report Noise Detects. Setting this bit causes the FLEX decoder to report the results of the noise detections that it performs under normal asynchronous operation (when first turned on and when asynchronous). The results of the noise detection are reported via NDR in the Roaming Status Packet. This bit is set and cleared by the host. (value after reset=0)

ABI: All Block Information Words. When this bit is set, the FLEX decoder sends all received Block Information Words 2–4 to the host. Note that setting the SBI bit in the Control Packet only enables error and real-time clock-related block information words. (value after reset=0)

SAS: Start A-word Search. Setting this bit while in asynchronous battery save mode causes the FLEX decoder to warm up the receiver, and run an A-word search. If, during the A-word search, the FLEX decoder finds sufficient FLEX signal, it enters synchronous mode and starts decoding the frame. If the A-word search times out without finding sufficient FLEX signal, it battery-saves and continues doing periodic noise detections. The time-out for the A-word search is controlled by the AST bits in the Timing Control Packet and the MOT bit in the Configuration Packet. The A-word search takes priority over noise detections. Therefore, if the FLEX decoder is performing an A-word search and the time comes to do automatic noise detection, the noise detection is not performed. This bit is set by the host and cleared by the FLEX decoder when it has been acted on. (value after reset=0)

DAS: Disable A-word Search. When this bit is set, an A-word search does not automatically occur after a noise detection in asynchronous mode finds the FLEX signal. This includes automatic noise detections and noise detections initiated by the host by setting SND. The FLEX decoder shuts down the receiver after the noise detection finishes, regardless of the result. When this bit is cleared, an A-word search occurs after a noise detection finds the signal in asynchronous mode. (value after reset=0)

MFC: Missed Frame Control. These bits control the frames for which missing frame data (MS1, MFI, MS2, MBI, and MAW) is reported (see Table 3–13) in the Roaming Status Packet. (value after reset=0)

Table 3–13. Missing Frame Data

MFC_1	MFC_0	Missing Frame Data Reported
0	0	Never
0	1	Only during frames 0 through 3
1	0	Only during frames 0 through 7
1	1	Always

MCO: Maximum Carry On. The value of these bits sets the maximum carry on that the FLEX decoder follows. For example, if the FLEX decoder receives a carry on of 3 over the air and MCO is set to 1, the FLEX decoder only carries on for one frame. (value after reset=3)

3.3.7 Timing Control Packet

The timing control packet gives the host control of the timing used when FLEX decoder is in asynchronous mode (see Table 3–14). The packet ID for the timing control packet is 6.

Table 3–14. Timing Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	1	1	0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	AST_7	AST_6	AST_5	AST_4	AST_3	AST_2	AST1	AST_0
Byte 0	ABT_7	ABT_6	ABT_5	ABT_4	ABT_3	ABT_2	ABT1	ABT_0

AST: A-word Search Time. The value of these bits sets the A-word search time for all asynchronous A-word searches in units of 8 0ms (e.g., the value of 1 is 80 ms, the value of 2 is 160 ms, etc.) If the value is 0, the FLEX decoder defaults to the 1-minute (MOT = 1) or 4-minute (MOT = 0) A-word search time, which is controlled by the MOT bit in the configuration packet. (value after reset=0)

ABT: Asynchronous Battery-Save Time. The value of these bits sets the battery save time (time from the beginning of one automatic noise detection to the beginning of the next automatic noise detection) in asynchronous mode in units of 80 ms (e.g., the value of 1 is 80 ms, the value of 2 is 160 ms, etc.) If the value is 0, the battery save time is set to the default value of 1.5 seconds. The minimum allowed ABT is 320 ms; therefore, values 1, 2, 3, and 4 are invalid. (value after reset=0)

3.3.8 Receiver Line Control Packet

The Receiver Line Control Packet (see Table 3–15) gives the host control over the settings on the receiver control lines (S0–S7) in all modes except reset. In reset, the receiver control lines are in high-impedance settings. The ID for the Receiver Line Control Packet is 15 (decimal).

Table 3–15. Receiver Line Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	1	1	1	1
Byte 2	0	0	0	0	0	0	0	0
Byte 1	FRS_7	FRS_6	FRS_5	FRS_4	FRS_3	FRS_2	FRS_1	FRS_0
Byte 0	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0

FRS: Force Receiver Setting. Setting this bit to 1 causes the corresponding CLS bit in this packet to override the internal receiver control settings on the corresponding receiver control line (S0–S7). Clearing a bit gives control of the corresponding receiver control lines (S0–S7) back to the FLEX decoder. (value after reset = 0)

CLS: Control Line Setting. If the corresponding FRS bit is set in this packet, these bits define what setting should be applied to the corresponding receiver control lines. (value after reset = 0)

3.3.9 Receiver Control Configuration Packets

Receiver Control Configuration Packets allow the host to configure (1) what setting is applied to the receiver control lines S0–S7, (2) how long to apply the setting, and (3) when to read the value of the LOBAT input pin. For a more detailed description of how the FLEX decoder uses these settings, see Section 3.6, *Receiver Control.* The FLEX decoder defines 12 different receiver control settings. The FLEX decoder ignores these packets when decoding is enabled (i.e., the ON bit in the Control Packet is set). The IDs for these packets range from 16 to 27 (decimal).

3.3.10 Receiver Off Setting Packet

Table 3–16 shows Receiver Off Setting Packet bit assignments.

Table 3–16. Receiver Off Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	0	0	0	0
Byte 2	0	0	0	0	LBC	0	0	0
Byte 1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
Byte 0	ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

LBC: Low Battery Check. If this bit is set, the FLEX decoder checks the status of the LOBAT port just before leaving this receiver state. (value after reset = 0)

CLS: Control Line Setting. This bit is the value to be output on the receiver control lines (S0 – S7) for this receiver state. (value after reset = 0)

ST: Step Time. This bit is the length of time the FLEX decoder keeps the receiver off before applying the first warm-up state's receiver control value to the receiver control lines. The setting is in steps of 625 μs. Valid values are 625 μs (ST = 01) to 159.375 ms (ST = FF in hexadecimal). (value after reset = 625 μs)

3.3.11 Receiver Warm Up Setting Packets

Table 3–17 shows Receiver Warm Up Setting Packet bit assignments.

Table 3–17. Receiver Warm Up Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	0	s_2	s_1	s_0
Byte 2	SE	0	0	0	LBC	0	0	0
Byte 1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
Byte 0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

s: Setting number. This bit is the receiver control setting for which this packet's values are to be applied. Table 3–18 shows the names of each of the values for **s** that apply to this packet.

Table 3–18. Receiver Control Setting

s_2	s_1	s_0	Setting Name
0	0	1	Warm Up 1
0	1	0	Warm Up 2
0	1	1	Warm Up 3
1	0	0	Warm Up 4
1	0	1	Warm Up 5

SE: Step Enable. The receiver setting is enabled when this bit is set. If a step in the warm-up sequence is disabled, all steps following the disabled step are ignored. (value after reset = 0)

LBC: Low Battery Check. If this bit is set, the FLEX decoder checks the status of the LOBAT port just before leaving this receiver state. (value after reset = 0)

CLS: Control Line Setting. This bit is the value to be output on the receiver control lines (S0 – S7) for this receiver state. (value after reset = 0)

ST: Step Time. This bit is the amount of time the FLEX decoder waits before applying the next state's receiver control value to the receiver control lines. The setting is in steps of 625 μs. Valid values are 625 μs (ST = 01) to 79.375 ms (ST = 7F in hexadecimal). (value after reset = 625 μs)

3.3.12 3200 sps Sync Setting Packets

Table 3–19 shows the 3200 symbols per second (sps) Sync Setting Packet bit assignments.

Table 3–19. 3200 sps Sync Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	0	1	1	0
Byte 2	0	0	0	0	LBC	0	0	0
Byte 1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
Byte 0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

LBC: Low Battery Check. If this bit is set, the FLEX decoder checks the status of the LOBAT port just before leaving this receiver state. (value after reset = 0)

CLS: Control Line Setting. This bit is the value to be output on the receiver control lines (S0 – S7) for this receiver state. (value after reset = 0)

ST: Step Time. This bit is the amount of time the FLEX decoder waits before expecting good signals on the EXTS1 and EXTS0 signals after warming up. The setting is in steps of 625 μs. Valid values are 625 μs (ST = 01) to 79.375 ms (ST=7F in hexadecimal). (value after reset = 625 μs)

3.3.13 Receiver On Setting Packets

Table 3–20 shows the Receiver On Setting Packet bit assignments.

Table 3–20. Receiver On Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	s_3	s_2	s_1	s_0
Byte 2	0	0	0	0	LBC	0	0	0
Byte 1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
Byte 0	0	0	0	0	0	0	0	0

s: Setting number. This bit is the receiver control setting for which this packet's values are to be applied. Table 3–21 shows the names of each of the values for **s** that apply to this packet.

Table 3–21. Receiver On Setting Names

s_3	s_2	s_1	s_0	Setting Name
0	1	1	1	1600 sps Sync
1	0	0	0	3200 sps Data
1	0	0	1	1600 sps Data

LBC: Low Battery Check. If this bit is set, the FLEX decoder checks the status of the LOBAT port just before leaving this receiver state. (value after reset = 0)

CLS: Control Line Setting. This bit is the value to be output on the receiver control lines (S0 – S7) for this receiver state. (value after reset = 0)

3.3.14 Receiver Shutdown Setting Packets

Table 3–22 shows the Receiver Shutdown Setting Packet bit assignments.

Table 3–22. Receiver Shutdown Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	1	0	1	s
Byte 2	SE	0	0	0	LBC	0	0	0
Byte 1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
Byte 0	0	0	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

s: Setting number. This bit is the receiver control setting for which this packet's values are to be applied. Table 3–23 shows the names of each of the values for **s** that apply to this packet.

Table 3–23. Receiver Shutdown Setting Names

s	Setting Name
0	Shut Down 1
1	Shut Down 2

SE: Step Enable. The receiver setting is enabled when this bit is set. If a step in the shutdown sequence is disabled, all steps following the disabled step are ignored. (value after reset = 0)

LBC: Low Battery Check. If this bit is set, the FLEX decoder checks the status of the LOBAT port just before leaving this receiver state. (value after reset = 0)

CLS: Control Line Setting. This bit is the value to be output on the receiver control lines (S0 – S7) for this receiver state. (value after reset = 0)

ST: Step Time. This bit is the amount of time the FLEX decoder waits before applying the next state's receiver control value to the receiver control lines. The setting is in steps of 625 μs. Valid values are 625 μs (ST = 01) to 39.375 ms (ST = 3F in hexadecimal). (value after reset = 625 μs)

3.3.15 Frame Assignment Packets

The FLEX protocol defines that each address of a FLEX pager is assigned a home frame and a battery cycle. This information is determined by the service provider. The FLEX decoder must be configured so that a frame that is assigned by one or more of the address home frames and battery cycle has its corresponding configuration bit set. For example, if the FLEX decoder has one enabled address and it is assigned to frame 3 with a battery cycle of 4 (see Section 2.9, *FLEX CAPCODE,* for a definition of battery cycle), the AF bits for frames 3, 19, 35, 51, 67, 83, 99, and 115 should be set, and the AF bits for all other frames should be cleared.

When the FLEX decoder is configured for manual collapse mode by setting the MCM bit in the Roaming Control Packet, the FLEX decoder does not apply the received system collapse to the AF bits. The host should set the AF bits for all frames to be decoded on all channels. For example, if frames 0 and 64 are to be decoded on one channel and frames 4, 36, 68, and 100 decoded on another channel, all six of the corresponding AF bits should be set. The host can then change the receiver's carrier frequency after the FLEX decoder decodes frames 0, 36, 64, and 100.

There are eight Frame Assignment Packets (see Table 3–24). The IDs for these packets range from 32 to 39 (decimal).

Table 3–24. Frame Assignment Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	1	0	0	f_2	f_1	f_0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	AF_{15}	AF_{14}	AF_{13}	AF_{12}	AF_{11}	AF_{10}	AF_9	AF_8
Byte 0	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0

f: Frame range. This bit value determines which 16 frames correspond to the 16 AF bits in the packet, as shown in Table 3–25. At least one of these bits must be set when the FLEX decoder is turned on by setting the ON bit in the control packet. (value after reset = 0)

Table 3–25. Frame Range Packet Bit Assignments

f_2	f_1	f_0	AF_{15}	AF_0
0	0	0	Frame 127	Frame 112
0	0	1	Frame 111	Frame 96
0	1	0	Frame 95	Frame 80
0	1	1	Frame 79	Frame 64
1	0	0	Frame 63	Frame 48
1	0	1	Frame 47	Frame 32
1	1	0	Frame 31	Frame 16
1	1	1	Frame 15	Frame 0

AF: Assigned Frame. If this bit is set, the FLEX decoder considers the corresponding frame to be assigned via an address's home frame and pager collapse. (value after reset = 0)

3.3.16 User Address Enable Packet

The User Address Enable Packet (see Table 3–26) is used to enable and disable the 16 user address words. Although the host is allowed to change the user address words while the FLEX decoder is decoding FLEX signals, the host must disable a user address word before changing it. The ID of the User Address Enable Packet is 120 (decimal).

Table 3–26. User Address Enable Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	1	1	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	UAE_{15}	UAE_{14}	UAE_{13}	UAE_{12}	UAE_{11}	UAE_{10}	UAE_{9}	UAE_{8}
Byte 0	UAE_{7}	UAE_{6}	UAE_{5}	UAE_{4}	UAE_{3}	UAE_{2}	UAE_{1}	UAE_{0}

UAE: User Address Enable. When this bit is set, the corresponding user address word is enabled. When it is cleared, the corresponding user address word is disabled. UAE_0 corresponds to the user address word configured using a packet ID of 128, and UAE_{15} corresponds to the user address word configured using a packet ID of 143. (value after reset = 0)

3.3.17 User Address Assignment Packets

The FLEX decoder has 16 user address words. Each word can be programmed to be a short address or part of a long address. The addresses are configured using the Address Assignment Packets (see Table 3–27). Each user address can be configured as long or short and tone-only or regular. Although the host is allowed to send these packets while the FLEX decoder is on, the host must disable the user address word by clearing the corresponding UAE bit in the User Address Enable Packet before changing any of the bits in the corresponding User Address Assignment Packet. This method allows for easy reprogramming of user addresses without disrupting normal operation. The IDs for these packets range from 128 to 143 (decimal).

Table 3–27. User Address Assignment Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	1	0	0	0	a_3	a_2	a_1	a_0
Byte 2	0	LA	TOA	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}
Byte 1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_{9}	A_{8}
Byte 0	A_{7}	A_{6}	A_{5}	A_{4}	A_{3}	A_{2}	A_{1}	A_{0}

a: User Address word number. This bit specifies which address word is being configured. A zero in this field corresponds to address index zero (AI = 0) in the Address Packet received from the FLEX decoder when an address is detected (see subsection 3.4.2, *Address Packet*).

LA: Long Address. When this bit is set, the address is considered a long address. Both words of a long address must have this bit set. The first word of a long address must have an even user address word number and the second word must be in the address index immediately following the first word.

TOA: Tone Only Address. When this bit is set, the FLEX decoder considers this address a tone-only address and does not decode a vector word when the address is received. If the TOA bit of a long address word is set, the TOA bit of the other word of the long address must also be set.

A: Address word. This bit is the 21-bit value of the address word. Valid FLEX messaging addresses or Network IDs must be used.

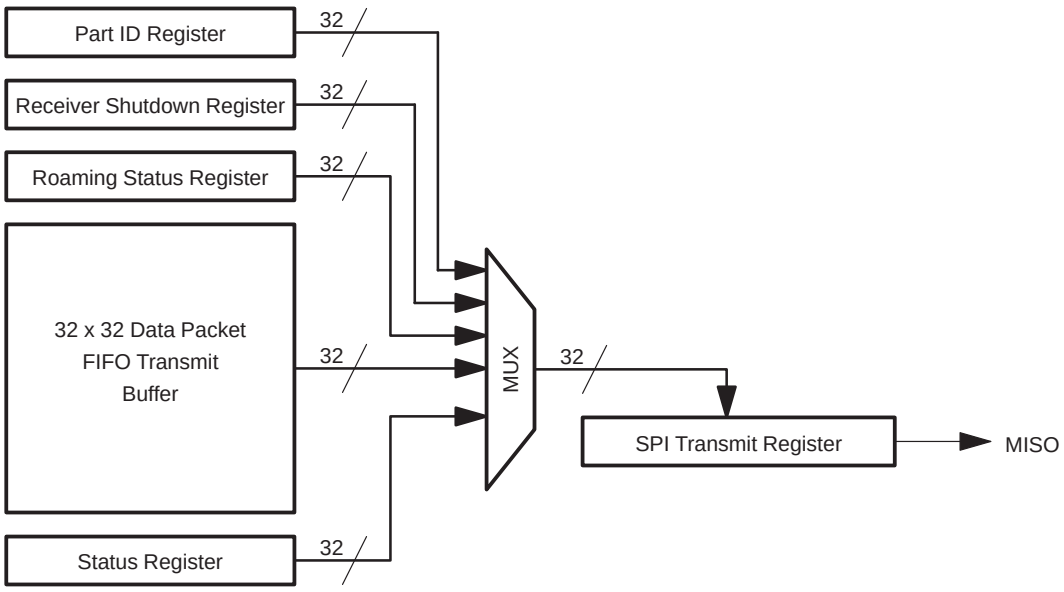
3.4 Decoder-To-Host Packet Descriptions

The following sections describe the packets of information that are sent from the FLEX decoder to the host. In all cases the packets are sent MSB first (bit 7 of byte 3 = bit 31 of the packet = MSB). The FLEX decoder determines what data should be sent to the host. See Figure 3–8 for the FLEX decoder SPI transmit functional block diagram. If the FLEX decoder is disabled through the checksum feature (see subsection 3.3.1, *Checksum Packet*), the Part ID Packet is sent. Data packets relating to data received over the air are buffered in the 32-packet transmit buffer. The data packets include Block Information Word Packets, Address Packets, Vector Packets, and Message Packets.

If the FLEX decoder is enabled and a Receiver Shutdown Packet is pending, the Receiver Shutdown Packet is sent. If there is no Receiver Shutdown Packet pending, but there is a Roaming Status Packet pending, the Roaming Status Packet is sent. If neither the Receiver Shutdown Packet nor the Roaming Status Packet is pending and there is data in the transmit buffer, a packet from the transmit buffer is sent. Otherwise, the FLEX decoder sends the Status Packet (which is not buffered). If a buffer overflow occurs, the FLEX decoder automatically stops decoding and clears the buffer information.

TI recommends that the host be designed to empty the FIFO buffer every block with enough time remaining to read a status packet. This ensures that any applicable Status Packet is received within one block of the new status available.

Figure 3–8. FLEX Decoder SPI Transmit Functional Block Diagram



3.4.1 Block Information Word Packet

The Block Information Word Packet is the first field following the synchronization codes of the FLEX protocol. (see Chapter 2, *FLEX Signal Structure*). This field contains information about the frame such as number of addresses and messages, as well as information about current time, channel ID, channel attributes, etc. The first block information word of each phase is used internally by the FLEX decoder and is never transmitted to the host, except when the FLEX decoder is in manual collapse mode and a system collapse occurs; in this case, the information is transmitted to the host.

All time and date block information words 2–4 (f = 001, 010, or 101) can be optionally sent to the host by setting the SBI bit in the control packet (see subsection 3.3.3, *Control Packet*). All block information words 2–4 can be optionally sent to the host by setting the ABI bit in the Roaming Control Packet. Table 3–28 shows the Block Information Word Packet bit assignments. When the SBI bit is set and a block information word is received with an uncorrectable number of bit errors, the FLEX decoder sends the block information word to the host with the e bit set regardless of the value of the f field in the block information word. The FLEX decoder does not support decoding of the vector and message words associated with the Data/System Message block information word (f = 101). The ID of a Block Information Word Packet is 0 (decimal).

Table 3–28. Block Information Word Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	0
Byte 2	e	p_1	p_0	x	x	f_2	f_1	f_0
Byte 1	x	x	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8
Byte 0	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0

e: Set if more than two bit errors are detected in the word or if the check character calculation fails after error correction has been performed.

p: Phase on which the block information word was found (0 = a, 1 = b, 2 = c, 3 = d).

x: Unused bits. The value of these bits is not guaranteed.

f: Word format type. The value of these bits modifies the meaning of the s bits in this packet as described in Table 3–29. If the **e** bit is not set, this field is 001, 010, or 101.

s: These are the information bits of the block information word. The definition of these bits depend on the f bits in this packet. Table 3–29 describes the block information words that the FLEX decoder decodes. See Section 2.8, *FLEX Local Time and Date,* for detailed information about these block information words.

Table 3–29. Block Information Word Definitions

$f_2 f_1 f_0$	$s_{13} s_{12} s_{11} s_{10} s_9\ s_8\ s_7\ s_6\ s_5\ s_4\ s_3\ s_2\ s_1\ s_0$	Description
000	$i_8\ i_7\ i_6\ i_5\ i_4\ i_3\ i_2\ i_1\ i_0\ C_4\ C_3\ C_2\ C_1\ C_0$	Local ID, Coverage Zone
001	$m_3\ m_2\ m_1\ m_0\ d_4\ d_3\ d_2\ d_1\ d_0\ Y_4\ Y_3\ Y_2\ Y_1\ Y_0$	Month, Day, Year
010	$S_2\ S_1\ S_0\ M_5\ M_4\ M_3\ M_2\ M_1\ M_0\ H_4\ H_3\ H_2\ H_1\ H_0$	Second, Minute, Hour
011	Reserved by FLEX protocol for future use	
100	Reserved by FLEX protocol for future use	
101	$z_9\ z_8\ z_7\ z_6\ z_5\ z_4\ z_3\ z_2\ z_1\ z_0\ A_3\ A_2\ A_1\ A_0$	System Message
110	Reserved by FLEX protocol for future use	
111	$c_9\ c_8\ c_7\ c_6\ c_5\ c_4\ c_3\ c_2\ c_1\ c_0\ T_3\ T_2\ T_1\ T_0$	Country Code, Traffic Management Flags

3.4.2 Address Packet

The Address Packet field follows the Block Information Word Packet field in the FLEX protocol. (see Chapter 2, *FLEX Signal Structure*). It contains all of the addresses in the frame. See Table 3–30 for the Address Packet bit assignments.

If fewer than three bit errors are detected in a received address word and the received address word matches an enabled address assigned to the FLEX decoder, an Address Packet is sent to the host processor. The Address Packet contains assorted data about the address and its associated vector and message. The ID of an Address Packet is 1 (decimal).

Table 3–30. Address Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	1
Byte 2	PA	p_1	p_0	LA	x	x	x	x
Byte 1	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0
Byte 0	TOA	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0

PA: Priority Address. This bit is set if the address was received as a priority address.

p: Phase on which the address was detected (0 = a, 1 = b, 2 = c, 3 = d).

LA: Long Address type. This bit is set if the address was programmed in the FLEX decoder as a long address.

AI: Address Index (valid values are 0 through 15 and 128 through 159). The index identifies which of the addresses was detected. Values 0 through 15 correspond to the 16 programmable address words. Values 128 through 159 correspond to the 16 operator messaging addresses. For long addresses, the address detect packet is only sent once, and the index refers to the second word of the address.

TOA: Tone Only Address. Set if the address was programmed in the FLEX decoder as a tone-only address. This bit is never sent for temporary or operator messaging addresses. No vector word is sent for tone-only addresses.

WN: Word Number of vector (2 – 87). Describes the location in the frame of the vector word for the detected address. This value is invalid for this packet if the TOA bit is set.

x: Unused bits. The value of these bits is not guaranteed.

3.4.3 Vector Packet

The Vector Packet field follows the Address Packet field in the FLEX protocol. See Chapter 2, *FLEX Signal Structure*, for more details. Each Vector Packet must be matched to its corresponding Address Packet. The ID of the vector packet is the word number where the vector word was received in the frame. This value corresponds to the WN bits sent in the associated Address Packet. The phase information in both the Address Packet and the Vector Packet must also match. For long addresses, the first message word is transmitted in the word location that immediately follows the associated vector (see Section 3.7, *Message Building*). The word number (identified by b_6 to b_0) in the Vector Packet indicates the message start of the second message word if the message is longer than one word.

There are several types of vectors—3 types of Numeric Vectors, a Short Message/Tone Only Vector, a Hex/Binary Vector for Address 2: Message Words located at WN = 12 to 15, phase Binary Vector, an Alphanumeric Vector, a Secure Message Vector, and a Short Instruction Vector. Each vector is described in the following subsections. The Short Instruction Vector is used for assigning temporary addresses that may be associated with a group call.

The Numeric, Hex/Binary, Alphanumeric, and Secure Message Vector Packets have associated Message Word Packets in the message field. The host must use the n and b bits of the vector word to calculate what message word locations are associated with the vector. The message word location and the phase must match.

Four of the vectors (Hex/Binary, Alphanumeric, Secure Message, and Short Instruction) enable the FLEX decoder to begin the All Frame Mode. This mode is required to allow for the decoding of temporary addresses and/or fragmented messages. The host disables the All Frame Mode after the proper time by writing to the decoder via the All Frame Mode Packet. See Section 3.8, *Building a Fragmented Message* and *Section 3.9, Operation of a Temporary Address—Group Messaging*, for more information. For any Address Packet sent to the host (except tone-only addresses), a corresponding Vector Packet is always sent. If more than two bit errors are detected (via BCH calculations, parity calculations, check character calculations, or value validation) in the vector word, the e bit is set, and the message words are not sent.

3.4.3.1 Numeric Vector Packet

Table 3–31 shows the Numeric Vector Packet bit assignments.

Table 3–31. Numeric Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
Byte 2	e	p_1	p_0	x	x	V_2	V_1	V_0
Byte 1	x	x	K_3	K_2	K_1	K_0	n_2	n_1
Byte 0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

V: Vector type identifier.

Table 3–32 shows the Numeric Vector definitions.

Table 3–32. Numeric Vector Definitions

$V_2V_1V_0$	Name	Description
011	Standard Numeric Format	No special formatting of characters is specified
100	Special Format Numeric Vector	Formatting of the received characters is predetermined by special rules in the host. See Section 2.2, *FLEX Message Word Definitions.*
111	Numbered Numeric Vector	The received information has been numbered by the service provider to indicate that all messages have been properly received

WN: Word Number of vector (2 – 87 decimal). Describes the location of the vector word in the frame.

e: This bit is set if more than two bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: Phase on which the vector was found (0 = a, 1 = b, 2 = c, 3 = d).

K: Beginning check bits of the message.

n: Number of message words in the message including the second vector word for long addresses (000 = 1 word message, 001 = 2 word message, etc.). For long addresses, the first message word is in the word location that immediately follows the associated vector.

b: Word number of message start in the message field (3 – 87 decimal). For long addresses, the word number indicates the location of the second message word.

x: Unused bits. The value of these bits is not guaranteed.

3.4.3.2 Short Message/Tone Only Vector

Table 3–33 shows the Short Message/Tone Only Vector Packet bit assignments.

Table 3–33. Short Message/Tone Only Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
Byte 2	e	p_1	p_0	x	x	V_2	V_1	V_0
Byte 1	x	x	d_{11}	d_{10}	d_9	d_8	d_7	d_6
Byte 0	d_5	d_4	d_3	d_2	d_1	d_0	t_1	t_0

V: 010 for a Short Message/Tone Only Vector.

WN: Word Number of vector (2 – 87 decimal). Describes the location of the vector word in the frame.

e: This bit is set if more than two bit errors are detected in the word or, if after error correction, the check character calculation fails.

p: Phase on which the vector was found (0 = a, 1 = b, 2 = c, 3 = d).

d: Data bits whose definition depend on the value of t in this packet, as shown in Table 3–34. If this vector is received on a long address and the e bit in this packet is not set, the decoder sends a Message Packet from the word location immediately following the Vector Packet. Except for the short message on a non-network address (t = 0), all message bits in the Message Packet are unused and should be ignored.

Table 3–34. Short Message/Tone Only Vector Definitions

t_1t_0	$d_{11}d_{10}d_9$ d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	Description
00	c_3 c_2 c_1 c_0 b_3 b_2 b_1 b_0 a_3 a_2 a_1 a_0	Short Numeric: 3 numeric characters when on a messaging address (see Note 1)
00	T_3 T_2 T_1 T_0 M_2 M_1 M_0 A_4 A_3 A_2 A_1 A_0	Part of NID when on a Network Address
01	s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0 S_2 S_1 S_0	Tone Only: 8 sources (S) and 9 unused bits (s)
10	s_1 s_0 R_0 N_5 N_4 N_3 N_2 N_1 N_0 S_2 S_1 S_0	Tone Only: 8 sources (S), message number (N), message retrieval flag (R—see Note 2), and 2 unused bits (s)
11		spare message type

Notes: 1) For long addresses, an extra five characters are sent in the Message Packet immediately following the Vector Packet.

2) For a description of the R and N bits, see the description of the same bits for numeric messages in subsection 2.2.1, *Numeric Data Message*.

t: Message type. These bits define the meaning of the d bits in this packet.

x: Unused bits. The value of these bits is not guaranteed.

3.4.3.3 Hex/Binary, Alphanumeric, and Secure Message Vector

Table 3–35 shows the Hex/Binary, Alphanumeric, and Secure Message Vector Packet bit assignments.

Table 3–35. Hex/Binary, Alphanumeric, and Secure Message Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
Byte 2	e	p_1	p_0	x	x	V_2	V_1	V_0
Byte 1	x	x	n_6	n_5	n_4	n_3	n_2	n_1
Byte 0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

V: Vector type identifier.

Table 3–36 shows the Vector type identifiers.

Table 3–36. Vector Type Identifiers

$V_2V_1V_0$	Type
000	Secure
101	Alphanumeric
110	Hex/Binary

WN: Word Number of vector (2 – 87 decimal). Describes the location of the vector word in the frame.

e: This bit is set if more than two bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: Phase on which the vector was found (0 = a, 1 = b, 2 = c, 3 = d).

n: Number of message words in this frame including the first message word that immediately follows a long address vector. Valid values are 1 through 85 decimal.

b: Word number of message start in the message field. Valid values are 3 through 87 decimal.

x: Unused bits. The value of these bits is not guaranteed.

Note: For long addresses, the first message packet is sent immediately following the Vector Packet. The b bits indicate the second message word in the message field, if one exists.

3.4.3.4 Short Instruction Vector

The Short Instruction Vector is used for assigning temporary addresses that may be associated with a group call. Table 3–37 shows the Short Instruction Vector Packet bit assignments.

Table 3–37. Short Instruction Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
Byte 2	e	p_1	p_0	x	x	V_2	V_1	V_0
Byte 1	x	x	d_{10}	d_9	d_8	d_7	d_6	d_5
Byte 0	d_4	d_3	d_2	d_1	d_0	i_2	i_1	i_0

V: 001 for a Short Instruction Vector.

WN: Word Number of vector (2 – 87 decimal). Describes the location of the vector word in the frame.

e: This bit is set if more than two bit errors are detected in the word or, if after error correction, the check character calculation fails.

p: Phase on which the vector was found (0 = a, 1 = b, 2 = c, 3 = d).

d: Data bits whose definition depend on the **i** bits in this packet, as shown in Table 3–38. If this vector is received on a long address and the **e** bit in this packet is not set, the decoder sends a Message Packet immediately following the Vector Packet. All message bits in the message packet are unused and should be ignored.

Table 3–38. Short Instruction Vector Definitions

$i_2i_1i_0$	d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	Description
000	a_3 a_2 a_1 a_0 f_6 f_5 f_4 f_3 f_2 f_1 f_0	Temporary address assignment (see Note)
001		Reserved
010		Reserved
011		Reserved
100		Reserved
101		Reserved
110		Reserved
111		Reserved for test

Note: Assigned temporary address (a) and assigned frame (f). See Section 3.9, *Operation of a Temporary Address—Group Messaging*.

i: Instruction type. These bits define the meaning of the **d** bits in this packet.

x: Unused bits. The value of these bits is not guaranteed.

3.4.4 Message Packet

The Message Packet field follows the Vector Packet field in the FLEX protocol. It contains the message data, checksum information, and may contain fragment numbers and message numbers. See Section 2.2, *FLEX Message Word Definitions*.

If the error bit of a vector word is not set and the vector word indicates that there are message words associated with the page, the message words are sent in Message Packets. See Table 3–39 for the Message Packet bit assignments.

The ID of the Message Packet is the word number where the message word was received in the frame.

Table 3–39. Message Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN6	WN5	WN4	WN3	WN2	WN1	WN0
Byte 2	e	p_1	p_0	i_{20}	i_{19}	i_{18}	i_{17}	i_{16}
Byte 1	i_{15}	i_{14}	i_{13}	i_{12}	i_{11}	i_{10}	i_9	i_8
Byte 0	i_7	i_6	i_5	i_4	i_3	i_2	i_1	i_0

WN: Word Number of message word (3 – 87 decimal). Describes the location of the message word in the frame.

e: This bit is set if more than two bit errors are detected in the word.

p: Phase on which the message word was found (0 = a, 1 = b, 2 = c, 3 = d).

i: These are the information bits of the message word. The definitions of these bits depend on the vector type and which word of the message is being received. See Section 2.2, *FLEX Message Word Definitions,* for a detailed description of these bits.

3.4.5 Roaming Status Packet

The FLEX decoder prompts the host to read a Roaming Status Packet if RSR, MS1, MFI, MS2, MBI, MAW, NDR_1, NDR_0, NBU, or SCU is set. Roaming Status Packet Bit assignments are shown in Table 3–40.

Table 3–40. Roaming Status Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	0	0	0	0	0
Byte 2	RSR	MS1	MFI	MS2	MBI	MAW	NBU	n
Byte 1	x	x	x	x	x	x	NDR_1	NDR_0
Byte 0	x	x	x	x	SCU	RSC_2	RSC_1	RSC_0

RSR: Resynchronized Signal Received. Set when the FLEX decoder detects a resynchronization signal, and when the host configures the FLEX decoder to ignore it via the IRS bit in the Roaming Control Packet. This bit is cleared when read.

MS1: Missed Synchronization 1. Set when the FLEX decoder fails to detect the first synchronization pattern ($A/\overline{A}$) of a FLEX frame, and when the FLEX decoder is configured to report missed frame information via the MFC bit in the Roaming Control Packet. This bit is cleared when read.

MFI: Missed Frame Information word. Set when the frame information word is received with an uncorrectable number of errors, and when the FLEX decoder is configured to report missed frame information via the MFC bit in the Roaming Control Packet. This bit is cleared when read.

MS2: Missed Synchronization 2. Set when the FLEX decoder fails to detect the second synchronization pattern (C/$\overline{C}$) of a frame, and when the FLEX decoder is configured to report missed frame information via the MFC bit in the Roaming Control Packet. This bit is cleared when read.

MBI: Missed Block Information word. Set when at least one of the block information word 1's is received with an uncorrectable number of errors, and when the FLEX decoder is configured to report missed frame information via the MFC bit in the Roaming Control Packet. This bit is set no more than once per frame, regardless of the number of phases in the frame. This bit is cleared when read.

MAW: Missed Address Word. Set when any address words in the address field are received with an uncorrectable number of errors, and when the FLEX decoder is configured to report missed frame information via the MFC bit in the Roaming Control Packet. This bit is set no more than once per frame, regardless of the number of address words in the frame. This bit is cleared when read.

NDR: Noise Detect Result. These bits indicate the result of a noise detection. The results of noise detections initiated by setting the SND bit in the Roaming Control Packet are always reported. The results of the automatic noise detections performed in asynchronous mode are only reported if the RND bit is set in the Roaming Control Packet. When continuous noise detections during block data are enabled by setting the CND bit in the Roaming Control Packet, only the *No FLEX signal detected* results are reported. These bits are cleared when read. Noise Detection results are shown in Table 3–41.

Table 3–41. Noise Detection Results

NDR	Noise Detection Result
00	No information
01	Noise detection was abandoned
10	FLEX signal detected
11	FLEX signal not detected

NBU: Network Bit Update. Set when the NBC bit in the roaming control packet is set and a frame information word is received with a correctable number of errors. This bit does not set when the frame information word is not received because the first synchronization pattern (A/$\overline{A}$) is missing. This bit is cleared when read.

n: Network bit value. When NBU is set, this is the value of the n bit in the last received frame information word.

SCU: System Collapse Update. Set when the Flex decoder is configured for manual collapse mode by setting the MCM bit in the Roaming Control Packet, and when the system collapse of a frame is received. This bit is set no more than once per frame, regardless of the number of phases in the frame. This bit is not set in frames that do not receive block information word 1's properly. This bit is cleared when read.

RSC: Received System Collapse. When SCU is set, this value represents the system collapse value that is received in the frame.

3.4.6 Receiver Shutdown Packet

The Receiver Shutdown Packet is sent in both synchronous and asynchronous mode. It indicates to the host that the receiver is turned off, and it determines the amount of time remaining until the FLEX decoder automatically turns it back on.

Table 3–42. Receiver Shutdown Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	1	1	1	1	0
Byte 2	FNV	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
Byte 1	TNF_7	TNF_6	TNF_5	TNF_4	TNF_3	TNF_2	TNF_1	TNF_0
Byte 0	FCO	NAF_6	NAF_5	NAF_4	NAF_3	NAF_2	NAF_1	NAF_0

FNV: Frame Number Valid. This bit is set if the last frame information word is correctable, and if the frame number is the expected value. When in asynchronous mode, this value is 0.

CF: Current Frame. When in synchronous mode, this is the current frame number. This value is latched on the negative edge of the $\overline{\text{READY}}$ line when this packet is sent to the host. The value of this field is valid only if the FLEX decoder is in synchronous mode and the FIV bit in the status packet is set. When in asynchronous mode, this value is 0.

TNF: Time to Next Frame. In synchronous mode, TNF indicates the time to the start of the A-word check, if the FLEX decoder warms up for the next frame. In asynchronous mode, TNF indicates the time to the start of the next automatic noise detection. See Section 3.10, *Using the Receiver Shutdown Packet*, for an explanation on how to use this value. This value is latched on the negative edge of the $\overline{\text{READY}}$ line when this packet is sent to the host.

FCO: Frame Carried On. Set if the FLEX decoder is decoding the next frame due to the reception of a non-zero carry-on value in a previous frame. In asynchronous mode, this value is 0.

NAF: Next Assigned Frame. This is the frame number of the next frame that the FLEX decoder is scheduled to decode when the receiver shuts down. The value of this field is valid only if the FLEX decoder is in synchronous mode and the FIV bit in the status packet is set. In asynchronous mode, this value is 0.

3.4.7 Status Packet

The Status Packet contains various types of information that the host may require. The Status Packet is sent to the host whenever the FLEX decoder is polled and has no other data to send. The FLEX decoder can also prompt the host to read the Status Packet due to events for which the FLEX decoder was configured to send it (see subsection 3.3.2, *Configuration Packet*, and subsection 3.3.3, *Control Packet*, for a detailed description of the bits). Table 3–43 shows the Status Packet bit assignments. The FLEX decoder prompts the host to read a Status Packet if any of the following conditions are true.

- The SMU bit in the Status Packet and the SME bit in the Configuration Packet are set.
- The MT bit in the Status Packet and the MTE bit in the Configuration Packet are set.
- The EOF bit in the Status Packet is set.
- The LBU bit in the Status Packet is set.
- The EA bit in the Status Packet is set.
- The BOE bit in the Status Packet is set.

The ID of the Status Packet is 127 (decimal).

Table 3–43. Status Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	1	1	1	1	1
Byte 2	FIV	f_6	f_5	f_4	f_3	f_2	f_1	f_0
Byte 1	SM	LB	x	x	c_3	c_2	c_1	c_0
Byte 0	SMU	LBU	x	MT	x	EOF	EA	BOE

FIV: Frame Info Valid. This bit is set when a valid frame info word has been received since becoming synchronous to the system and the f, c, and n fields contain valid values. If this bit is clear, no valid frame info words have been received since the FLEX decoder became synchronous to the system. This value changes from 0 to 1 at the end of block 0 of the frame in which the first frame info word is properly received. It is cleared when the FLEX decoder goes into asynchronous mode. This bit is initialized to 0 when the FLEX decoder is reset and when the FLEX decoder is turned off by clearing the ON bit in the Control Packet.

f: Current frame number. This bit value is updated every frame regardless of whether the FLEX decoder needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SM: Synchronous Mode. This bit is set when the FLEX decoder is synchronous to the system. The FLEX decoder sets this bit when the first synchronization words are received. It clears this bit when synchronization to the FLEX decoder signal is lost in any frame for 8, 16, or 32 minutes (depending on the number of assigned frames and the system collapse). This bit is initialized to 0 when the FLEX decoder is reset and when it is turned off by clearing the ON bit in the Control Packet.

LB: Low Battery. This bit is set to the value last read from the LOBAT pin. The host controls when the LOBAT pin is read via the Receiver Control Packets. This bit is initialized to 0 at reset. It is also initialized to the inverse of the LBP bit in the Configuration Packet when the FLEX decoder is turned on by setting the ON bit in the Control Packet.

c: Current system cycle number. This value is updated every frame, regardless of whether the FLEX decoder needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SMU: Synchronous Mode Update. This bit is set if the SM bit has been updated in this packet. When the FLEX decoder is turned on, this bit is set when the first synchronization words are found (SM changes to 1) or when the first synchronization search window after the FLEX decoder is turned on expires (SM stays 0). The latter condition gives the host the option of assuming the paging device is in range when it is turned on, and displaying out-of-range only after the initial A-word search window expires. After the initial synchronous mode update, the SMU bit is set whenever the FLEX decoder transitions from/to synchronous mode. It is cleared when read. Changes in the SM bit due to turning off the FLEX decoder do not cause the SMU bit to be set. This bit is initialized to 0 when the FLEX decoder is reset.

LBU: Low Battery Update. This bit is set if the value on two consecutive reads of the LOBAT pin yielded different results. It is cleared when read. The host controls when the LOBAT pin is read via the Receiver Control Packets. Changes in the LB bit due to turning on the FLEX decoder do not cause the LBU bit to be set. This bit is initialized to 0 when the FLEX decoder is reset.

MT: Minute Time-Out. This bit is set if one minute has elapsed. It is cleared when read. This bit is initialized to 0 when the FLEX decoder is reset.

EOF: End Of Frame. This bit is set when the FLEX decoder is in All Frame Mode and the end of frame has been reached. The FLEX decoder is in All Frame Mode if the All Frame Mode enable counter is non-zero, if any temporary address enabled counter is non-zero, or if the FAF bit in the All Frame Mode Packet is set. It is cleared when read. This bit is initialized to 0 when the FLEX decoder is reset.

EA: End of Address. If EAE of the control packet is set and an address is in the frame, EA is set after the FLEX decoder processes the last address in the frame. Because data packets take priority over status packets, the status packet with the EA bit set will come after all address packets for the frame. It is cleared when read. This bit is initialized to 0 when the FLEX decoder is reset.

BOE: Buffer Overflow Error. This bit is set when information has been lost due to slow host response time. When the SPI transmit buffer on the FLEX decoder overflows, the FLEX decoder clears the transmit buffer, turns off decoding by clearing the ON bit in the Control Packet, and sets this bit. Cleared when read. This bit is initialized to 0 when the FLEX decoder is reset.

x: Unused bits. The value of these bits is not guaranteed.

3.4.8 Part ID Packet

The Part ID Packet is sent by the FLEX decoder whenever the FLEX decoder is disabled due to the checksum feature (see subsection 3.3.1, *Checksum Packet*). Because the FLEX decoder is disabled after reset, this is the first packet that will be received by the host after reset. Table 3–44 shows the Part ID Packet bit assignments. The ID of the Part ID Packet is 255 (decimal)**.**

Table 3–44. Part ID Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	1	1	1	1	1	1	1	1
Byte 2	MDL_1	MDL_0	CID_{13}	CID_{12}	CID_{11}	CID_{10}	CID_9	CID_8
Byte 1	CID_7	CID_6	CID_5	CID_4	CID_3	CID_2	CID_1	CID_0
Byte 0	REV_7	REV_6	REV_5	REV_4	REV_3	REV_2	REV_1	REV_0

MDL: Model. This identifies the FLEX decoder model. Current value is 0.

CID: Compatibility ID. This value describes what other parts with the same model number are compatible with this part. Current value is 3. Any future versions of FLEX decoder that have MDL set to 0 and CID_1 set to 1 will be 100% compatible with this version. CID_0 is set to 1 because this chip is 100% compatible with all standard FLEX decoders.

REV: Revision. This identifies the revision and manufacturer of the FLEX decoder. Currently defined values are shown in Table 3–45.

Table 3–45. FLEX Decoder Revisions

Rev	Description
0, 1, 2, 4	Preproduction Parts
3	Motorola Semiconductor Products Sector Production Parts
5	Texas Instruments Production Parts

3.5 Electrical Characteristics

Table 3–46 shows the absolute maximum ratings over operating temperature ranges for the TLV5593 FLEX roaming decoder.

Table 3–46. Absolute Maximum Ratings Over Operating Temperature Ranges (Unless Otherwise Noted)†

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input voltage range, failsafe	–0.5 V to 6.5 V
Output voltage range, standard	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1)	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2)	±20 mA
Virtual junction temperature, T_J	150°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Notes: 1) Applies to input and bidirectional buffers. V_I > V_{CC} does not apply to fail-safe pins.

2) Applies to output and bidirectional buffers. V_O > V_{CC} does not apply to fail-safe pins.

Table 3–47 shows the recommended operating conditions for the TLV5593 FLEX roaming decoder.

Table 3–47. Recommended Operating Conditions

		Min	Nom	Max	Unit
V_{CC}	Supply voltage	1.8	3.3	3.6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage†	0		V_{CC}	V
V_{IH}	High-level input voltage	0.7V_{CC}			V
V_{IL}	Low-level input voltage			0.2V_{CC}	V
t_t	Input transition (rise and fall) time	0		25	ns
T_A	Operating ambient temperature range	–40	25	90	°C
T_J	Virtual junction temperature‡	–40	25	125	°C

† Applies to output buffers

‡ These junction temperatures reflect simulation conditions. Absolute maximum junction temperature is 150°C. Customer is responsible for verifying junction temperature.

Table 3–48 shows the electrical characteristics over recommended operating conditions for the TLV5593 FLEX roaming decoder.

Table 3–48. Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)

	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = Rated	V_{CC} –0.5		V
V_{OL}	Low-level output voltage	I_{OL} = Rated		0.5	V
V_{IT+}	Positive-going threshold voltage†	CMOS compatible		$0.7V_{CC}$	V
$V_{IT–}$	Negative-going threshold voltage†	CMOS compatible	$0.2V_{CC}$		V
V_{hys}	Hysteresis ($V_{IT+} – V_{IT–}$)	CMOS compatible	$0.1V_{CC}$	$0.3V_{CC}$	V
I_{OZ}	3-state-output Hi-Z current	$V_I = V_{CC}$ or GND‡		±10	µA
I_{IL}	Low-level input current	V_I = GND§		–1	µA
I_{IH}	High-level input current	$V_I = V_{CC}$¶		1	µA

† Applies to input and bidirectional buffers with hysteresis
‡ 3-state or open-drain output must be in the high-impedance mode.
§ Specifications only apply with pullup terminator turned off.
¶ Specifications only apply with pulldown terminator turned off.

3.6 Receiver Control

The FLEX decoder has eight programmable receiver control lines (S0–S7). The host controls the receiver warm-up and shut-down timing and the various settings on the control lines through configuration registers on the FLEX decoder. The configuration registers for most settings allow the host to configure (1) what setting is applied to the control lines, (2) how long to apply the setting, and (3) if the low battery (LOBAT) input pin is polled before changing from the setting. With this programmability, the FLEX decoder should be able to interface with many off-the-shelf receiver ICs. For details on the configuration of the receiver control settings, see subsection 3.3.9, *Receiver Control Configuration Packets*.

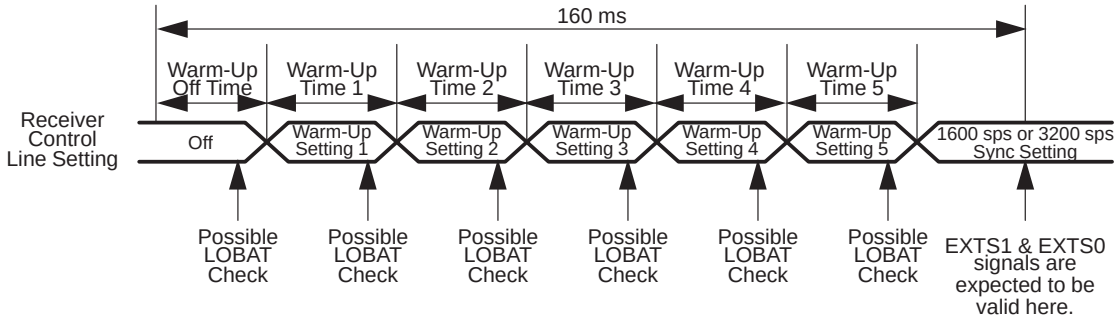
3.6.1 Receiver Settings at Reset

The receiver control ports are three-state outputs that are set to the high-impedance state when the FLEX decoder is reset and until the corresponding FRS bit in the receiver line control packet is set, or until the FLEX decoder is turned on by setting the ON bit in the Control Packet. This allows the designer to force the receiver control lines to the receiver off setting with external pullup or pulldown resistors before the host can configure these settings in the FLEX decoder. When the FLEX decoder is turned on, the receiver control ports are driven to the settings configured by the Receiver Control Configuration Packet until the FLEX decoder is reset again.

3.6.2 Automatic Receiver Warm-Up Sequence

The FLEX decoder allows for up to six steps associated with warming up the receiver. When the FLEX decoder turns on the receiver while decoding, it starts the warm-up sequence 160 ms before it requires valid signals at the EXTS0 and EXTS1 input pins. The first step of the warm-up sequence involves leaving the receiver control lines in the Off state for the amount of time programmed for Warm-Up Off Time. At the end of the Warm-Up Off Time, the first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting. Each subsequent warm-up setting is applied to the receiver control lines for their corresponding time until a disabled warm-up setting is found. At the end of the last used warm-up setting, the 1600 symbols per second (sps) Sync Setting or the 3200 sps Sync Setting is applied to the receiver control lines, depending on the current state of the FLEX decoder. The sum total of all of the used warm-up times and the Warm-Up Off Time must not exceed 160 ms. If it exceeds 160 ms, the FLEX decoder executes the receiver shut-down sequence at the end of the 160 ms warm-up period. Figure 3–9 shows the receiver warm-up sequence during decoding when all warm-up settings are enabled.

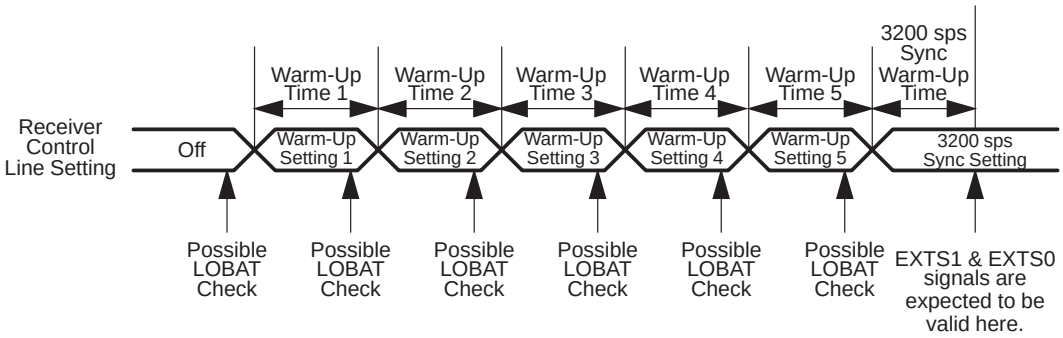
Figure 3–9. Automatic Warm-Up Sequence



3.6.3 Host-Initiated Receiver Warm-Up Sequence

The host can cause the FLEX decoder to warm up the receiver if the host (1) turns on the FLEX decoder with the ON bit in the control packet, (2) requests noise detection by setting the SND bit in the Roaming Control Packet, or (3) requests an A-word search by setting the SAS bit in the Roaming Control Packet. When the FLEX decoder warms up the receiver in response to one of these host requests, the first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting. Each subsequent warm-up setting is applied to the receiver control lines for their corresponding time until a disabled warm-up setting is found. When a disabled warm-up setting is found, the 3200 sps Sync Setting (for ON and SND warmups) or the 1600 sps Sync Setting (for SAS warmups) is applied to the receiver control lines and the decoder does not expect a valid signal until after the 3200 sps Sync Warm-Up Time (for ON, SND, and SAS warmups) has expired. Figure 3–10 shows the receiver warm-up sequence when the host initiates a warm-up sequence and when all warm-up settings are enabled.

Figure 3–10. Host-Initiated Warm-Up Sequence



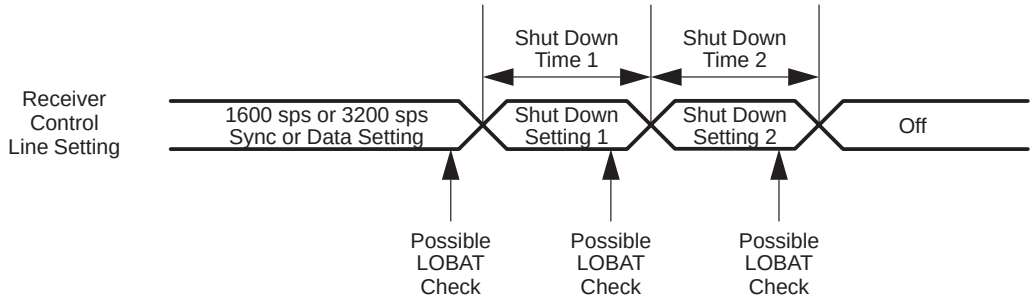
3.6.4 Receiver Shut-Down Sequence

The FLEX decoder allows for up to three steps associated with shutting down the receiver. When the FLEX decoder decides to turn off the receiver, the first shutdown setting, if enabled, is applied to the receiver control lines for the corresponding shutdown time. At the end of the last used shutdown time, the *Off* setting is applied to the receiver control lines. If the first shutdown setting is not enabled, the FLEX decoder transitions directly from the current *On*

setting to the *Off* setting. Figure 3–11 shows the receiver turn-off sequence when all shutdown settings are enabled.

If the receiver is on or being warmed up when the decoder is turned off (by clearing the ON bit in the Control Packet), the FLEX decoder executes the receiver shutdown sequence. If the FLEX decoder is executing the shutdown sequence when the FLEX decoder is turned on (by setting the ON bit in the Control Packet), the FLEX decoder completes the shutdown sequence before starting the warm-up sequence.

Figure 3–11. Receiver Shutdown Sequence



3.6.5 Miscellaneous Receiver States

In addition to the warm-up and shutdown states, the FLEX decoder has four other receiver states. When these settings are applied to the receiver control lines, the FLEX decoder decodes the EXTS1 and EXTS0 input signals. The timing of these signals and their duration depends on the data that the FLEX decoder decodes. The four settings are as follows:

- **1600-sps Sync Setting**:

  This setting is applied when the FLEX decoder is searching for a 1600-sps signal.

- **3200-sps Sync Setting**:

  This setting is applied when the FLEX decoder is searching for a 3200-sps signal.

- **1600-sps Data Setting**:

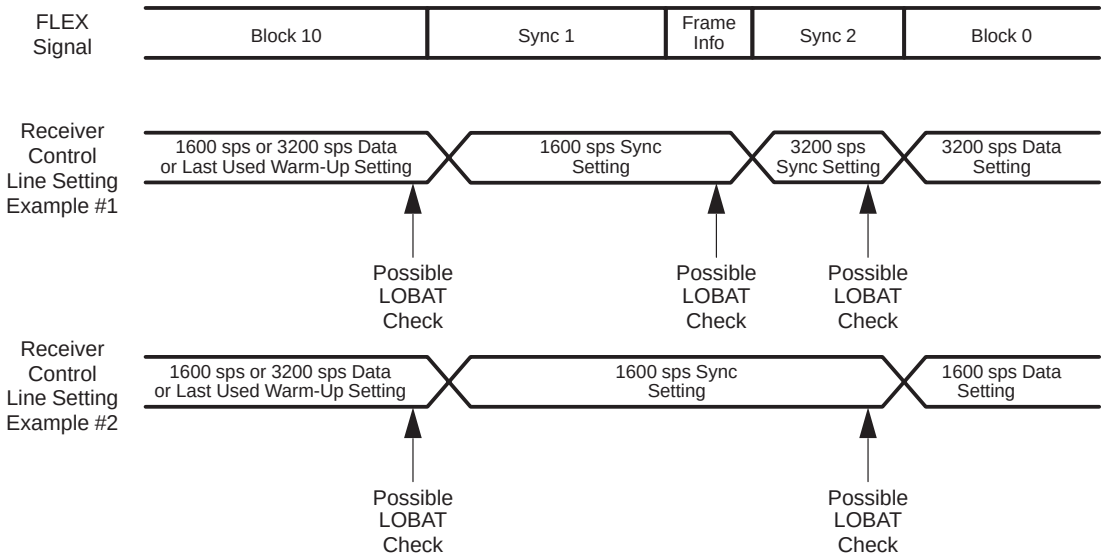
  This setting is applied after the FLEX decoder has found the C or $\overline{C}$ sync word in a 1600-sps frame.

- **3200-sps Data Setting**:

  This setting is applied after the FLEX decoder has found the C or $\overline{C}$ sync word in a 3200-sps frame.

Figure 3–12 shows some examples of how these settings are used in the FLEX decoder.

Figure 3–12. Examples of Receiver Control Transitions



3.6.6 Low Battery Detection

The FLEX decoder can be configured to poll the LOBAT input pin at the end of every receiver control setting. This check can be enabled or disabled for each receiver control setting. If the poll is enabled for a setting, the pin is read just before the FLEX decoder changes the receiver control lines from that setting to another setting. The FLEX decoder sends a Status Packet whenever the value on two consecutive reads of the LOBAT pin yields different results.

3.7 Message Building

A simple message consists of an Address Packet followed by a Vector Packet indicating the word numbers of associated Message Packets. Table 3–49 and Table 3–50 show a more complex example of receiving three Messages and two Block Information Word Packets in the first two blocks of a 2-phase 3200 bps, FLEX frame. Note that the messages shown may be portions of fragmented or group messages. Note further that in the case of a 6400-bps FLEX signal, there would be four phases: A, B, C and D, and in the case of a 1600-bps signal, there would be only a single phase, A.

Table 3–49 shows the block number, word number (WN), and word content of both phases A and C. Note that the contents of words not meant to be received by the host are left blank. Each phase begins with a block information word (WN 0); this is not sent to the host. The first message is in phase A and has an address (WN 3), vector (WN 7), and three message words (WN 9 – 11). The second message is also in phase A and has an address (WN 4), a vector (WN 8), and four message words (WN 12 – 15). The third message is in phase C and has a 2-word long address (WN 5 – 6) followed by a vector (WN 10) and three message words. Because the third message is sent on a long address, the first message word (WN 11) begins immediately after the vector. The vector indicates the location of the second and third message words (WN 14 – 15).

Table 3–49. FLEX Signal

Block	Word Number	Phase A	Phase C
0	0	BIW1	BIW1
	1		BIW
	3	Address 1	BIW
	4	Address 2	
	5		Long Address 3 Word 1
	6		Long Address 3 Word 2
	7	Vector 1	
1	8	Vector 2	
	9	Message 1,1	
	10	Message 1,2	Vector 3
	11	Message 1,3	Message 3,1
	12	Message 2,1	
	13	Message 2,2	
	14	Message 2,3	Message 3,2
	15	Message 2,4	Message 3,3

Table 3–50 shows the sequence of packets received by the host. The FLEX decoder processes the FLEX signal one block at a time in the assigned phase. Thus, the address and vector information in block 0 phase A is packetized and sent to the host in packets 1–3. Then, information in block 0 phase C (two block information words and one long address) is packetized and set to the host in packet 4–6. Packets 7–18 correspond to information in block 1, processed in phase A first and in phase C second.

Table 3–50. FLEX Decoder Packet Sequence

Packet	Packet Type	Phase	Word Number	Comment
1st	Address	A	N.A. (7)	Address 1 has a vector located at WN 7.
2nd	Address	A	N.A. (8)	Address 2 has a vector located at WN 8.
3rd	Vector	A	7	Vector for Address 1: Message Words located at WN = 9 to 11, phase A
4th	BIW	C	N.A.	If BIW is enabled, then BIW packet is sent.
5th	BIW	C	N.A.	If BIW is enabled, then BIW packet is sent.
6th	Long Address	C	N.A. (10)	Long Address 3 has a vector beginning in word 10 of phase C.
7th	Vector	A	8	Vector for Address 2: Message Words located at WN = 12 to 15, phase A
8th	Message	A	9	Message information for Address 1
9th	Message	A	10	Message information for Address 1
10th	Message	A	11	Message information for Address 1
11th	Message	A	12	Message information for Address 2
12th	Message	A	13	Message information for Address 2
13th	Message	A	14	Message information for Address 2
14th	Message	A	15	Message information for Address 2
15th	Vector	C	10	Vector for Long Address 3: Message Words located at WN = 14 to 15, phase C
16th	Message	C	11	Second word of Long Vector is first message information word of Address 3.
17th	Message	C	14	Message information for Address 3
18th	Message	C	15	Message information for Address 3

The first message is built by relating packets 1, 3, and 8–10. The second message is built by relating packets 2, 7, and 11–14. The third message is built by relating packets 6 and 15–18. Additionally, the host may process block information in packets 4 and 5 for time setting information.

3.8 Building a Fragmented Message

The longest message that fits into a frame is 84 code words, total of message data. Three alpha characters per word yield a maximum message of 252 characters in a frame assuming no other traffic. Messages longer than this value must be sent as several fragments.

Additional fragments can be expected when the continue bit in the first Message Word is set. This causes the pager to examine every following frame for an additional fragment until the last fragment with the continue bit reset is found. The only requirement relating to the placement in time of the remaining fragments is that no more than 32 frames (1 minute) or 128 frames (4 minutes) as indicated by the service provider may pass between fragment receptions.

Each fragment contains a check sum character to detect errors in the fragment, a fragment number 0, 1, or 2 to detect missing fragments, a message number to identify which message the fragment is a part, and the continue bit which either indicates that more fragments are in queue or that the last fragment has been received. All of this information is described in *Section 2.2, FLEX Message Word Definitions*.

The following describes the sequence of events between the host and the FLEX decoder required to handle a fragmented message:

- ❑ The host receives a vector indicating one of the following types:

$V_2V_1V_0$	Type
000	Secure
101	Alphanumeric
110	Hex/Binary

- ❑ The FLEX decoder increments the all frame mode counter inside the FLEX decoder and begins to decode all of the following frames.

- ❑ The host receives the Message Packet(s) contained within that frame followed by a Status Packet. The host must decide based on the Message Packet to return to normal decoding operation. If the message is indicated as fragmented by the Message Continued Flag C being set in the Message Packet for a Secure, Alphanumeric or Hex/Binary Message, then the host does not decrement the all frame mode counter at this time. The host decrements the counter if the Message Continued Flag C is clear by writing the All Frame Mode Packet to the FLEX decoder with the DAF bit = 1. If no other fragments, temporary addresses are pending, or the FAF bit is clear in the All Frame Mode Register, then the FLEX decoder returns to normal operation.

- The FLEX decoder continues to decode all of the frames and passes any address information, vector information and message information to the host followed by a status packet indicating the end of the frame. If the message is indicated as fragmented by the Message Continued Flag C is set in the Message Packet for a Secure, Alphanumeric or Hex/Binary Message then the host remains in the receive mode expecting more information from the FLEX decoder.

- After the host receives the second and subsequent fragment with the Message Continued Flag C = 1, it should decrement the all frame mode counter by sending an All Frame Mode Packet to the FLEX decoder with the DAF bit = 1. Alternatively, the host may choose to decrement the counter at the end of the entire message by decrementing the counter once for each fragment received.

- When the host receives a Message Packet with the Message Continued Flag C = 0, it will send two All Frame Mode Packets to the FLEX decoder with the DAF bit = 1. The two packets decrement the count for the first fragment and the last fragment. This decrements the all frame counter to zero, if no other fragmented messages or temporary addresses are pending, or if the FAF bit is clear in the All Frame Mode Register, and returns the FLEX decoder to normal operation.

- The above process must be repeated for each occurrence of a fragmented message. The host must keep track of the number of fragmented messages being decoded and ensure the all frame mode counter decrements after each fragment or after each fragmented message. Table 3–51 and Table 3–52 show alphanumeric message without fragmentation and with fragmentation, respectively.

Table 3–51. Alphanumeric Message Without Fragmentation

Packet	Packet Type	Phase	All Frame Counter	Comment
1st	Address 1	A	0	Address 1 is received.
2nd	Vector 1	A	1	Vector = Alphanumeric Type
3rd	Message	A	1	Message Word received C bit = 0, No more fragments are expected.
4th	TBD†		0	Host writes All Frame Mode Packet to the FLEX decoder with the DAF bit = 1.

† TBD – Host Initiated Packet. The FLEX decoder returns a packet according to section 3.4, *Decoder-To-Host Packet Descriptions.*

Table 3–52. Alphanumeric Message With Fragmentation

Packet	Packet Type	Phase	All Frame Counter	Comment
1st	Address 1	A	0	Address 1 is received.
2nd	Vector 1	A	1	Vector = Alphanumeric Type
3rd	Message	A	1	Message Word received C bit = 1, Message is fragmented, more expected
4th	Status		1	End of Frame Indication (EOF = 1)
5th	Address 1	B	1	Address 1 is received
6th	Vector 1	B	2	Vector = Alphanumeric Type
7th	Message	B	2	Message Word received C bit = 1, Message is fragmented, more expected.
8th	TBD†		1	Host writes All Frame Mode Packet to the FLEX decoder with the DAF bit = 1.
9th	Status		1	End of Frame Indication (EOF = 1)
10th	Address 1	A	1	Address 1 is received.
11th	Vector 1	A	2	Vector = Alphanumeric type
12th	Message	A	2	Message Word received C bit = 0, No more fragments are expected.
13th	TBD[a]		1	Host writes All Frame Mode Packet to the FLEX decoder with the DAF bit = 1.
14th	TBD[a]		0	Host writes All Frame Mode Packet to the FLEX decoder with the DAF bit = 1.

† TBD – Host Initiated Packet. The FLEX decoder returns a packet according to section 3.4, *Decoder-to-Host Packet Descriptions*.

3.9 Operation of a Temporary Address—Group Messaging

The FLEX protocol allows for a dynamic group call for the purpose of sending a common message to a group of paging devices. The dynamic group call approach assigns a Temporary Address using the personal address and the short instruction vector. The temporary address must be disabled by the host after the message is completed.

The FLEX protocol specifies 16 addresses for the dynamic group call, which may be temporarily activated in a specific future frame (If the designated frame is equal to the present frame the host is to interpret this as the next occurrence of this frame four minutes in the future.) The temporary address is valid for one message starting in the specified frame and remaining valid throughout the following frames to the completion of the message. If the message is not found in the specified frame (frame defined by a full 7-bit frame number) the host must disable the assigned temporary address.

The following describes the sequence of events between the host and the FLEX decoder required to handle a temporary address:

- Following an Address Packet, the host receives a Vector Packet with $V_2V_1V_0$ = 001 and $i_2i_1i_0$ = 000 for a Short Instruction Vector indicating a temporary address has been assigned to this pager. The vector packet indicates which temporary address is assigned and the frame in which the temporary address is expected.
- The FLEX decoder increments the corresponding temporary address counter and begin to decode all of the following frames.
- The FLEX decoder continues to decode all of the frames and passes any address information, vector information and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
- There are several scenarios that may occur with temporary addresses.
    1) The temporary address is not found in the frame assigned and therefore the host must terminate the temporary address mode by sending an All Frame Mode Packet to the FLEX decoder with the DTA bit of the particular temporary address set.
    2) The temporary address is found in the frame it was assigned and was not a fragmented message. Again, the host must terminate the temporary address mode by sending an All Frame Mode Packet to the FLEX decoder with the DTA bit of the particular temporary address set.
    3) The temporary address is found in the assigned frame and it is a fragmented message. In this case, the host must follow the rules for Operation of a Fragmented Message and determine the proper time to stop the all frame mode operation. In this case, the host must write to the DAF bit with a 1 and the appropriate DTA bit with a 1 in the All Frame Mode Register in order to terminate both the fragmented message and the temporary address.
- The above operation is repeated for every temporary address.

3.10 Using the Receiver Shutdown Packet

The following subsections discuss the transmission of timing information to the host via the Receiver Shutdown Packet.

3.10.1 Calculating Remaining Time

The Receiver Shutdown Packet gives timing information to the host. Two times are of particular interest when a roaming algorithm is implemented.

- TimeToWarmUpStart

  This is the amount of time there is before the receiver begins to warm up (i.e., transition from the off state to the first warm-up state).

- TimeToTaskDisabled

  This is the amount of time in which the host must complete any host-initiated tasks (e.g., by setting SND or SAS in the Roaming Control Packet). The formula for calculating these times depends on whether the FLEX decoder is in synchronous or asynchronous mode.

  - Synchronous Mode Calculations

  TimeToWarmUpStart $\geq$ (TNF $*$ 80 ms) + (SkippedFrames $*$ 1874.375 ms) + ReceiverOffTime – 167.5 ms

  TImeToTaskDisabled $\geq$ (TNF $*$ 80 ms) + (SkippedFrames $*$ 1874.375 ms) – 247.5 ms

  - Asynchronous mode Calculations

  TimeToWarmUpStart $\geq$ ((TNF – 2) $*$ 80 ms) + ReceiverOffTime

  TImeToTaskDisabled $\geq$ ((TNF – 3) $*$ 80 ms)

  where:

  TNF = Time to Next Frame. This is the value from the Receiver Shutdown Packet.

  SKippedFrames = The number of frames that are not decoded. This can be calculated from the Current Frame (CF) and Next Needed Frame (NAF) fields in the Receiver Shutdown Packet (e.g., If CF is 10 and NAF is 12, then SkippedFrames is 1.

  ReceiverOffTime = The time programmed in the Receiver Off Setting Packet.

3.10.2 Calculating Task Time

Because the TimeToTaskDisabled discussed previously limits how much the host can do while the FLEX decoder is battery saving, it is necessary for the host to know the amount of time needed for the FLEX decoder to perform a task.

The formulas given here calculate the amount of time needed for two types of host-initiated tasks to complete as measured from the last SPI clock of the packet that initiates the task to the time the receiver shutdown sequence begins. Note that the receiver shutdown sequence must begin before tasks are disabled.

The following formula calculates the amount of time needed to complete a noise detection started by setting the SND bit in the Roaming Control Packet. This formula assumes that (1) the noise detection was performed while in synchronous mode, (2) the noise detection was performed in asynchronous mode and did not find the FLEX signal, or (3) the noise detection found the FLEX signal but the DAS bit of the Roaming Control Packet was set.

TimeToPerformNoiseDetect $\leq$ TotalWarmUpTime + 82 ms

where:

TotalWarmUpTime = The sum of the times programmed for the used warm-up steps plus the time programmed for the 3200 sps Sync Setting in the Receiver Control Configuration Packets.

The following formula calculates the amount of time needed to complete an A-word search initiated by setting the SAS bit in the Roaming Control Packet. This formula assumes that the A-word search failed to find the roaming FLEX channel.

TimeToPerformAwardSearch $\leq$ TotalWarmUpTime + AST + 47 ms

where:

TotalWarmUpTime = The sum of the times programmed for the used warm-up steps plus the time programmed for the 3200 sps Sync Setting in the Receiver Control Configuration Packets.

AST = The value configured using the Timing Control Packet.

The following formula calculates the amount of time needed to complete a noise detection/A-word search combination. This can occur when (1) the noise detection is performed while in asynchronous mode, (2) the noise detection finds the FLEX signal, or (3) the DAS bit of the Roaming Control Packet is not set.

TimeToPerformBoth $\leq$ TotalWarmUpTime + AST + 127 ms

where:

TotalWarmUpTime = The sum of the times programmed for the used warm-up steps plus the time programmed for the 3200 sps Sync Setting in the Receiver Control Configuration Packets.

AST = The value configured using the Timing Control Packet.

Appendix A

TLV5590 Data Sheet

This chapter contains a complete data sheet for the TLV5590 converter.

Appendix B

Timing Diagrams

This appendix presents SPI interface timing, start-up timing, and reset timing for the TLV5593VF FLEX roaming decoder.

Topic **Page**

B.1 SPI Timing

Figure B–1 and Table B–1 describe the timing specifications of the SPI interface.

Figure B–1. SPI Interface Timing Specifications

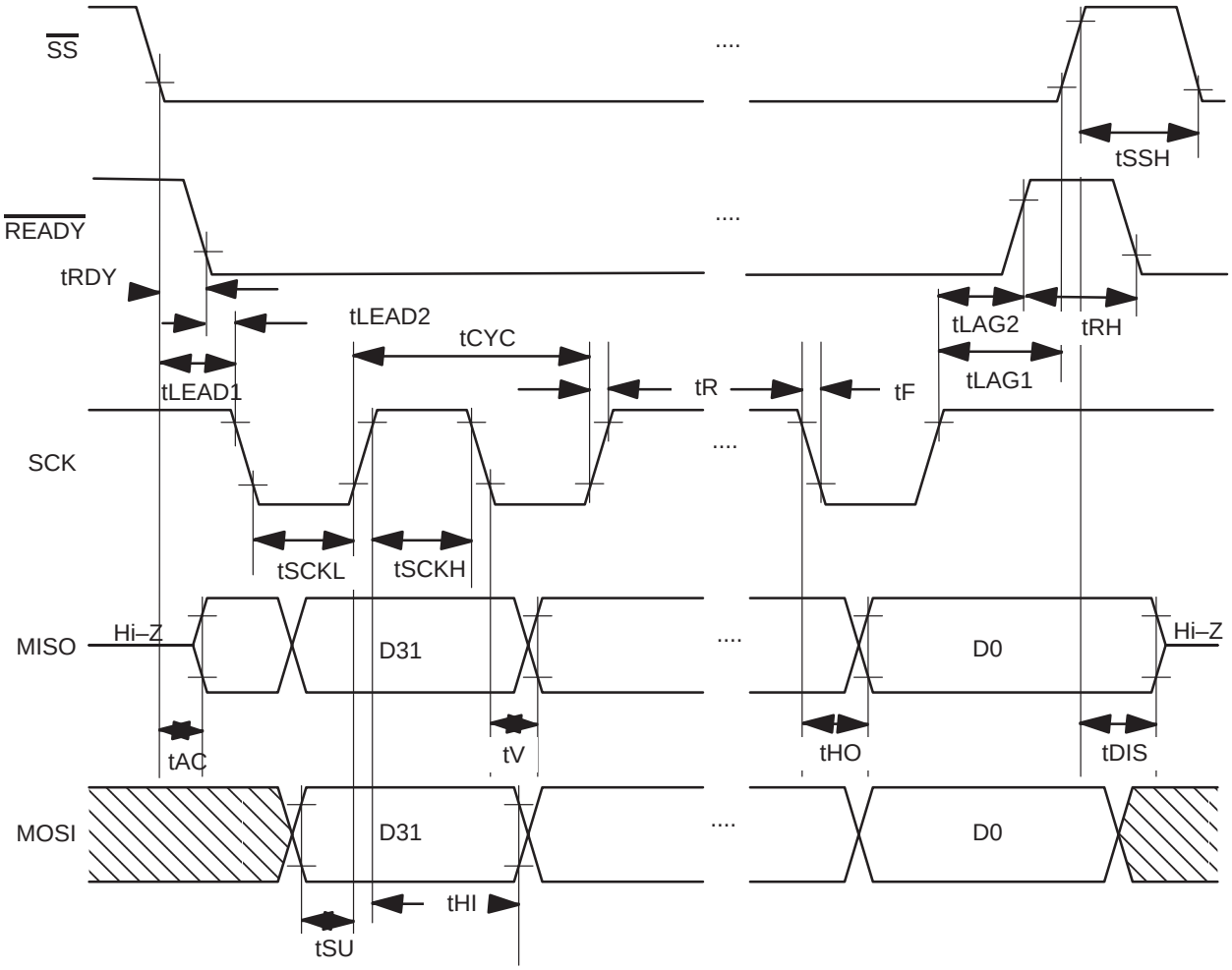


Table B–1.SPI Timing

Characteristic	Conditions	Symbol	Min†	Max†	Unit
Operating Frequency		f_{OP}	dc	1	MHz
Cycle Time		t_{CYC}	1000		ns
Select Lead Time		t_{LEAD1}	200		ns
Deselect Lag Time		t_{LAG1}	200		ns
Select-to-Ready Time	previous packet did not program an address word ‡ CL=50 pf	t_{RDY}		80	µs
Select-to-Ready Time	previous packet programmed an address word ‡ CL=50 pf	t_{RDY}		420	µs
Ready High Time		t_{RH}	50		µs
Ready Lead Time		t_{LEAD2}	200		ns
Not Ready Lag Time	CL=50 pf	t_{LAG2}		200	ns
MOSI Data Setup Time		t_{SU}	200		ns
MOSI Data Hold Time		t_{HI}	200		ns
MISO Access Time	CL=50 pf	t_{AC}	0	200	ns
MISO Disable Time		t_{DIS}		300	ns
MISO Data Valid Time	CL=50 pf	t_V		200	ns
MISO Data Hold Time		t_{HO}	0		ns
$\overline{SS}$ High Time		t_{SSH}	200		ns
SCK High Time		t_{SCKH}	300		ns
SCK Low Time		t_{SCKL}	300		ns
SCK Rise Time	20% to 70% V_{DD}	t_R		1	µs
SCK Fall Time	20% to 70% V_{DD}	t_F		1	µs

† The specifications given in this document indicate the minimum performance level of all FLEX decoders regardless of manufacturer. Individual manufacturers may have better performance than indicated.

‡ When the host reprograms an address word with a Host-to-FLEX decoder packet ID > 127 (decimal), there may be an added delay before the FLEX decoder is ready for another packet.

B.2 Startup Timing

Figure B–2 and Table B–2 describe the timing specifications of the FLEX decoder when power is applied.

Figure B–2. Startup Timing

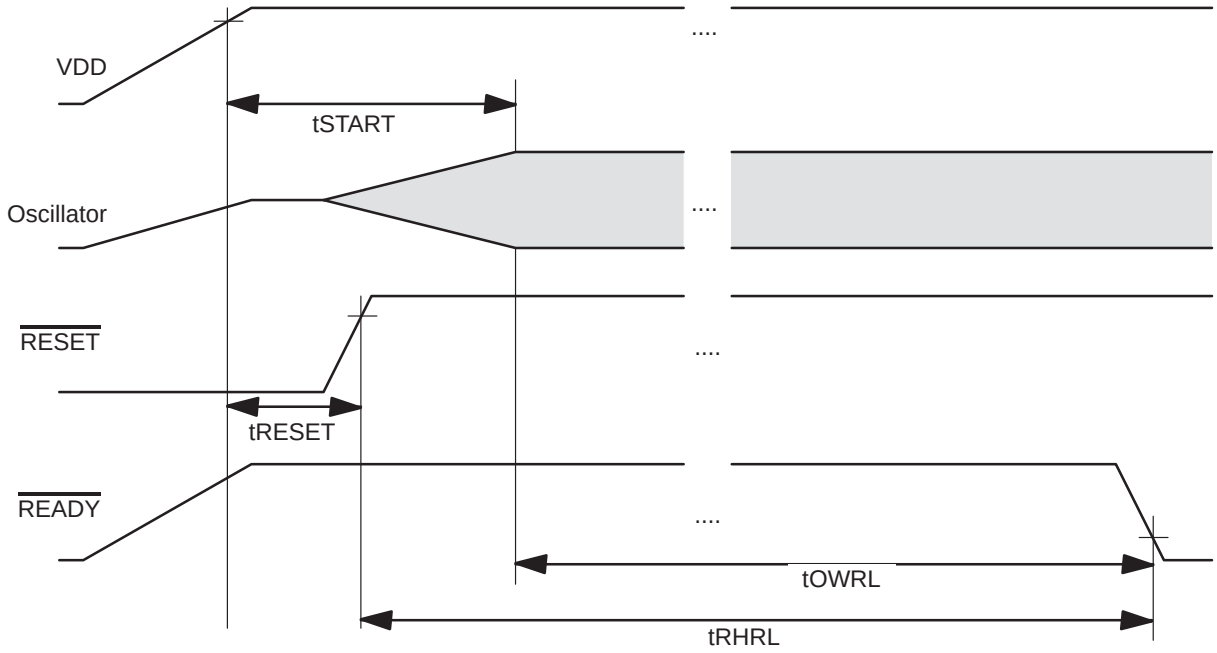


Table B–2. Startup Timing (V_{DD} = 1.8 V to 3.3 V, T_A = 0° C to 70° C)

Characteristic	Conditions	Symbol	Min†	Max†	Unit
Oscillator Startup Time		t_{START}		5	sec
$\overline{\text{RESET}}$ Hold Time		t_{RESET}	200		ns
RESET High to $\overline{\text{READY}}$ Low		t_{RHRL}	76 800	76 800	T‡
Oscillator Warmed Up to $\overline{\text{READY}}$ Low	CL=50 pf	t_{OWRL}	–	1	sec

† The specifications given in this document indicate the minimum performance level of all manufacturers of the FLEX decoder. Individual manufacturers may have better performance than indicated.

‡ T is one period of the 76.8 kHz clock source. Note that from power-up, the oscillator start-up time can impact the availability and period of clock strobes. This can affect the actual $\overline{\text{RESET}}$ high to $\overline{\text{READY}}$ low timing.

B.3 Reset Timing

Figure B–3 and Table B–3 describe the timing specifications of the FLEX decoder when it is reset.

Figure B–3. Reset Timing

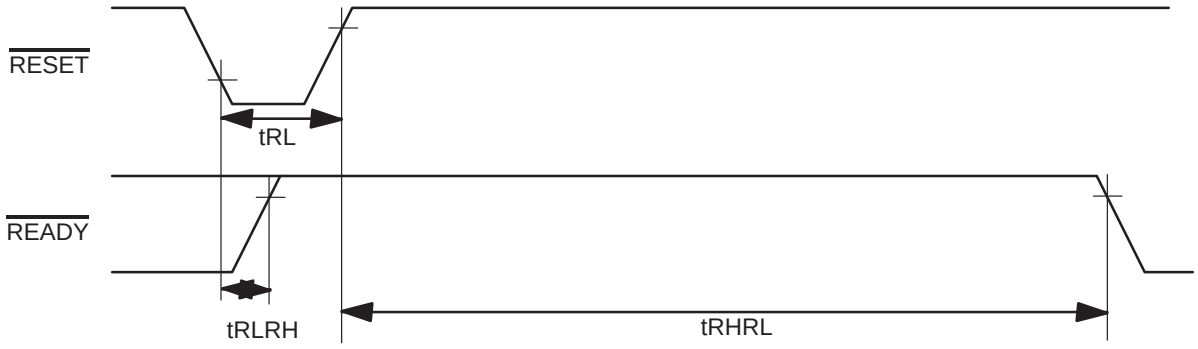


Table B–3. Reset Timing (V_{DD} = 1.8 V to 3.3 V, T_A = 0° C to 70° C)

Characteristic	Conditions	Symbol	Min†	Max†	Unit
$\overline{\text{RESET}}$ Pulse Width		t_{RL}	200	–	ns
$\overline{\text{RESET}}$ Low to $\overline{\text{READY}}$ High		t_{RLRH}	–	200	ns
$\overline{\text{RESET}}$ High to $\overline{\text{READY}}$ Low	Stable 76.8 kHz clock source	t_{RHRL}	–	1	sec

† The specifications given in this document indicate the minimum performance level of all manufacturers of the FLEX decoder. Individual manufacturers may have better performance than indicated.

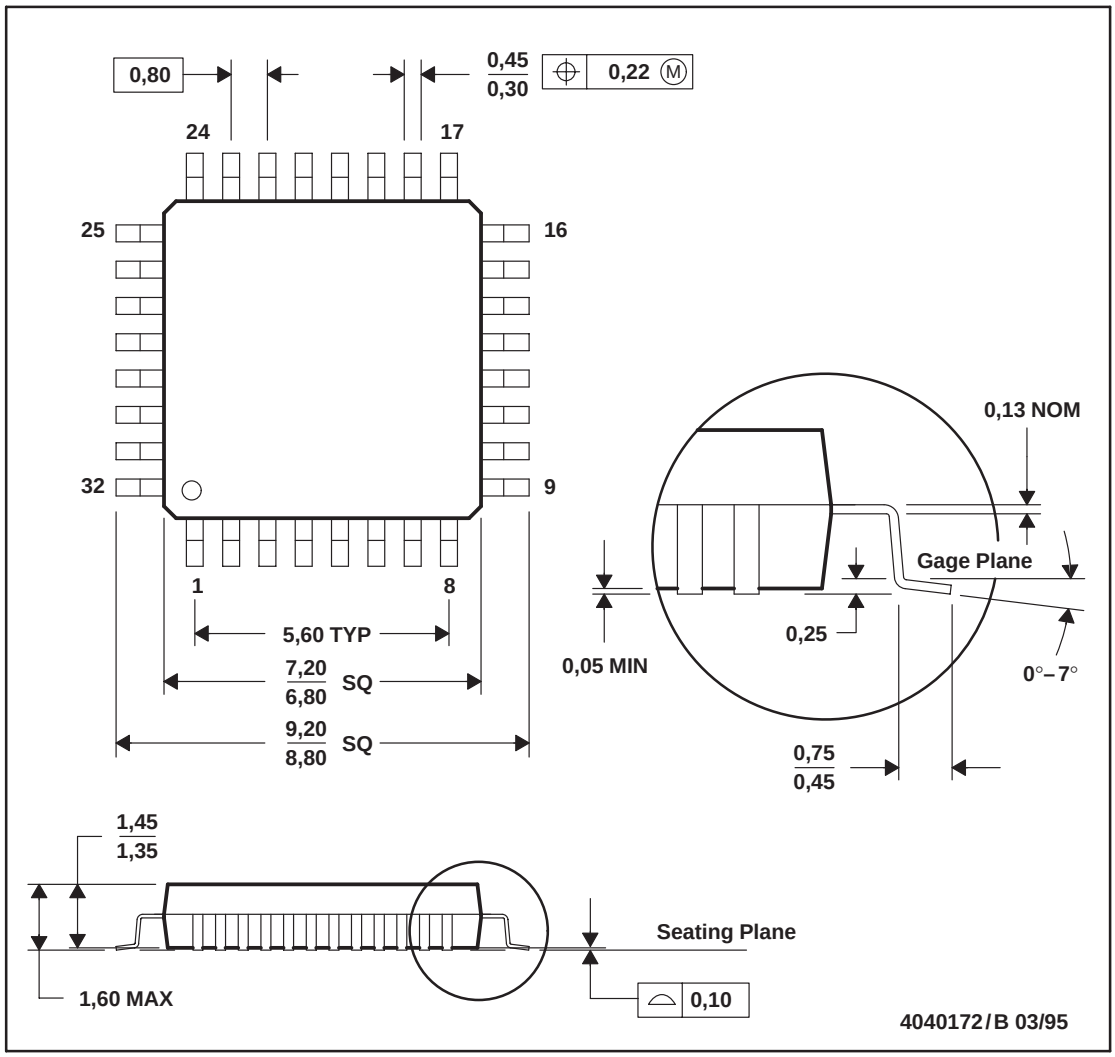
Appendix C

Mechanical Data

This appendix presents the mechanical data for the TLV5593VF FLEX roaming decoder.

Plastic Quad Flatpack

VF (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136