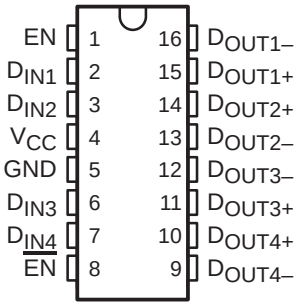
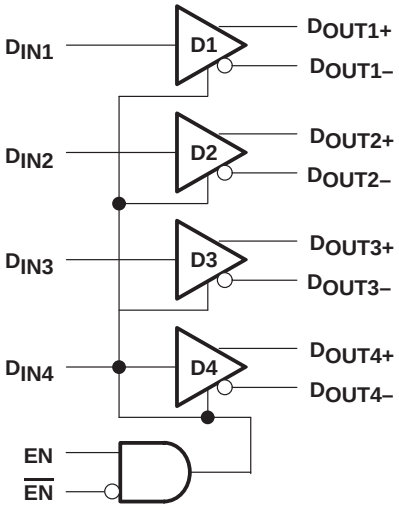
- **>400 Mbps (200 MHz) Signaling Rates**
- **Flow-Through Pinout Simplifies PCB Layout**
- **300 ps Maximum Differential Skew**
- **Propagation Delay Times 1.8 ns (Typical)**
- **3.3 V Power Supply Design**
- **±350 mV Differential Signaling**
- **High Impedance on LVDS Outputs on Power Down**
- **Conforms to TIA/EIA-644 LVDS Standard**
- **Industrial Operating Temperature Range (–40°C to 85°C)**
- **Available in SOIC and TSSOP Packages**

D OR PW PACKAGE
(TOP VIEW)



functional block diagram



description

The SN65LVDS047 is a quad differential line driver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of this device and signaling technique is for point-to-point and multidrop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

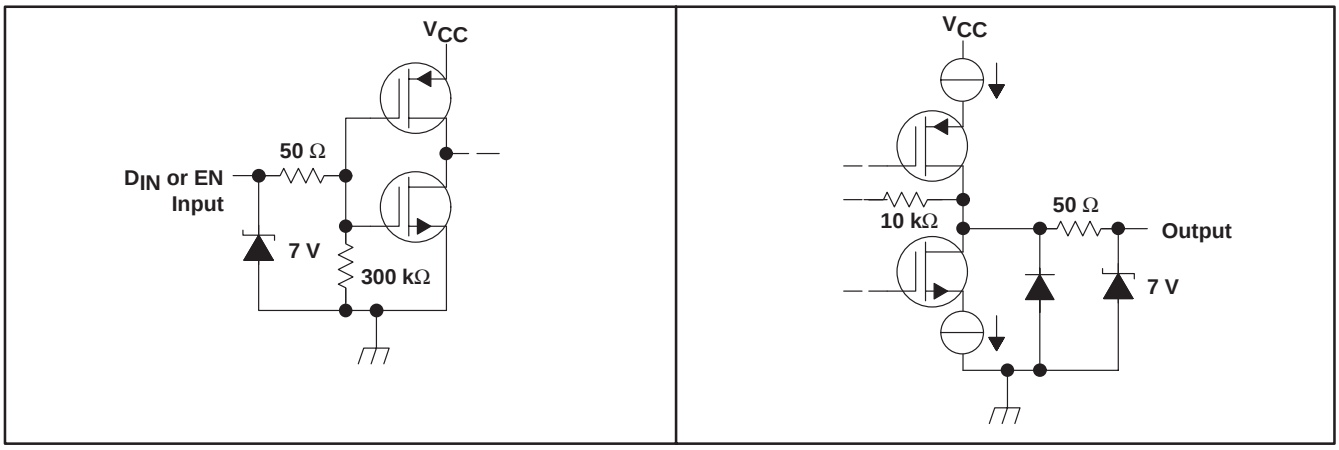
The SN65LVDS047 is characterized for operation from –40°C to 85°C.

TRUTH TABLE

INPUT	ENABLES		OUTPUTS	
D_{IN}	EN	$\overline{EN}$	D_{OUT+}	D_{OUT-}
L	H	L or OPEN	L	H
H			H	L
X	All other conditions		Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (see Note 1) (unless otherwise noted)†

Supply voltage (V_{CC}) . . . . . –0.3 V to 4 V
Input voltage range, $V_I(D_{IN})$ . . . . . –0.3 V to (V_{CC} +0.3 V)
Enable input voltage (EN, $\overline{EN}$) . . . . . –0.3 V to (V_{CC} +0.3 V)
Output voltage, $V_O(D_{OUT+}, D_{OUT-})$ . . . . . –0.3 V to 3.9 V
Electrostatic discharge, (see Note 2) . . . . . >10 kV
Short circuit duration (D_{OUT+},(D_{OUT-}) . . . . . Continuous
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Operating free-air temperature, T_A	–40	25	85	°C

electrical characteristics over recommended operating free-air temperature range (see Notes 3, 4) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OD}	Differential output voltage	R_L = 100 Ω (see Figure 1)	250	310	450	mV
$\Delta\|V_{OD}\|$	Change in magnitude of V_{OD} for complementary output states			1	35	|mV|
$V_{OC(SS)}$	Steady-state, common-mode output voltage		1.125	1.17	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			1	25	|mV|
V_{OH}	Output high voltage			1.33	1.6	V
V_{OL}	Output low voltage		0.90	1.02		V
V_{IH}	Input high voltage		2		V_{CC}	V
V_{IL}	Input low voltage		GND		0.8	V
I_{IH}	Input high current	V_{IN} = V_{CC} or 2.5 V	–10	3	10	μA
I_{IL}	Input low current	V_{IN} = GND or 0.4 V	–10	1	10	μA
V_{IK}	Input clamp voltage	I_{CL} = –18 mA	–1.5	–0.8		V
I_{OS}	Output short circuit current (see Note 5)	Enabled, D_{IN} = V_{CC}, D_{OUT+} = 0 V or D_{IN} = GND, $D_{OUT–}$ = 0 V		–3.1	–9	mA
I_{OSD}	Differential output short circuit current (see Note 5)	Enabled, V_{OD} = 0 V			–9	mA
I_{OFF}	Power-off leakage	V_O = 0 V or 3.6 V, V_{CC} = 0 V or Open	–1		1	μA
I_{OZ}	Output 3-state current	EN = 0.8 V and $\overline{EN}$ = 2 V, V_O = 0 V or V_{CC}	–1		1	μA
I_{CC}	No load supply current, drivers enabled	D_{IN} = V_{CC} or GND		7		mA
I_{CCL}	Loaded supply current, drivers enabled	R_L = 100 Ω all channels, D_{IN} = V_{CC} or GND (all inputs)		20	26	mA
$I_{CC(Z)}$	No load supply current, drivers disabled	D_{IN} = V_{CC} or GND, EN = GND, $\overline{EN}$ = V_{CC}		0.5	1.3	mA

† All typical values are given for: V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 3. Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.

4. The SN65LVDS047 is a current mode device and only functions within data sheet specifications when a resistive load is applied to the driver outputs, 90 Ω to 110 Ω typical range.

5. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

switching characteristics over recommended operating conditions (see Notes 6, 7, and 12) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Differential propagation delay, high-to-low	R_L = 100 Ω,, C_L = 15 pF (see Figures 2 and 3)	1.4	1.8	2.8	ns
t_{PLH}	Differential propagation delay, low-to-high		1.4	1.8	2.8	ns
$t_{SK(p)}$	Differential pulse skew ($t_{PHLD} – t_{PLHD}$) (see Note 8)			50	300	ps
$t_{SK(o)}$	Channel-to–channel skew (see Note 9)			40	300	ps
$t_{SK(pp)}$	Differential part-to-part skew (see Note 10)				1	ns
$t_{SK(lim)}$	Differential part-to-part skew (see Note 11)				1.2	ns
t_r	Rise time			0.5	1.5	ns
t_f	Fall time			0.5	1.5	ns
t_{PHZ}	Disable time high to Z	R_L = 100 Ω,, C_L = 15 pF (see Figures 4 and 5)		5.5	8	ns
t_{PLZ}	Disable time low to Z			5.5	8	ns
t_{PZH}	Enable time Z to high			8.5	12	ns
t_{PZL}	Enable time Z to low			8.5	12	ns
$f_{(MAX)}$	Maximum operating frequency (see Note 13)			250		MHz

† All typical values are given for: V_{CC} = 3.3 V, T_A = 25°C.

NOTES:
6. Generator waveform for all tests unless otherwise: f = 1 MHz, Z_O = 50 Ω, t_r < 1 ns, and t_f < 1 ns.
7. C_L includes probe and jig capacitance.
8. $t_{SK(p)}|t_{PHL}–t_{PLH}|$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
9. $t_{SK(o)}$ is the differential channel-to-channel skew of any event on the same device.
10. $t_{SK(pp)}$ is the differential part-to-part skew, and is defined as the difference between the minimum and the maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
11. $t_{SK(lim)}$ part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. $t_{SK(lim)}$ is defined as |Min – Max| differential propagation delay.
12. All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.
13. $f_{(MAX)}$ generator input conditions: $t_r = t_f$ < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% to 55%, V_{OD} > 250 mV, all channels switching

PARAMETER MEASUREMENT INFORMATION

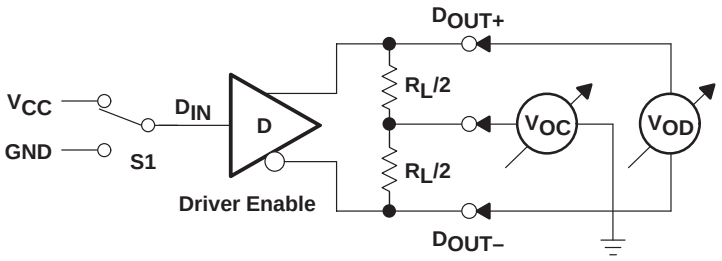


Figure 1. Driver V_{OD} and V_{OC} Test Circuit

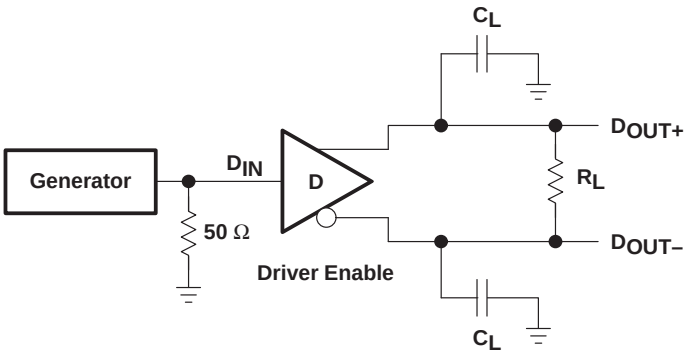


Figure 2. Driver Propagation Delay and Transition Time Test Circuit

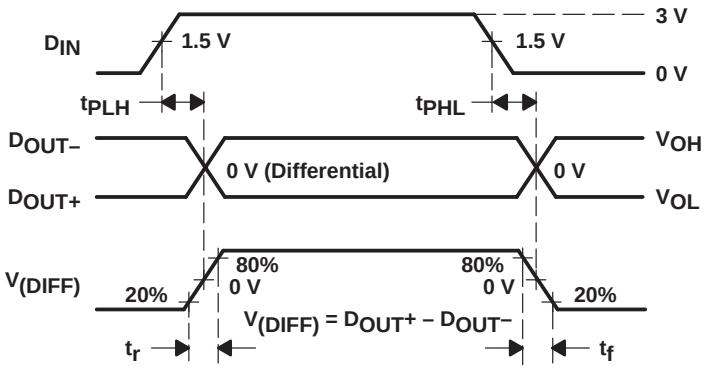


Figure 3. Driver Propagation Delay and Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION

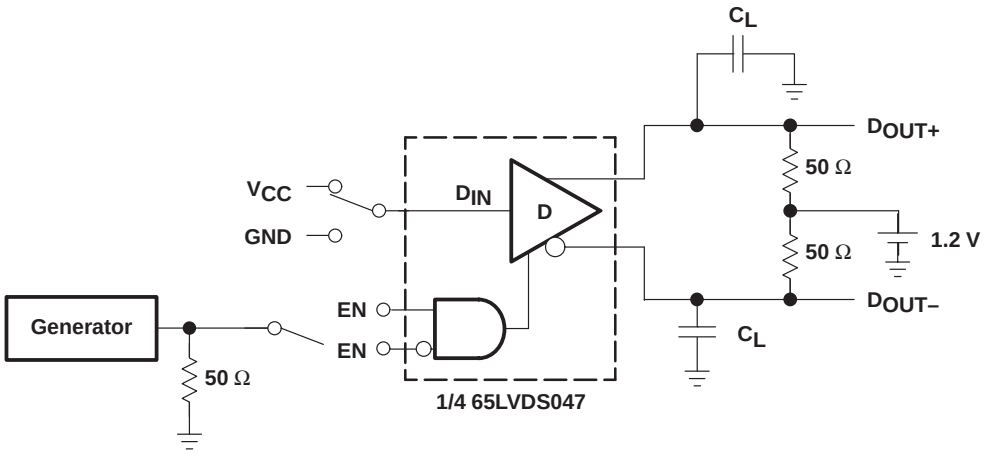


Figure 4. Driver 3-State Delay Test Circuit

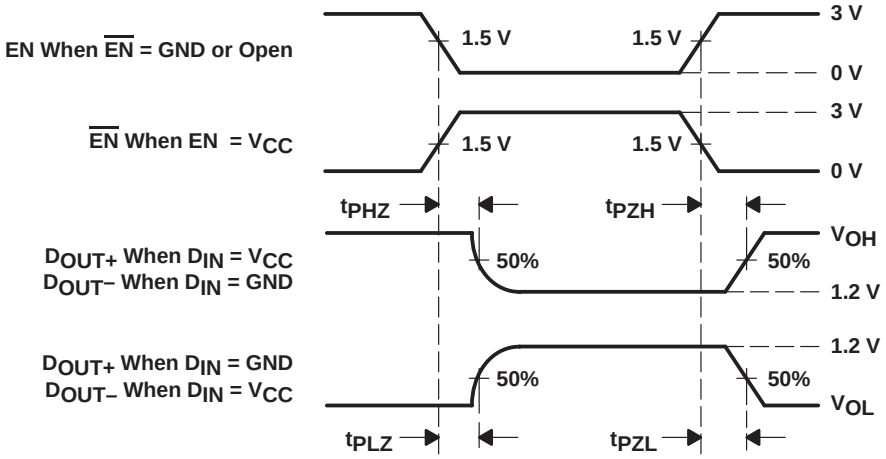


Figure 5. Driver 3-State Delay Waveform

TYPICAL CHARACTERISTICS

OUTPUT HIGH VOLTAGE vs POWER SUPPLY VOLTAGE

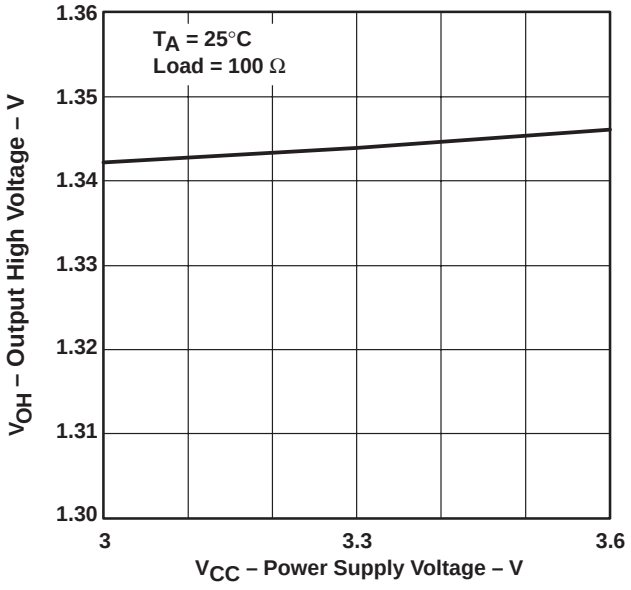


Figure 6

OUTPUT LOW VOLTAGE vs POWER SUPPLY VOLTAGE

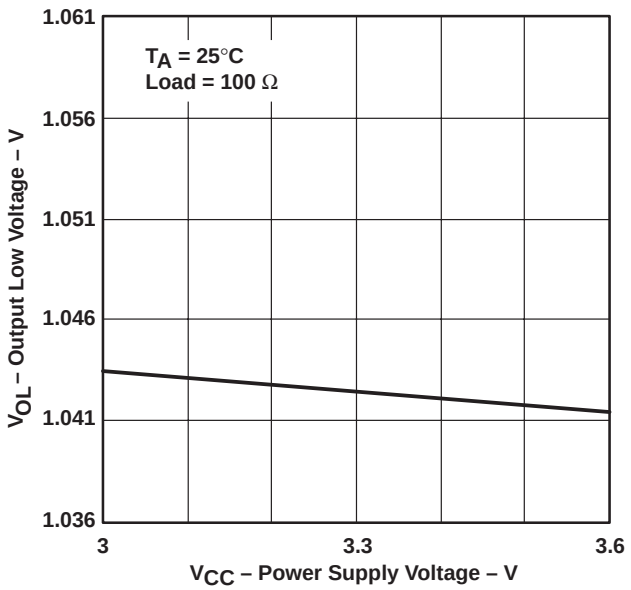


Figure 7

OUTPUT SHORT CIRCUIT CURRENT vs POWER SUPPLY VOLTAGE

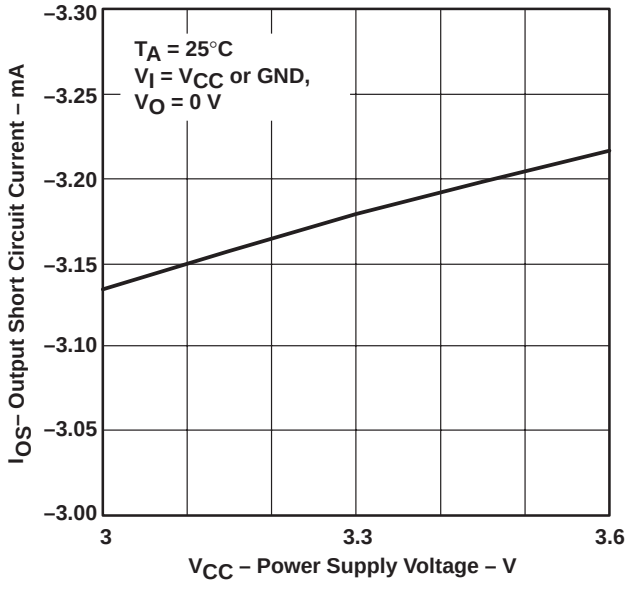


Figure 8

DIFFERENTIAL OUTPUT VOLTAGE vs POWER SUPPLY VOLTAGE

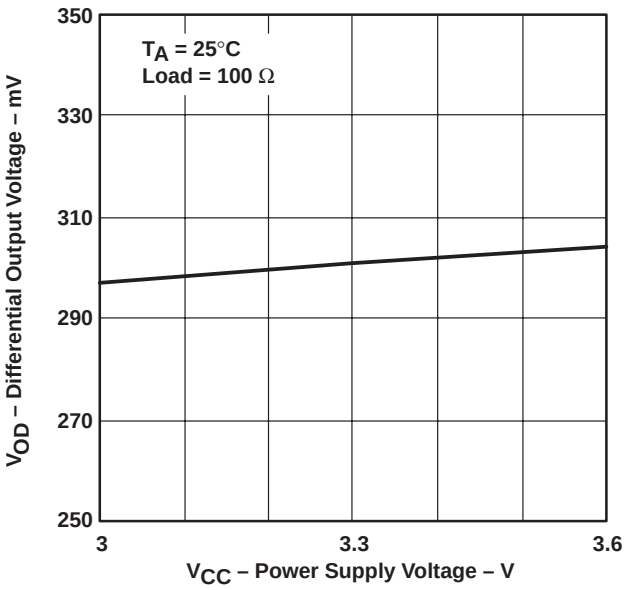


Figure 9

TYPICAL CHARACTERISTICS

COMMON-MODE OUTPUT VOLTAGE vs POWER SUPPLY VOLTAGE

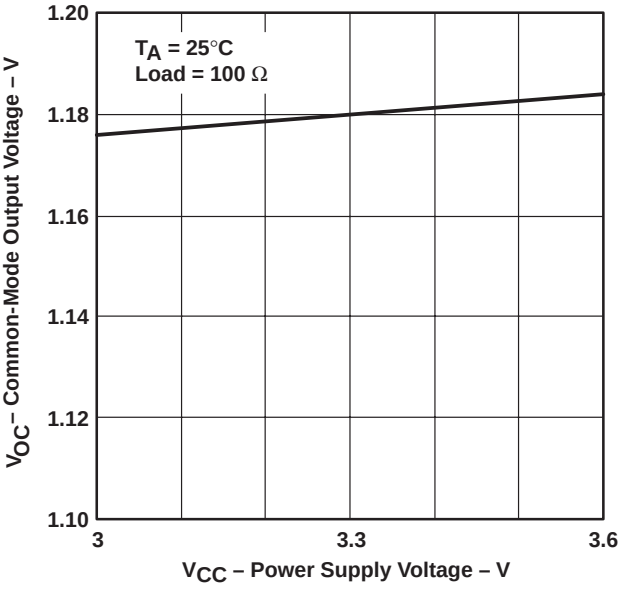


Figure 10

POWER SUPPLY CURRENT vs FREQUENCY

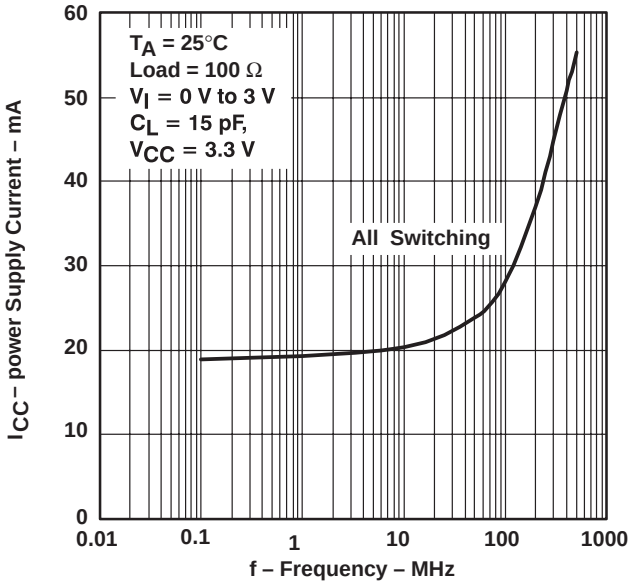
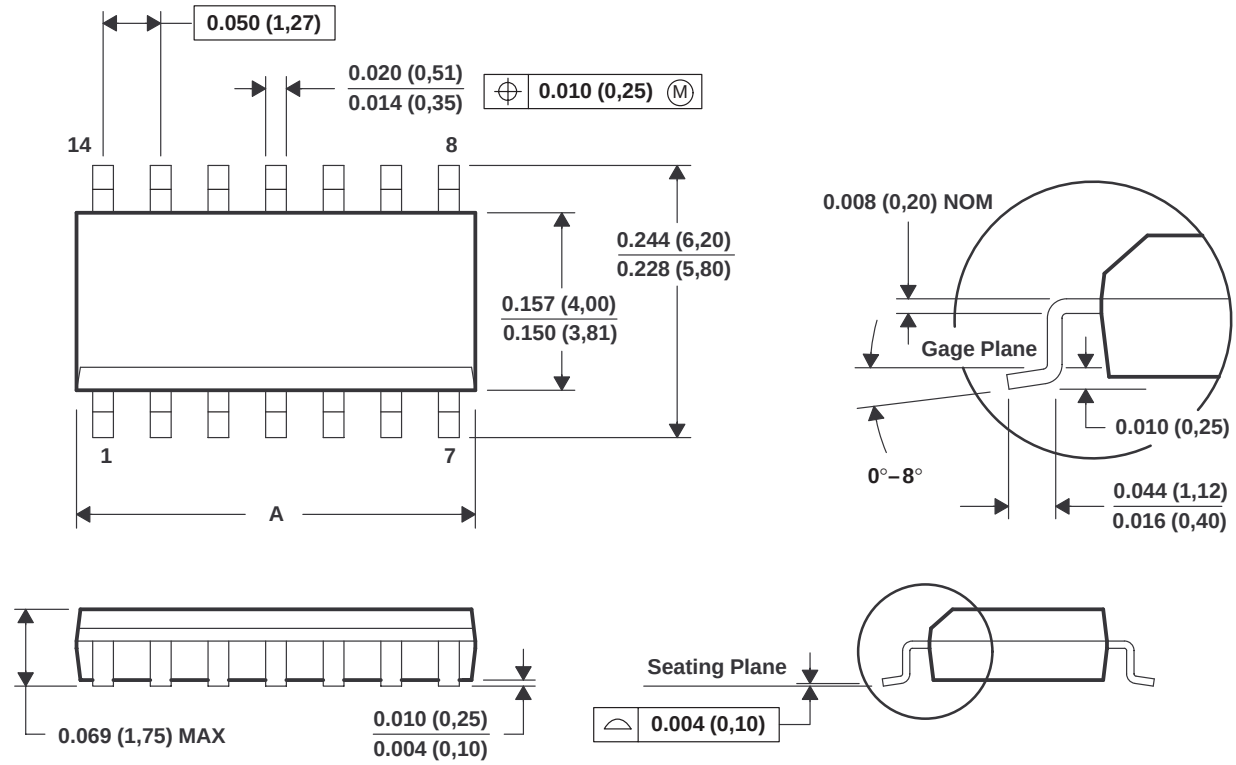


Figure 11

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

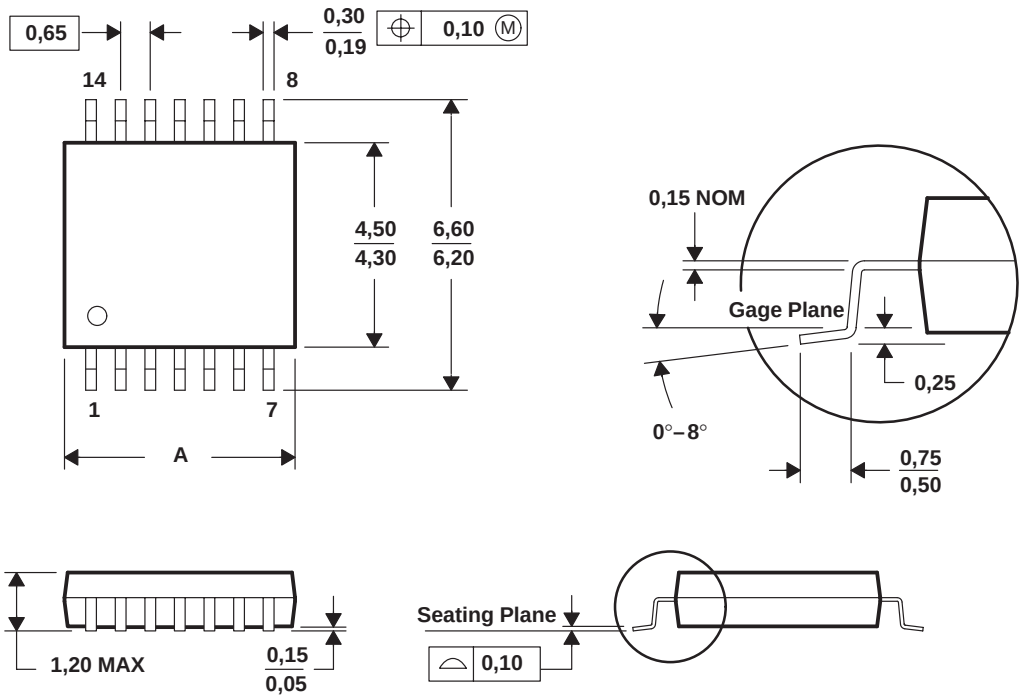
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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