

- 28:4 Data Channel Compression at up to 1.82 Gigabits per Second Throughput
- Suited for Point-to-Point Subsystem Communication With Very Low EMI
- 28 Data Channels Plus Clock in Low-Voltage TTL and 4 Data Channels Plus Clock Out Low-Voltage Differential
- Selectable Rising or Falling Clock Edge Triggered Inputs
- Bus Pins Tolerate 6-kV HBM ESD
- Operates From a Single 3.3-V Supply and 250 mW (Typ)
- 5-V Tolerant Data Inputs
- Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch
- Consumes <1 mW When Disabled
- Wide Phase-Lock Input Frequency Range 20 MHz to 65 MHz
- No External Components Required for PLL
- Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
- Industrial Temperature Qualified
 $T_A = -40^{\circ}\text{C}$ to 85°C
- Replacement for the DS90CR285

DGG PACKAGE
(TOP VIEW)

V _{CC}	1	56	D4
D5	2	55	D3
D6	3	54	D2
D7	4	53	GND
GND	5	52	D1
D8	6	51	D0
D9	7	50	D27
D10	8	49	LVDSGND
V _{CC}	9	48	Y1M
D11	10	47	Y1P
D12	11	46	Y2M
D13	12	45	Y2P
GND	13	44	LVDSV _{CC}
D14	14	43	LVDSGND
D15	15	42	Y3M
D16	16	41	Y3P
CLKSEL	17	40	CLKOUTM
D17	18	39	CLKOUTP
D18	19	38	Y4M
D19	20	37	Y4P
GND	21	36	LVDSGND
D20	22	35	PLL _{GND}
D21	23	34	PLL _{V_{CC}}
D22	24	33	PLL _{GND}
D23	25	32	SHTDN
V _{CC}	26	31	CLKIN
D24	27	30	D26
D25	28	29	GND

description

The SN65LVDS93 LVDS serdes (serializer/deserializer) transmitter contains four 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and five low-voltage differential signaling (LVDS) drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTTL data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN65LVDS94.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected via the clock select (CLKSEL) pin. The frequency of CLKIN is multiplied seven times and then used to serially unload the data registers in 7-bit slices. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN65LVDS93 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a low-level input and the possible use of the shutdown/clear (SHTDN). SHTDN is an active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers at a low level.

The SN65LVDS93 is characterized for operation over ambient air temperatures of -40°C to 85°C .



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**TEXAS
INSTRUMENTS**

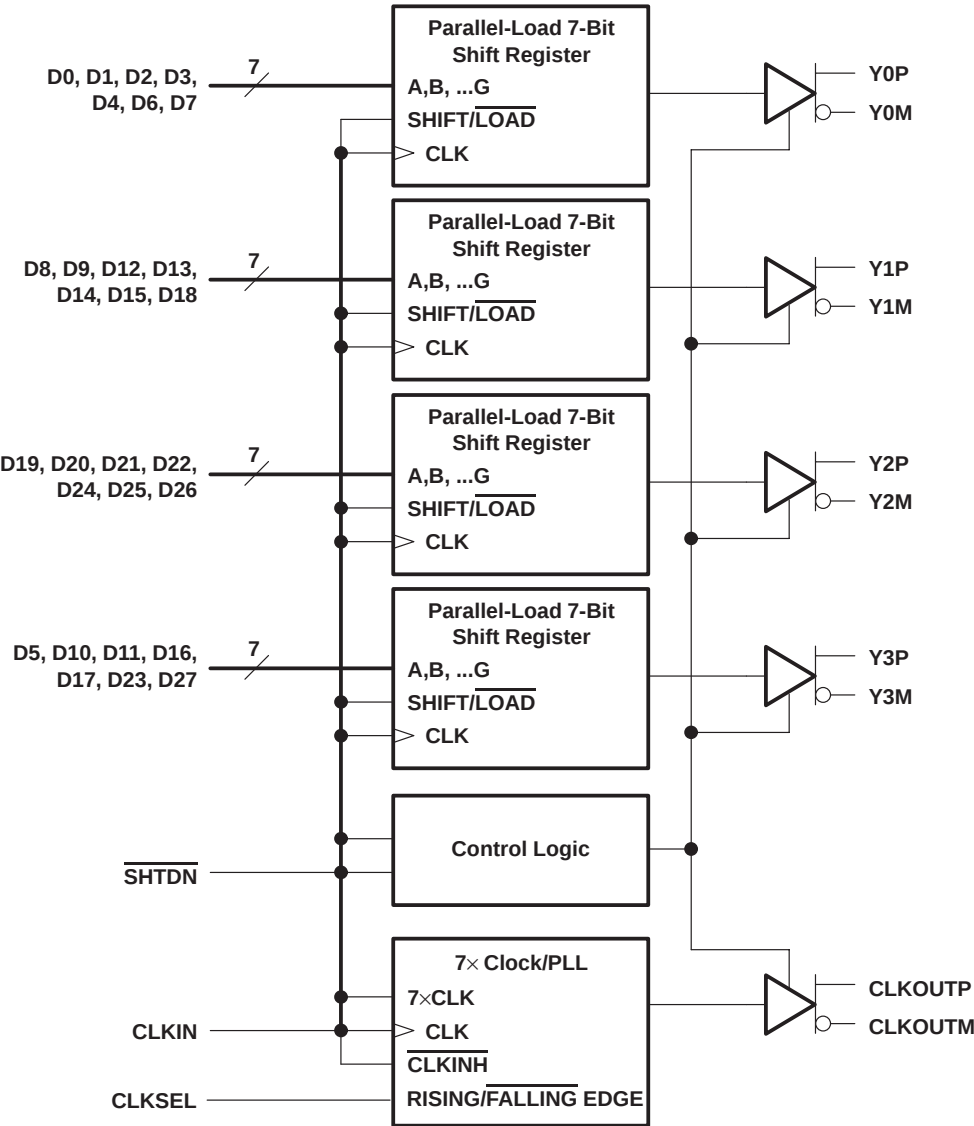
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SN65LVDS93
LVDS SERDES TRANSMITTER

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functional block diagram



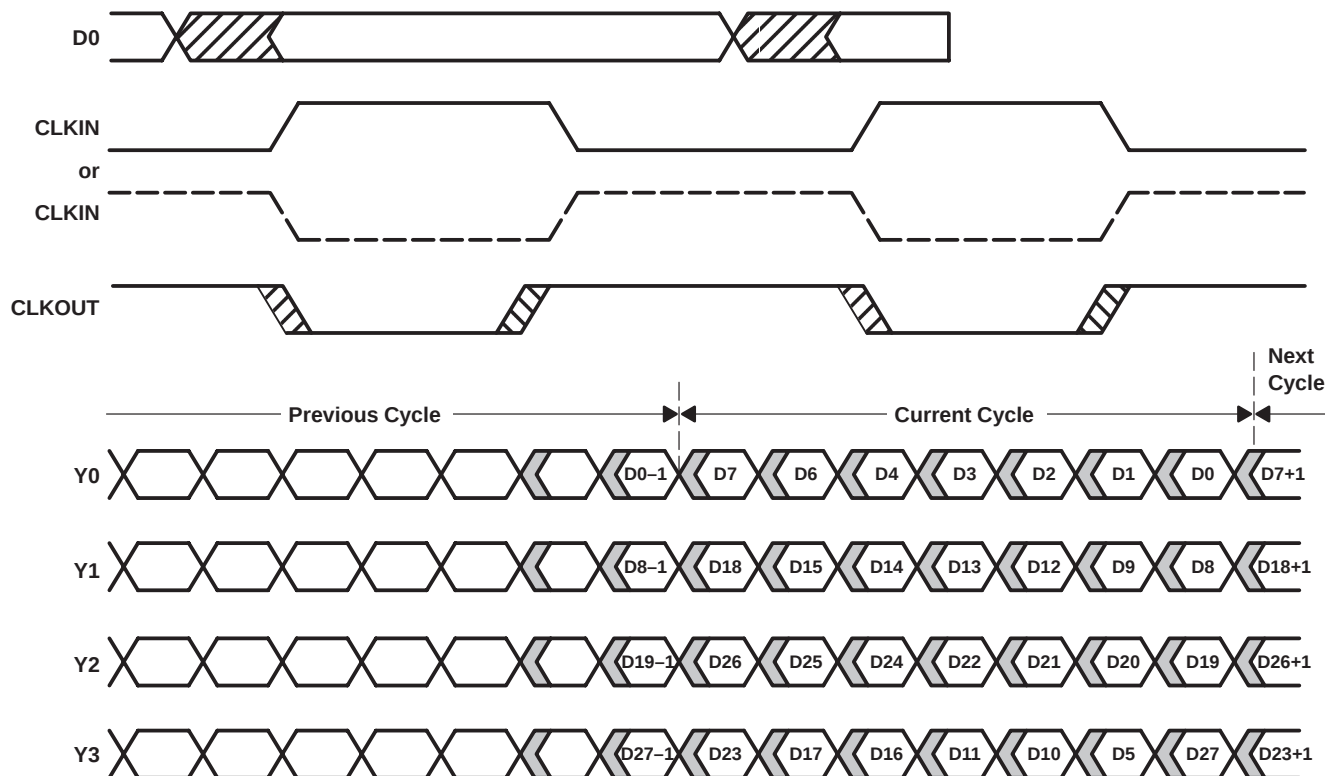
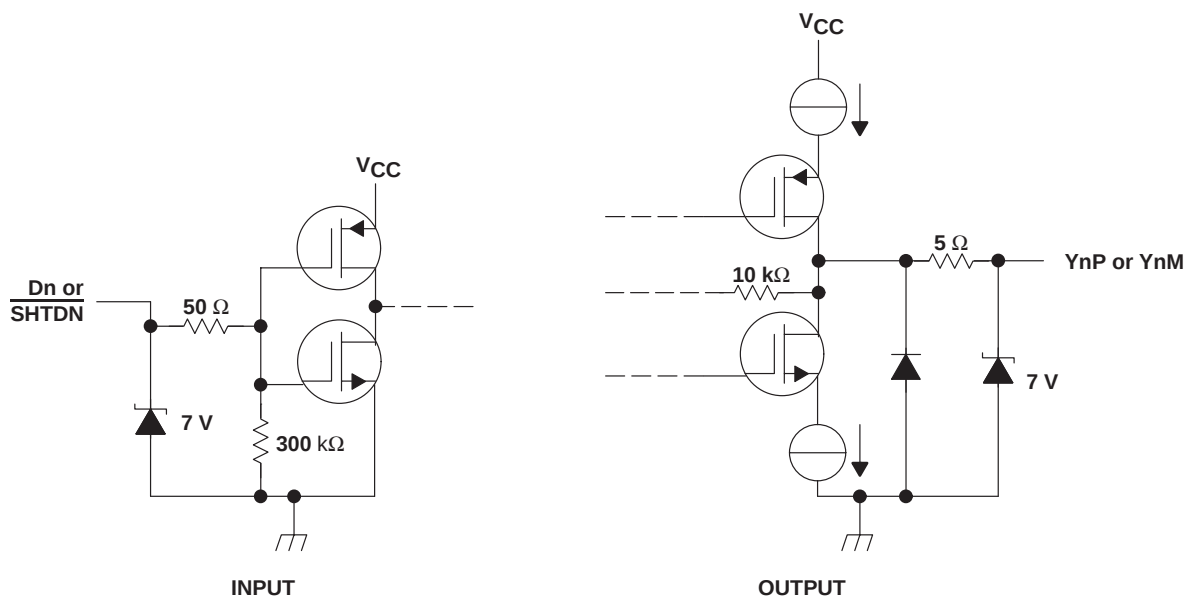


Figure 1. Typical 'LVDS93 Load and Shift Sequences

equivalent input and output schematic diagrams



SN65LVDS93

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 4 V
Voltage range at any output terminal, V_O	–0.5 V to $V_{CC} + 0.5$ V
Voltage range at any input terminal, V_I	–0.5 V to 5.5 V
Electrostatic discharge (see Note 2):	
Bus Pins (Class 3A)	6 kV
Bus Pins (Class 2B)	400 V
Bus Pins (Class 2A)	6 kV
Bus Pins (Class 2B)	200 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. This rating is measured using MIL-STD-883C Method, 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGG	1377 mW	11 mW/°C	882 mW	717 mW

[‡] This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Differential load impedance, Z_L	90		132	Ω
Operating free-air temperature, T_A	–40		85	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_T Input voltage threshold			1.4		V
$ V_{OD} $ Differential steady-state output voltage magnitude	$R_L = 100\ \Omega$, See Figure 3	247		454	mV
$\Delta V_{OD} $ Change in the steady-state differential output voltage magnitude between opposite binary states				50	mV
$V_{OC(SS)}$ Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$V_{OC(PP)}$ Peak-to-peak common-mode output voltage				150	mV
I_{IH} High-level input current	$V_{IH} = V_{CC}$			20	μA
I_{IL} Low-level input current	$V_{IL} = 0\ V$			± 10	μA
I_{OS} Short-circuit output current	$V_{OY} = 0\ V$			± 24	mA
	$V_{OD} = 0\ V$			± 12	mA
I_{OZ} High-impedance state output current	$V_O = 0\ V$ to V_{CC}			± 20	μA
$I_{CC(AVG)}$ Quiescent current (average)	Disabled, All inputs at GND			350	μA
	Enabled, $R_L = 100\ \Omega$ (5 places), Worst-case pattern (see Figure 4), $t_C = 15.38\ ns$		95	120	mA
C_i Input capacitance			3		pF

[†] All typical values are at $V_{CC} = 3.3\ V$, $T_A = 25^\circ C$.

timing requirements

	MIN	NOM	MAX	UNIT
t_C Input clock period	15.4	t_C	50	ns
t_W High-level input clock pulse width duration	$0.4t_C$		$0.6t_C$	ns
t_t Input signal transition time			5	ns
t_{su} Data setup time, D0 through D27 before $CLKIN\uparrow$ or $CLKIN\downarrow$ (See Figure 2)	3			ns
t_h Data hold time, D0 through D27 after $CLKIN\downarrow$ or $CLKIN\uparrow$ (See Figure 2)	1.5			ns

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switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t ₀ Delay time, CLKOUT↑ to serial bit position 0	t _C = 15.38 ns (±0.2%), Input clock jitter < 50 ps [‡] , See Figure 5	-0.20	0	0.20	ns
t ₁ Delay time, CLKOUT↑ to serial bit position 1		$\frac{1}{7}t_C - 0.20$	$\frac{1}{7}t_C + 0.20$		ns
t ₂ Delay time, CLKOUT↑ serial bit position 2		$\frac{2}{7}t_C - 0.20$	$\frac{2}{7}t_C + 0.20$		ns
t ₃ Delay time, CLKOUT↑ serial bit position 3		$\frac{3}{7}t_C - 0.20$	$\frac{3}{7}t_C + 0.20$		ns
t ₄ Delay time, CLKOUT↑ to serial bit position 4		$\frac{4}{7}t_C - 0.20$	$\frac{4}{7}t_C + 0.20$		ns
t ₅ Delay time, CLKOUT↑ to serial bit position 5		$\frac{5}{7}t_C - 0.20$	$\frac{5}{7}t_C + 0.20$		ns
t ₆ Delay time, CLKOUT↑ to serial bit position 6		$\frac{6}{7}t_C - 0.20$	$\frac{6}{7}t_C + 0.20$		ns
t _{sk(o)} Output skew, t _n - $\frac{n}{7}t_C$		-0.20		0.20	ns
t ₇ Delay time, CLKIN↓ or CLKIN↑ to CLKOUT↑	t _C = 15.38 ns (±0.2%), Input clock jitter < 50 ps [‡] , See Figure 5		4.2		ns
t _{C(o)} Output clock period			t _C		ps
Δt _{C(o)} Output clock cycle-to-cycle jitter [§]	t _C = 15.38 ns + 0.75sin(2π500E3t) ± 0.05 ns, See Figure 6		±80		ps
	t _C = 15.38 ns + 0.75sin(2π3E6t) ± 0.05 ns, See Figure 6		±300		ns
t _W High-level output clock pulse duration			$\frac{4}{7}t_C$		ps
t _t Differential output voltage transition time (t _r or t _f)	See Figure 3	260	700	1500	ps
t _{en} Enable time, SHTDN↑ to phase lock (Y _n valid)	See Figure 7		1		ms
t _{dis} Disable time, SHTDN↓ to off-state (CLKOUT low)	See Figure 8		250		ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

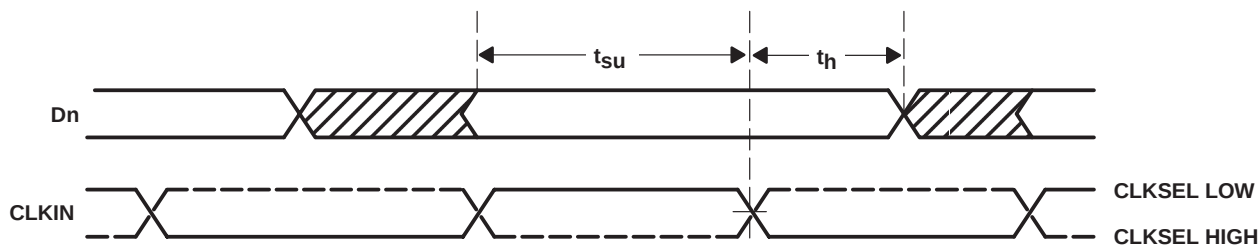
[‡] Input clock jitter is the magnitude of the charge in the input clock period

[§] The output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.



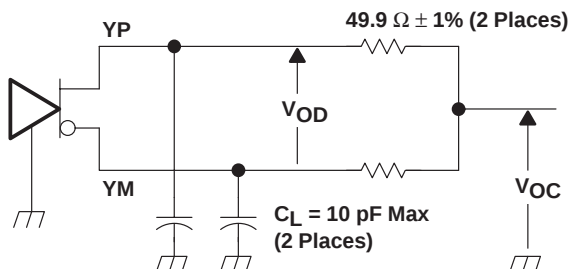
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PARAMETER MEASUREMENT INFORMATION



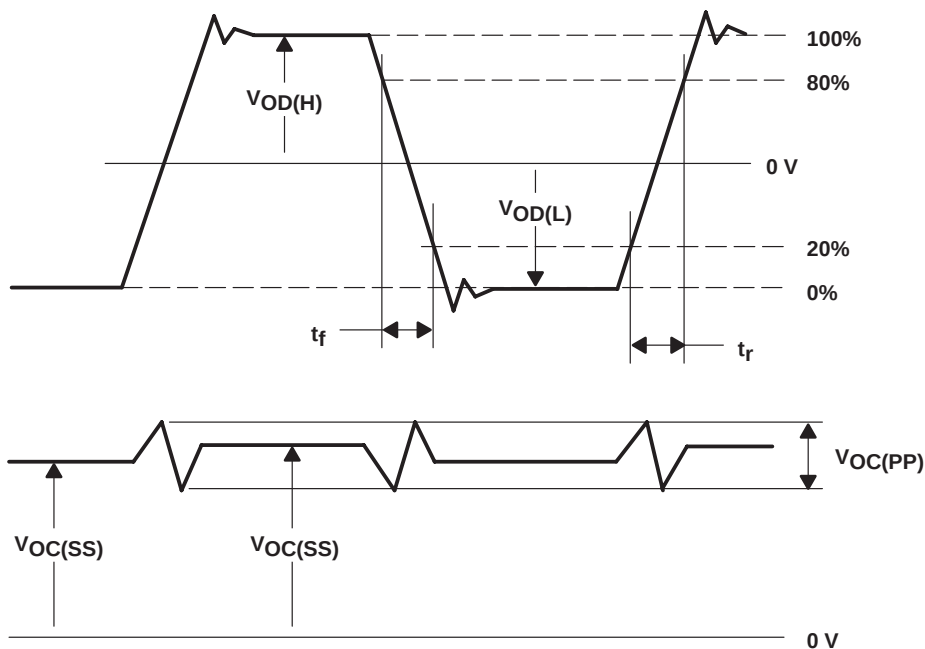
NOTE: All input timing is defined at 1.4 V on an input signal with a 10% to 90% rise or fall time of less than 5 ns.

Figure 2. Setup and Hold Time Definition



NOTE A: The lumped instrumentation capacitance for any single-ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output is similarly loaded.

(a) SCHEMATIC



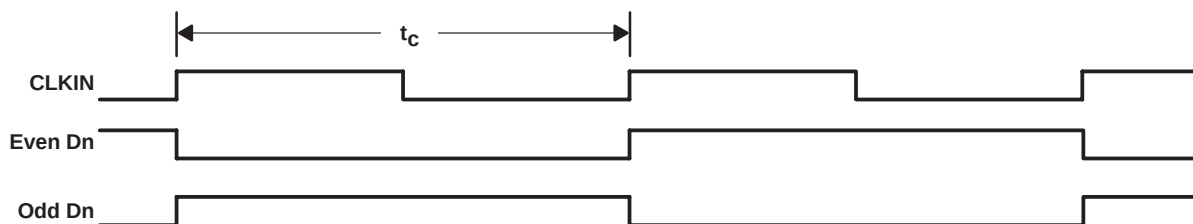
(b) WAVEFORMS

Figure 3. Test Load and Voltage Definitions for LVDS Outputs

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PARAMETER MEASUREMENT INFORMATION



NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs. Pattern with CLKSEL low shown.

Figure 4. Worst-Case Test Pattern (CLKSEL low shown)

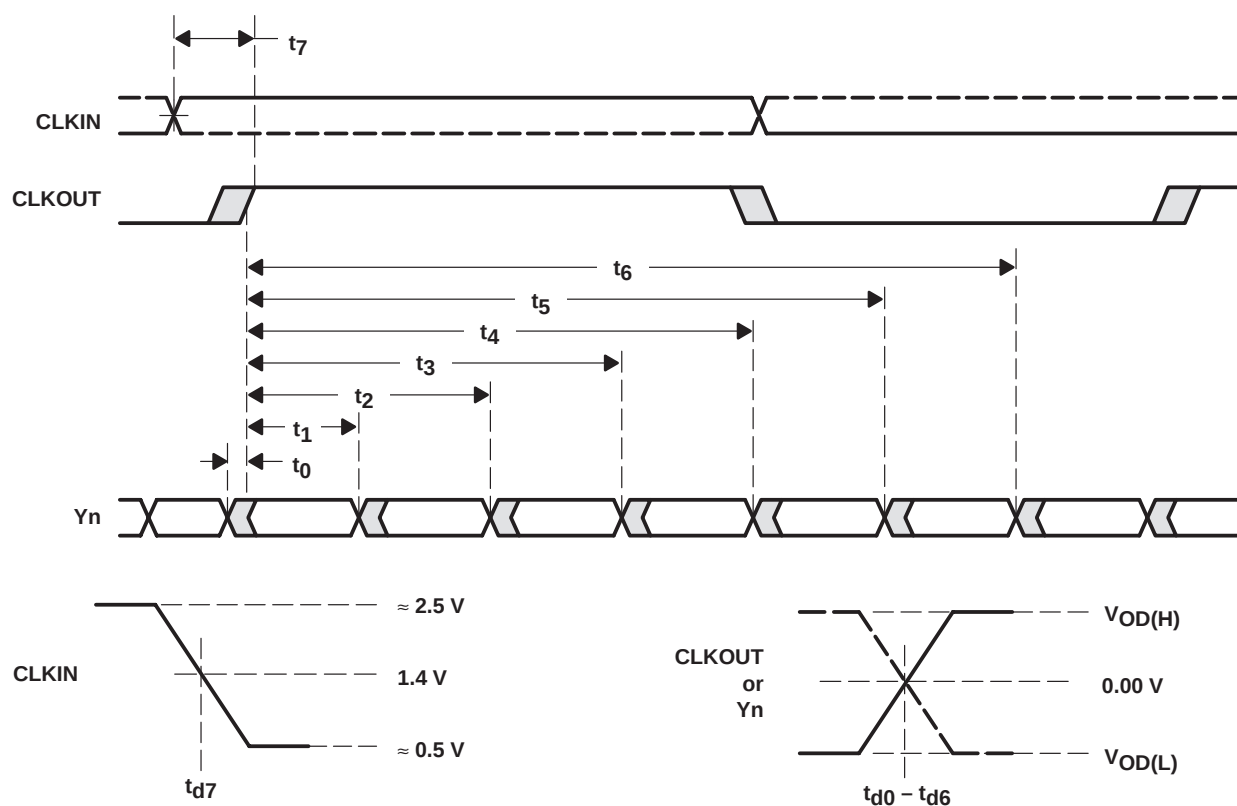


Figure 5. Timing Definitions

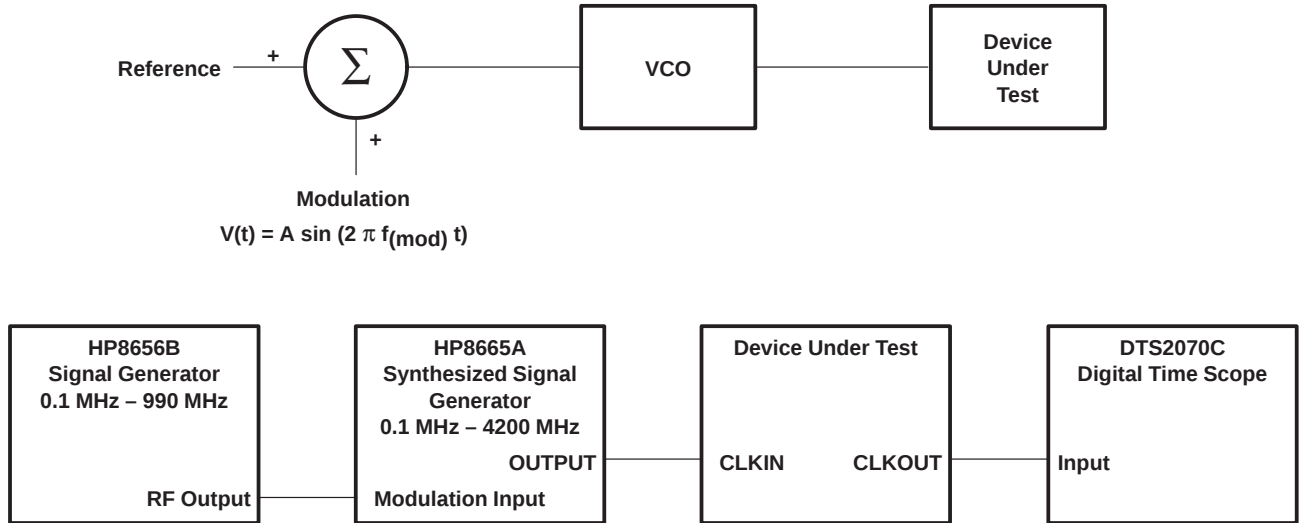


Figure 6. Output Clock Jitter Test Setup

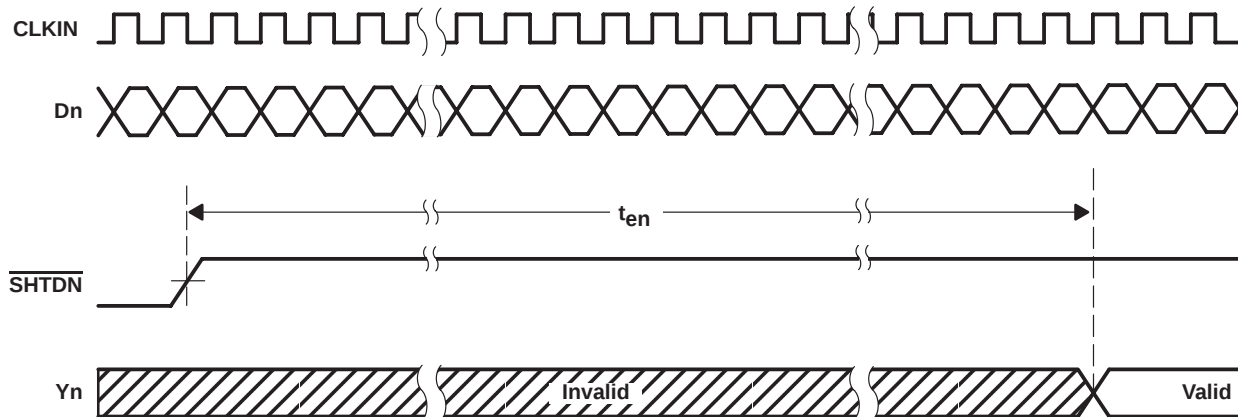


Figure 7. Enable Time Waveforms (CLKSEL low shown)

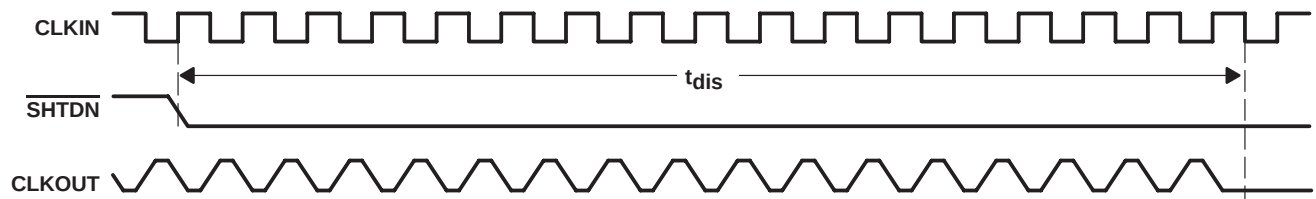


Figure 8. Disable Time Waveforms (CLKSEL low shown)

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TYPICAL CHARACTERISTICS

WORST-CASE SUPPLY CURRENT
VS
FREQUENCY

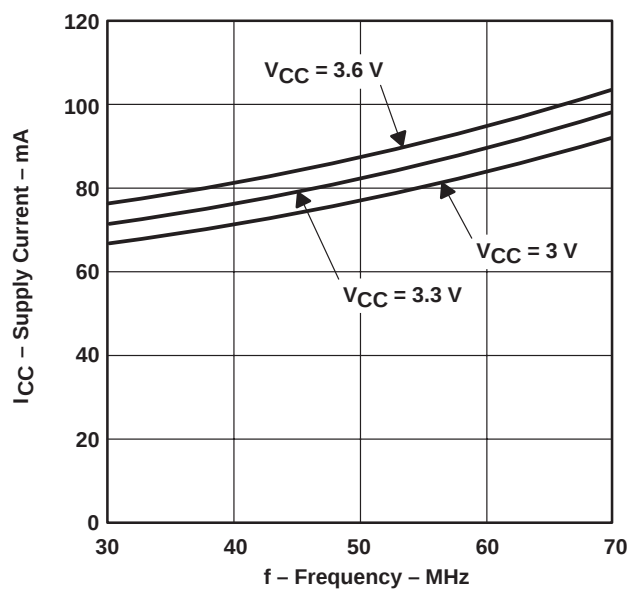


Figure 9

APPLICATION INFORMATION

16-bit bus extension

In a 16-bit bus application (Figure 10), TTL data and clock coming from bus transceivers that interface the backplane bus arrive at the Tx parallel inputs of the LVDS serdes transmitter. The clock associated with the bus is also connected to the device. The on-chip PLL synchronizes this clock with the parallel data at the input. The data is then multiplexed into three different line drivers which perform the TTL to LVDS conversion. The clock is also converted to LVDS and presented to a separate driver. This synchronized LVDS data and clock at the receiver, which recovers the LVDS data and clock, performs a conversion back to TTL. Data is then demultiplexed into a parallel format. An on-chip PLL synchronizes the received clock with the parallel data, and then all are presented to the parallel output port of the receiver.

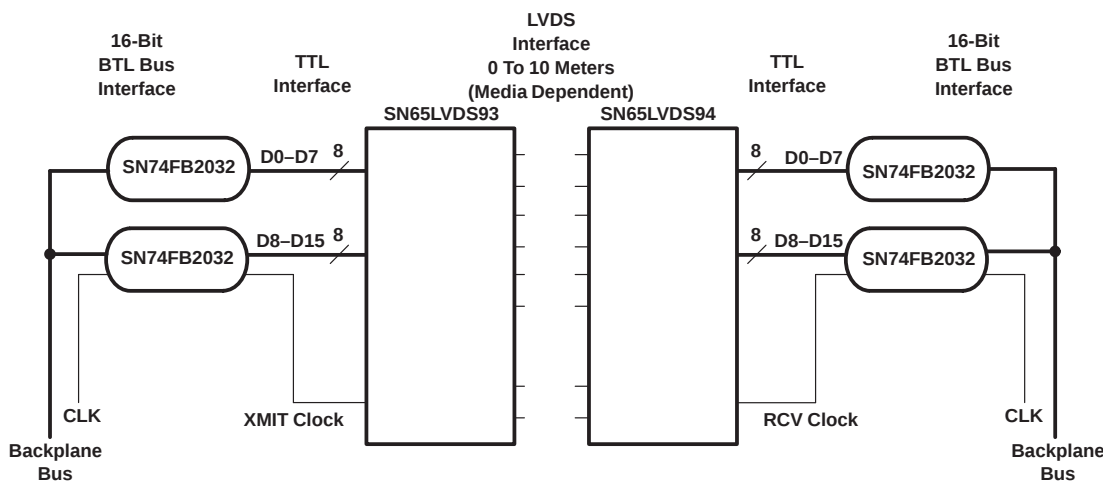


Figure 10. 16-Bit Bus Extension

16-bit bus extension with parity

In the previous application we did not have a checking bit that would provide assurance that the data crosses the link. If we add a parity bit to the previous example, we would have a diagram similar to the one in Figure 11. The device following the SN74FB2032 is a low-cost parity generator. Each transmit-side transceiver/parity generator takes the LVTTTL data from the corresponding transceiver, performs a parity calculation over the byte, and then passes the bits with its calculated parity value on the parallel input of the LVDS serdes transmitter. Again, the on-chip PLL synchronizes this transmit clock with the eighteen parallel bits (16 data + 2 parity) at the input. The synchronized LVDS data/parity and clock arrive at the receiver.

The receiver performs the conversion from LVDS to LVTTTL and the transceiver/parity generator performs the parity calculations. These devices compare their corresponding input bytes with the value received on the parity bit. The transceiver/parity generator will assert its parity error output if a mismatch is detected.

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APPLICATION INFORMATION

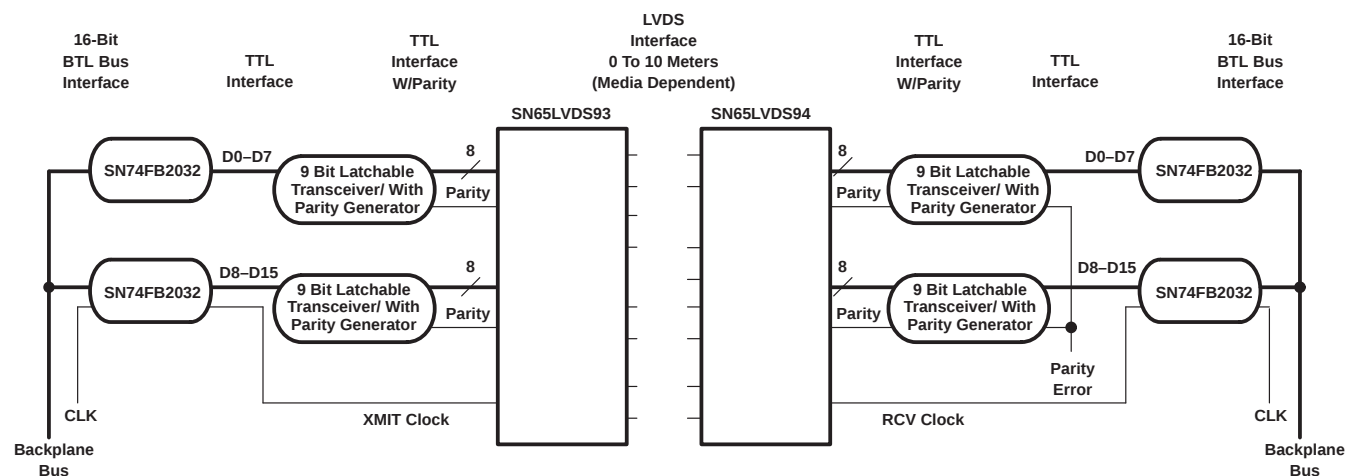


Figure 11. 16-Bit Bus Extension With Parity

low cost virtual backplane transceiver

Figure 12 represents LVDS serdes in an application as a virtual backplane transceiver (VBT). The concept of a VBT can be achieved by implementing individual LVDS serdes chipsets in both directions of subsystem serialized links.

Depending on the application, the designer will face varying choices when implementing a VBT. In addition to the devices shown in Figure 12, functions such as parity and delay lines for control signals could be included. Using additional circuitry, half-duplex or full-duplex operation can be achieved by configuring the clock and control lines properly.

The designer may choose to implement an independent clock oscillator at each end of the link and then use a PLL to synchronize LVDS serdes's parallel I/O to the backplane bus. Resynchronizing FIFOs may also be required.

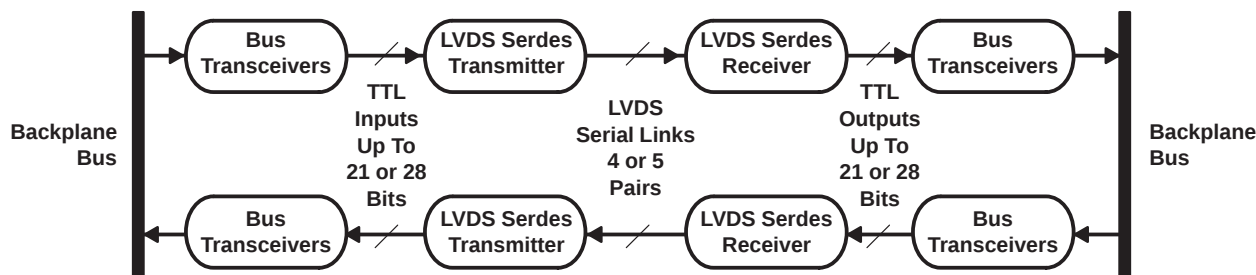


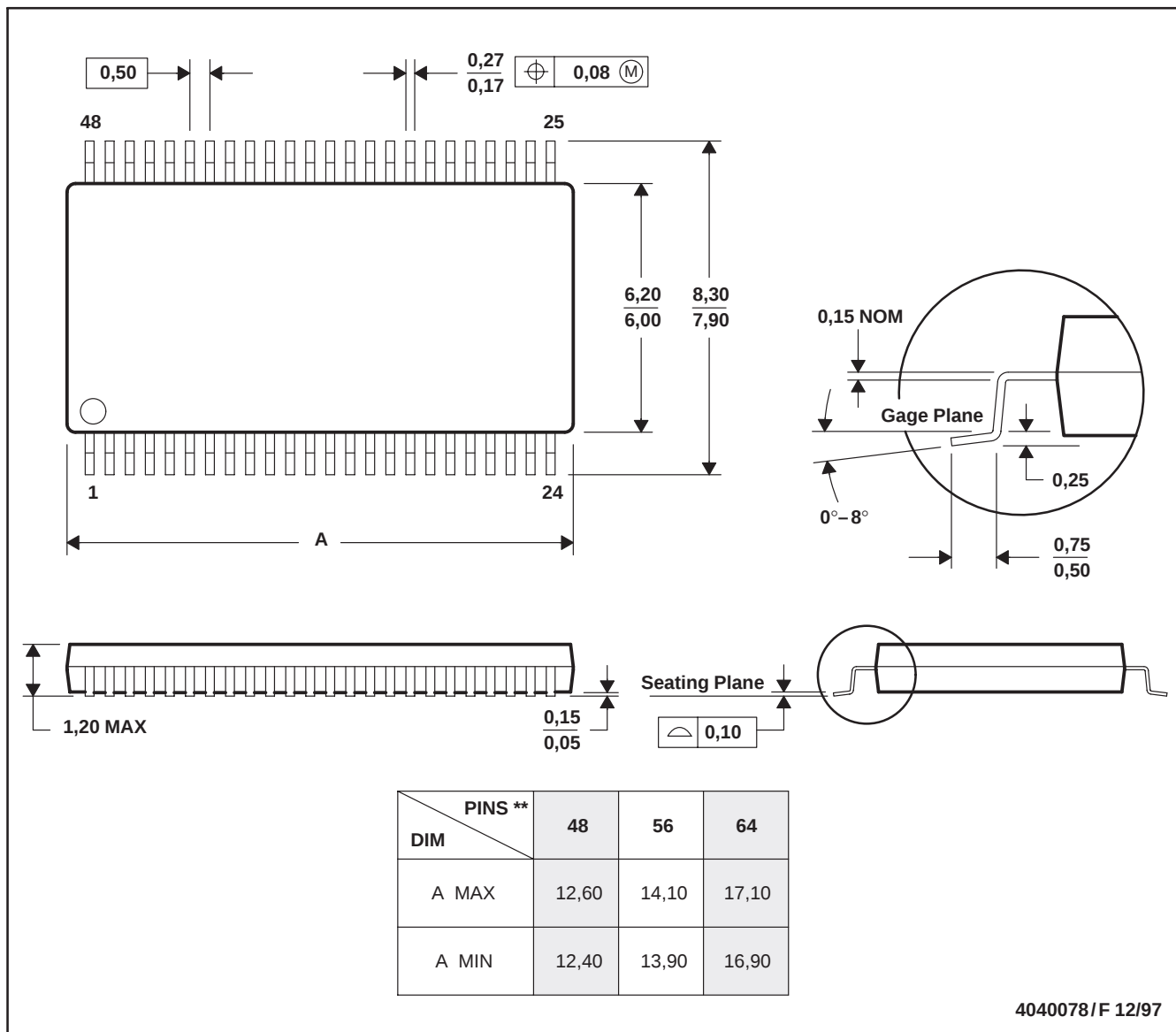
Figure 12. Virtual Backplane Transceiver

MECHANICAL DATA

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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