- Nine Differential Channels for the Data and Control Paths of the Differential Small Computer Systems Interface (SCSI)

- Meets or Exceeds the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)

- Packaged in Shrink Small-Outline Package With 25-mil Terminal Pitch

- Designed to Operate at 10 Million Transfers Per Second

- Low Disabled Supply Current 1.4 mA Typ

- Thermal Shutdown Protection

- Power-Up/Power-Down Glitch Protection

- Positive and Negative Output-Current Limiting

- Open-Circuit Fail-Safe Receiver Design

DL PACKAGE
(TOP VIEW)

NC	1	56	NC
WRAP2	2	55	NC
WRAP1	3	54	CE
1A	4	53	9B+
1DE/$\overline{\text{RE}}$	5	52	9B−
2A	6	51	8B+
2DE/$\overline{\text{RE}}$	7	50	8B−
3A	8	49	7B+
3DE/$\overline{\text{RE}}$	9	48	7B−
4A	10	47	6B+
4DE/$\overline{\text{RE}}$	11	46	6B−
V_{CC}	12	45	V_{CC}
GND	13	44	GND
GND	14	43	GND
GND	15	42	GND
GND	16	41	GND
GND	17	40	GND
V_{CC}	18	39	V_{CC}
5A	19	38	5B+
5DE/$\overline{\text{RE}}$	20	37	5B−
6A	21	36	4B+
6DE/$\overline{\text{RE}}$	22	35	4B−
7A	23	34	3B+
7DE/$\overline{\text{RE}}$	24	33	3B−
8A	25	32	2B+
8DE/$\overline{\text{RE}}$	26	31	2B−
9A	27	30	1B+
9DE/$\overline{\text{RE}}$	28	29	1B−

Pins 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

description

The SN75LBC978 is a nine-channel differential transceiver based on the 75LBC176 LinASIC™ cell. Use of TI's LinBiCMOS™† process technology allows the power reduction necessary to integrate nine differential balanced transceivers†. On-chip enabling logic makes this device applicable for the data path (eight data bits plus parity) and the control path (nine bits) for the Small Computer Systems Interface (SCSI) standard. The WRAP function allows in-circuit testing and wired-OR channels for the BSY, RST, and SEL signals of the SCSI bus.

The SN75LBC978 is packaged in a shrink small-outline package (DL) with improved thermal characteristics using heat-sink terminals. This package is ideal for low-profile, space-restricted applications such as hard disk drives.

The switching speed of the SN75LBC978 is sufficient to transfer data over the data bus at 10 million transfers per second. Each of the nine identical channels conforms to the requirements of the ANSI RS-485 and ISO 8482:1987(E) standards referenced by ANSI X3.131-1993 (SCSI-2) and the proposed SCSI-3 standards.

The SN75LBC978 is characterized for operation from 0°C to 70°C.

† Patent Pending
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logic diagram (positive logic)
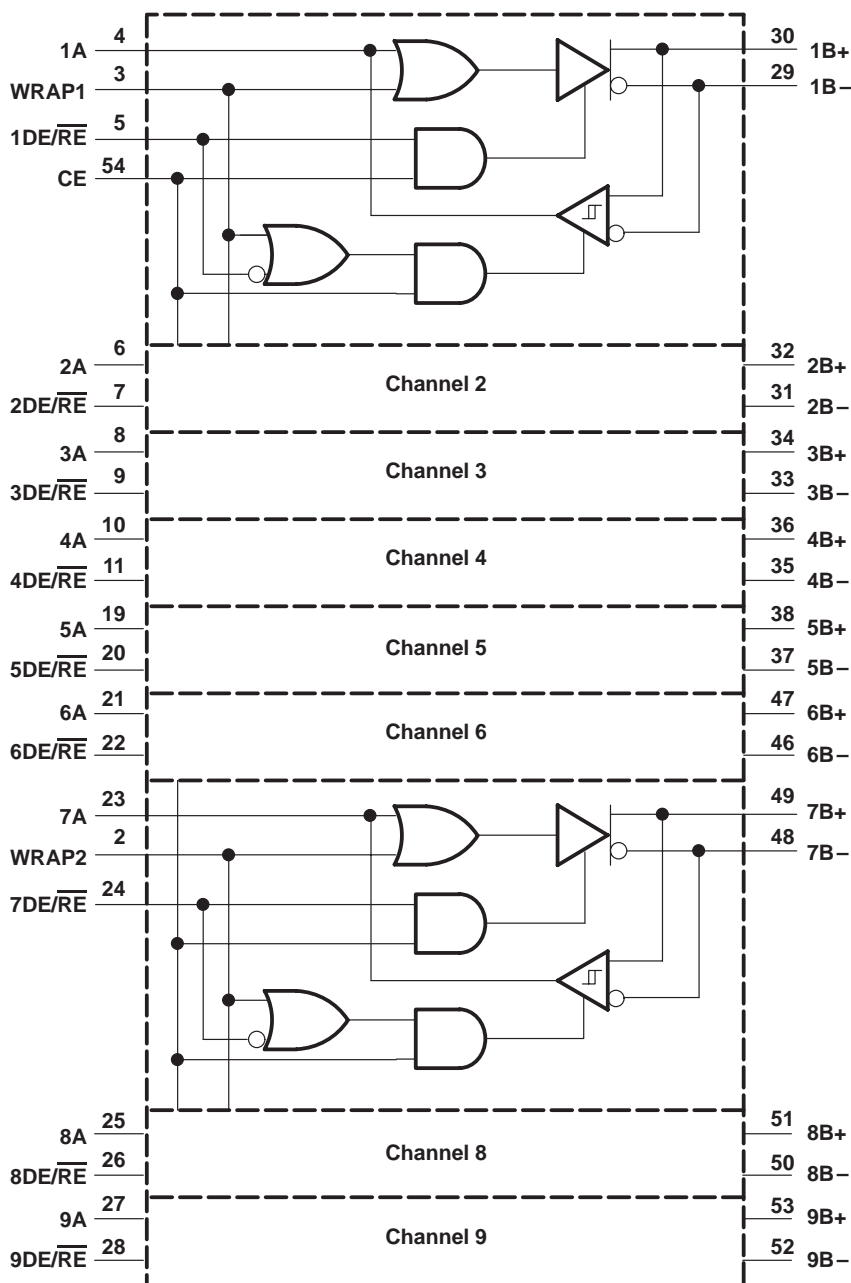
schematics of inputs and outputs

ALL INPUTS EXCEPT CE

INPUT CE

B+ AND B– I/O PORTS

RECEIVER OUTPUT
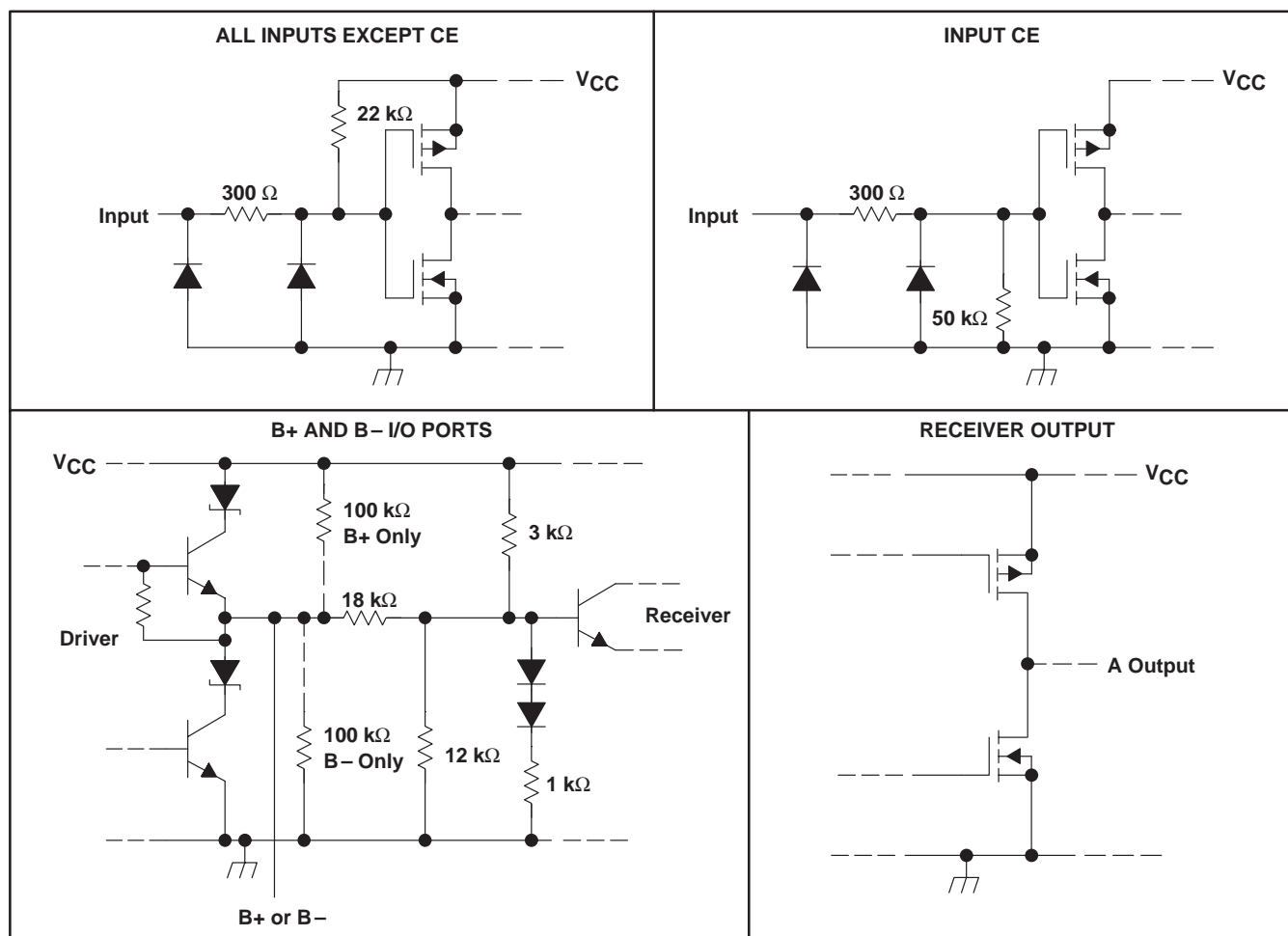
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... −0.3 V to 7 V
Bus voltage range .... −10 V to 15 V
Data I/O and control (A-side) voltage range .... −0.3 V to 7 V
Continuous power dissipation .... internally limited
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are dc and with respect to GND.

SN75LBC978
9-CHANNEL DIFFERENTIAL TRANSCEIVER

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_O, V_I, or V_{IC}	B+ or B−			12	V
				−7	
High-level input voltage, V_{IH}	All except B+ and B−	2			V
Low-level input voltage, V_{IL}	All except B+ and B−			0.8	V
High-level output current, I_{OH}	B+ or B−			−60	mA
	A			−8	mA
Low-level output current, I_{OL}	B+ or B−			60	mA
	A			8	mA
Operating free-air temperature, T_A		0		70	°C

device electrical characteristics over recommended ranges of operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	A, WRAP, DE/$\overline{RE}$	See Figure 1	V_{IH} = 2 V			−200	µA
		CE					100	µA
I_{IL}	Low-level input current	A, WRAP, DE/$\overline{RE}$		V_{IL} = 0.8 V			−200	µA
		CE					100	µA
I_{CC}	Supply current	All drivers and receivers disabled	CE at 0 V			1.4	3	mA
		All receivers enabled	No load, CE at 5 V,	V_{ID} = 5 V, WRAP and DE/$\overline{RE}$ at 0 V		29	45	mA
		All drivers enabled	No load, WRAP at 0 V	CE and DE/$\overline{RE}$ at 5 V,		7	10	mA
C_O	Bus port output capacitance		B+ or B−			19		pF
C_{pd}	Power dissipation capacitance		One driver			460		pF
			One receiver			40		pF

driver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$|V_{OD}|$	Differential output voltage	V_{test} = −7 V to 12 V, See Figure 2	1	2		V
I_{OS}	Output short-circuit current	See Figure 3			±250	mA
I_{OZ}	High-impedance-state output current	See receiver input current				

receiver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted) (see Figure 3)

	PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$V_{ID} = 200$ mV,	$I_{OH} = -8$ mA	2.5			V
V_{OL}	Low-level output voltage		$V_{ID} = -200$ mV,	$I_{OL} = 8$ mA			0.8	V
V_{IT+}	Differential-input high-level threshold voltage		$I_{OH} = -8$ mA				0.2	V
V_{IT-}	Differential-input low-level threshold voltage		$I_{OL} = 8$ mA		−0.2			V
V_{hys}	Receiver input hysteresis voltage ($V_{IT+} - V_{IT-}$)					45		mV
I_I	Receiver input current	B+ and B−	$V_I = 12$ V, $V_{CC} = 5$ V, Other input at 0 V			0.7	1	mA
			$V_I = 12$ V, $V_{CC} = 0$ V, Other input at 0 V			0.8	1	mA
			$V_I = -7$ V, $V_{CC} = 5$ V, Other input at 0 V			−0.5	−0.8	mA
			$V_I = -7$ V, $V_{CC} = 0$ V, Other input at 0 V			−0.4	−0.8	mA
I_{OZ}	High-impedance-state output current		$V_O = $ GND				−200	µA
			$V_O = V_{CC}$				50	

driver switching characteristics over recommended ranges of operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential delay time, high- to low-level output ($t_{d(ODH)}$) or low- to high-level output ($t_{d(ODL)}$)	See Figure 4		11.8		26.4	ns
		$V_{CC} = 5$ V, $T_A = 25°C$, See Figure 4		14	18	22	
		$V_{CC} = 5$ V, $T_A = 70°C$, See Figure 4		18	22	26	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					15	ns
		$V_{CC} = 5$ V,	See Note 2			8	
$t_{sk(p)}$	Pulse skew ($|t_{d(ODL)} - t_{d(ODH)}|$)	See Figure 4			0	6	ns
t_t	Transition time (t_r or t_f)				10		ns

receiver switching characteristics over recommended ranges of operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{pd}	Propagation delay time, high- to low-level output (t_{PHL}) or low- to high-level output (t_{PLH})	See Figure 5		19.5		30.7	ns
		$V_{CC} = 5$ V, $T_A = 25°C$, See Figure 5		20.2	24.7	29.2	
		$V_{CC} = 5$ V, $T_A = 70°C$, See Figure 5		21.1	25.6	30.1	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					12	ns
		$V_{CC} = 5$ V,	See Note 2			9	
$t_{sk(p)}$	Pulse skew ($|t_{PHL} - t_{PLH}|$)	See Figure 5			2	6	ns
t_t	Transition time (t_r or t_f)				3		ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ C_{pd} determines the no-load dynamic current consumption; $I_S = C_{pd} \cdot V_{CC} \cdot f + I_{CC}$.
NOTE 2: This specification applies to any 5°C band within the operating temperature range.

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SN75LBC978
9-CHANNEL DIFFERENTIAL TRANSCEIVER

SLLS134E – APRIL 1992 – REVISED MAY 1997

transceiver switching characteristics over recommended ranges of operating conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{en(TXL)}$	Enable time, transmit-to-receive to low-level output			80	ns
$t_{en(TXH)}$	Enable time, transmit-to-receive to high-level output			80	ns
$t_{en(RXL)}$	Enable time, receive-to-transmit to low-level output	See Figure 6		150	ns
$t_{en(RXH)}$	Enable time, receive-to-transmit to high-level output			150	ns
t_{su}	Setup time, WRAP1 or WRAP2 before active input(s) or output(s)		150		ns

thermal characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			12		°C/W

PARAMETER MEASUREMENT INFORMATION
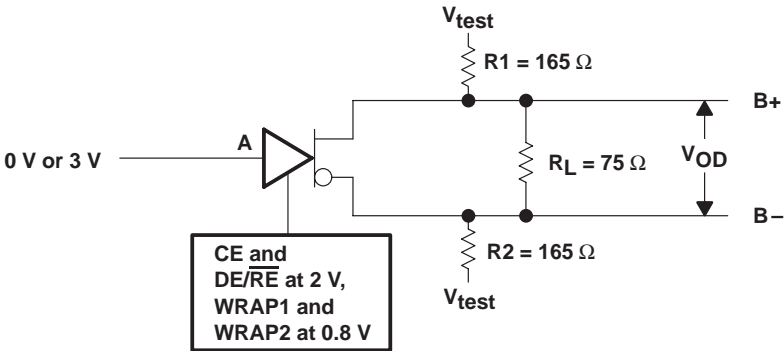
Figure 1. Driver V_{OD} Test Circuit
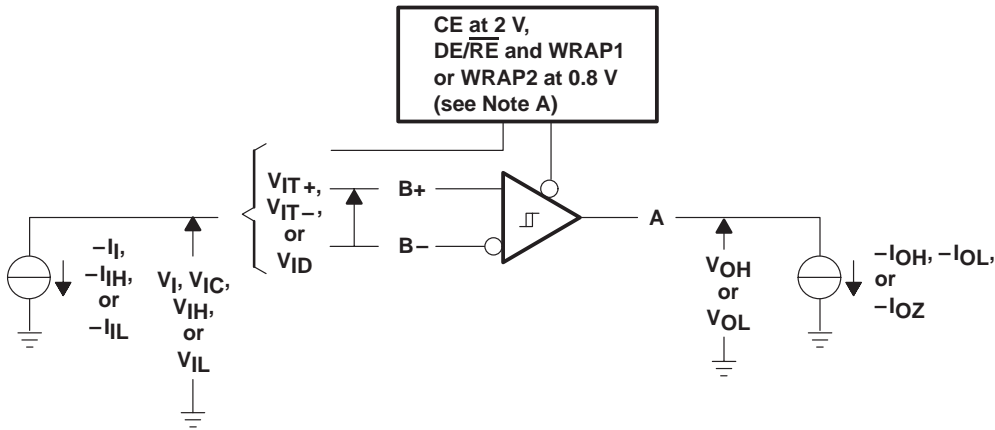
NOTE A: For the I_{OZ} measurement, CE is at 0.8 V.

Figure 2. Receiver Test Circuit and Input Conditions

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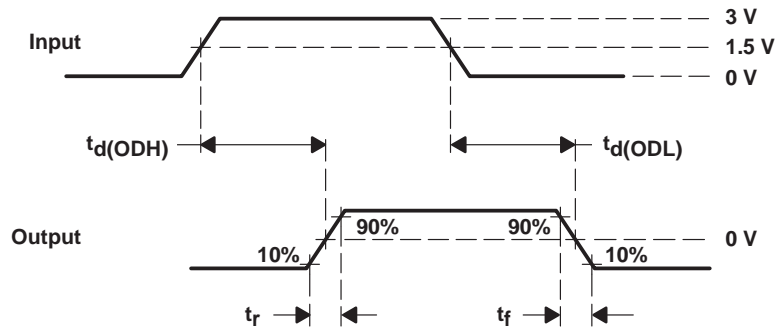
6

PARAMETER MEASUREMENT INFORMATION
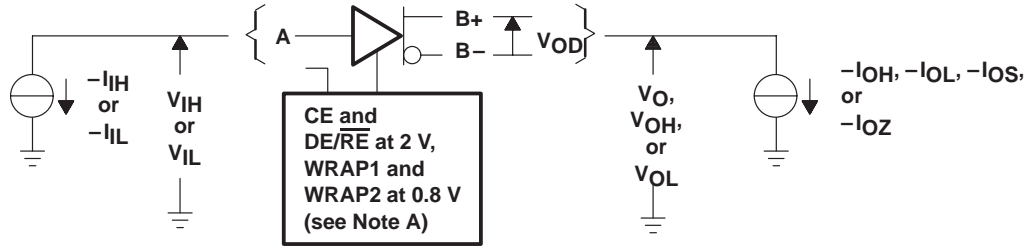
NOTE A: For the I_{OZ} test, the CE input is at 0.8 V.

Figure 3. Driver Test and Input Conditions
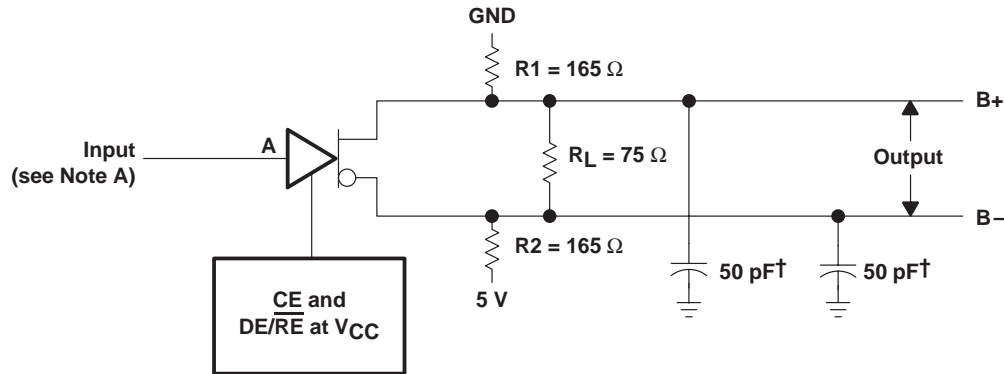
TEST CIRCUIT

VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.
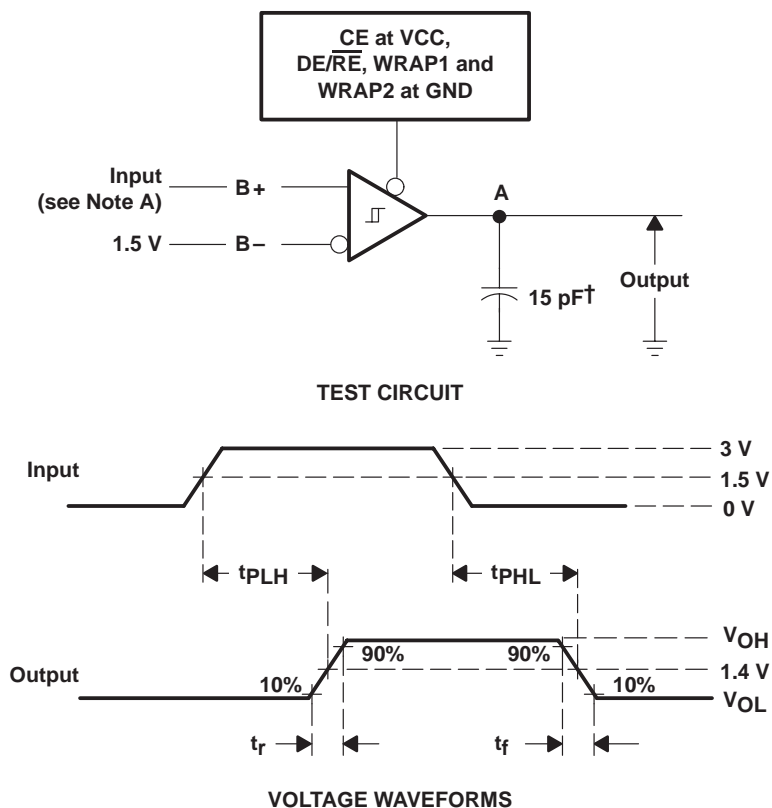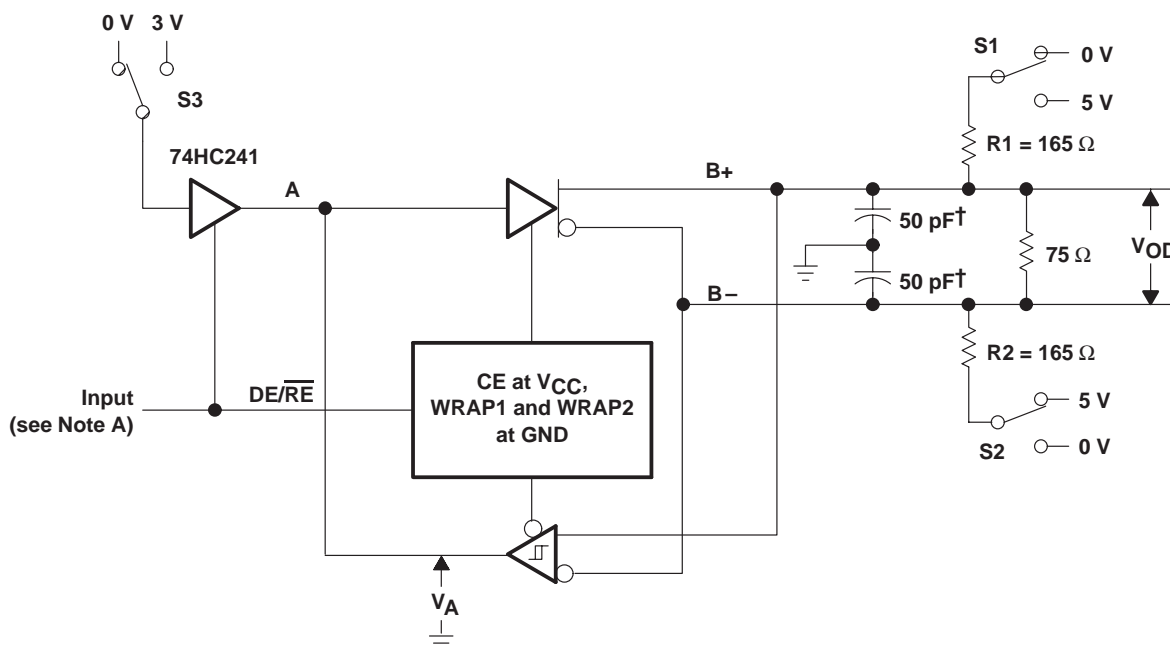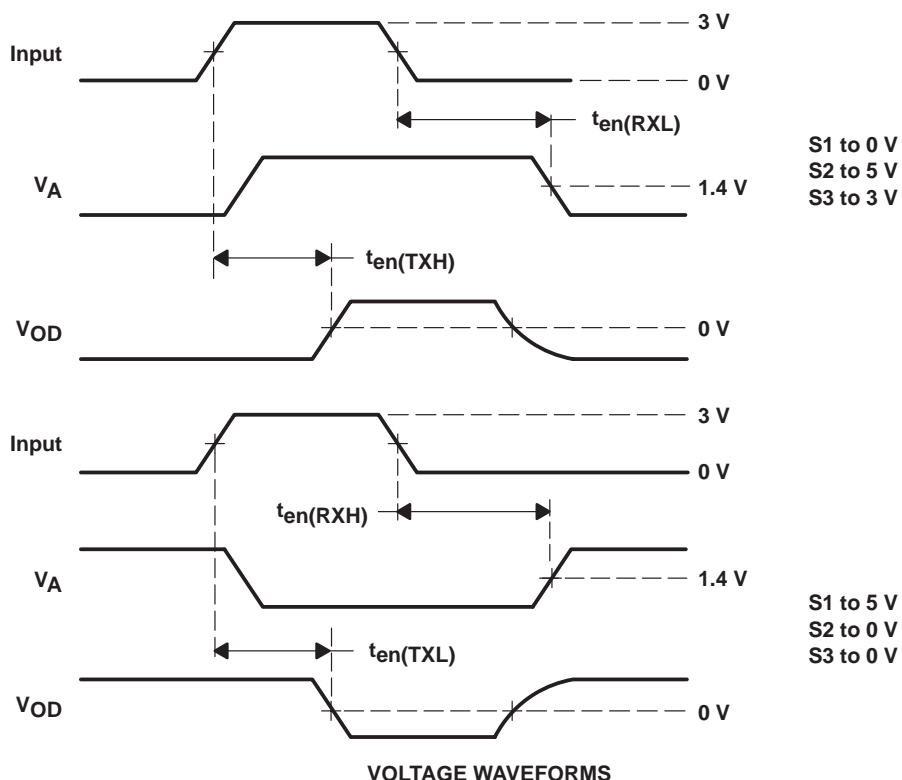
Figure 4. Driver Propagation Delay Time Test Circuit and Waveforms

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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 5. Receiver Propagation Delay Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 6. Enable Time Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

Figure 7

INPUT CURRENT
vs
INPUT VOLTAGE

Figure 8

INPUT CURRENT
vs
INPUT VOLTAGE

Figure 9

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TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 10

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 11

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT
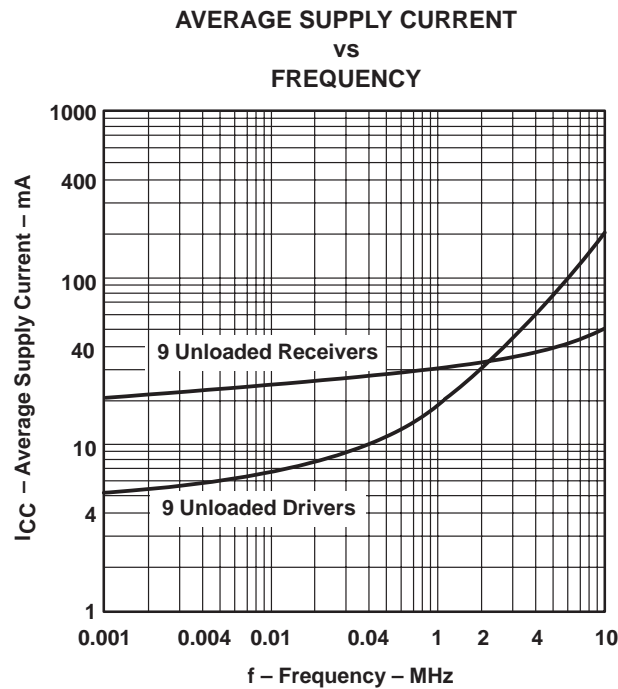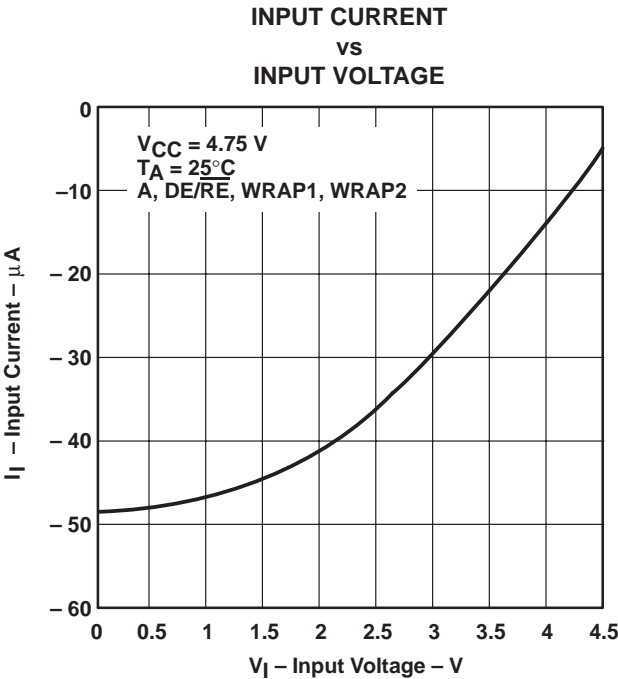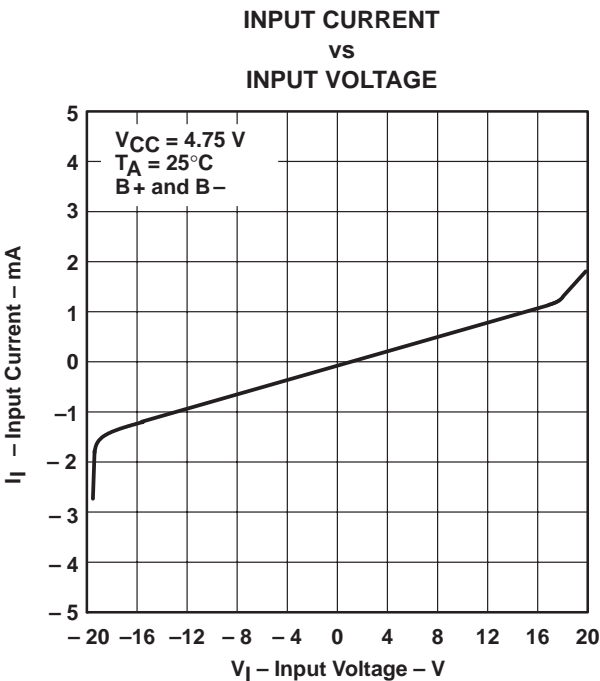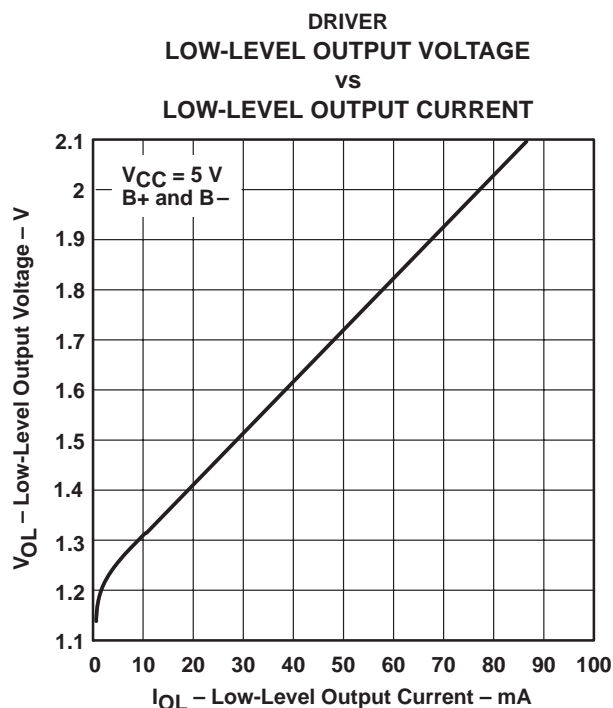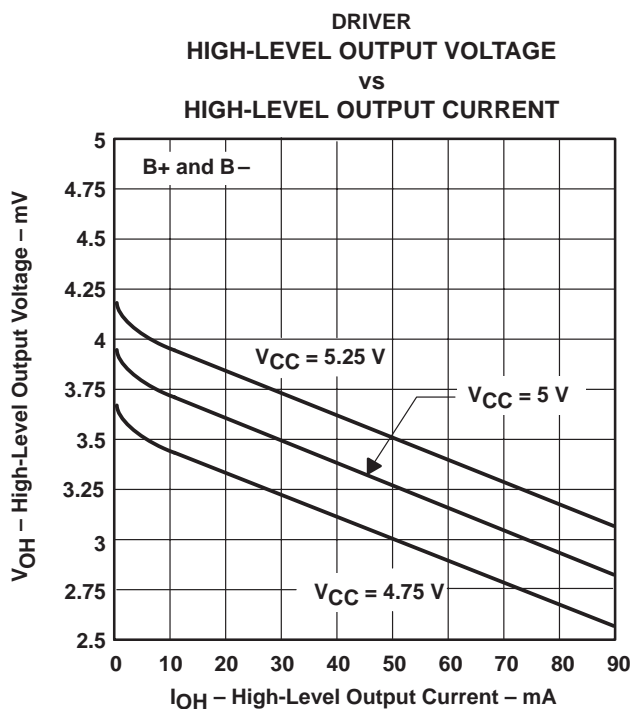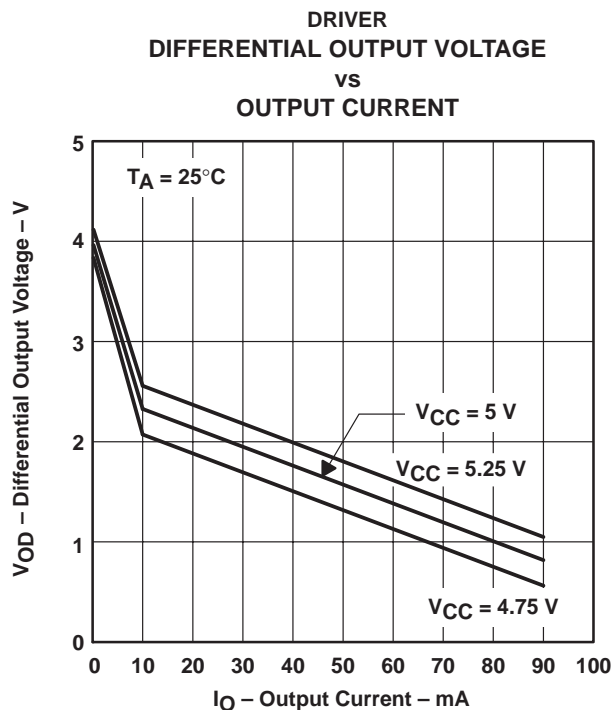
Figure 12

SN75LBC978
9-CHANNEL DIFFERENTIAL TRANSCEIVER

TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 13

DRIVER
HIGH-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 14

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 15

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 16

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TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 17

RECEIVER
PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

Figure 18

DRIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE
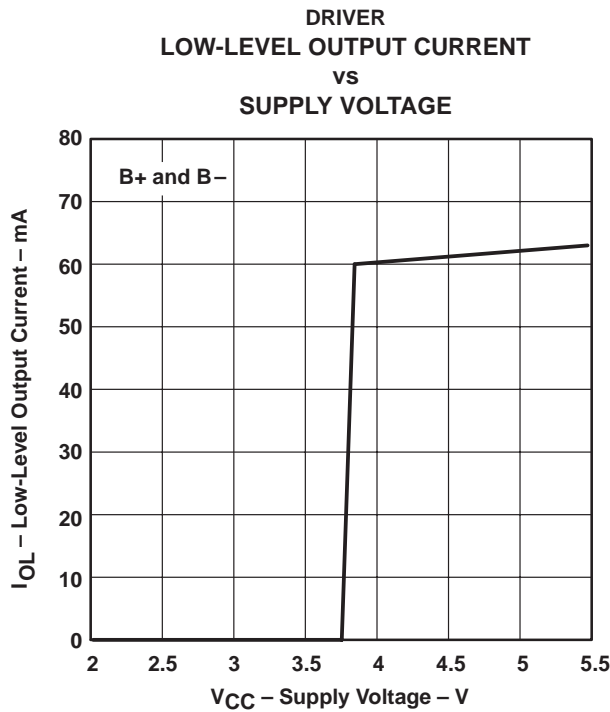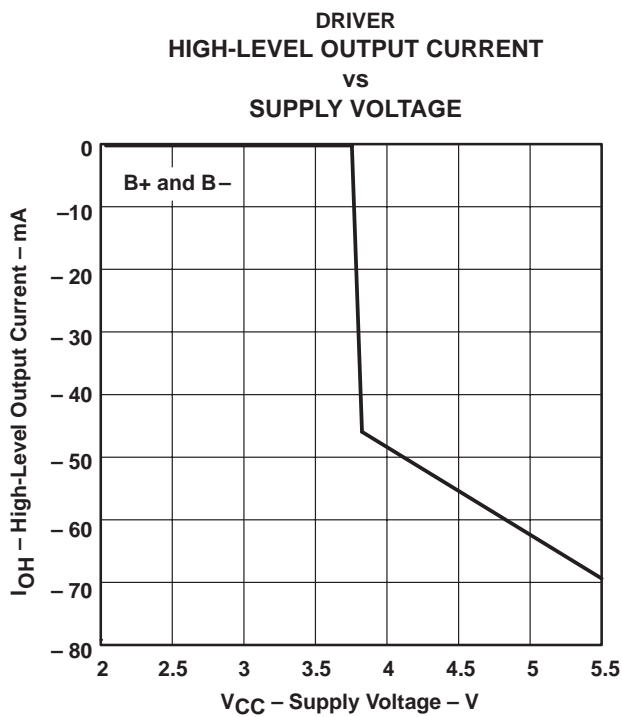
Figure 19

APPLICATION INFORMATION

function tables

Table 1. Channel Configuration for Totem Pole Circuit

CE is high, WRAP1 or WRAP2 is low
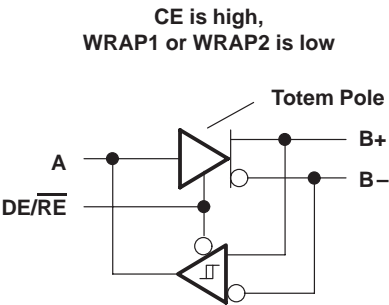
INPUTS				OUTPUTS		
DE/RE	A	B+†	B−†	A	B+	B−
L	X	L	H	L	Z	Z
L	X	H	L	H	Z	Z
H	L	X	X	Z	L	H
H	H	X	X	Z	H	L

H = high level   L = low level   X = irrelevant   Z = high impedance

† An H in this column represents a voltage 200 mV higher than the other bus input. An L represents a voltage 200 mV lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

Table 2. Channel Configuration for Emitter Follower Circuit

CE is high, WRAP1 or WRAP2 is high
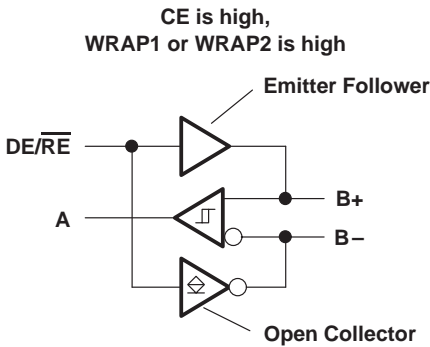
INPUTS			OUTPUTS		
DE/RE	B+	B−	A	B+	B−
L	L	H	L	Z	Z
L	H	L	H	Z	Z
H	X	X	H	H	L
H	X	X	H	H	L

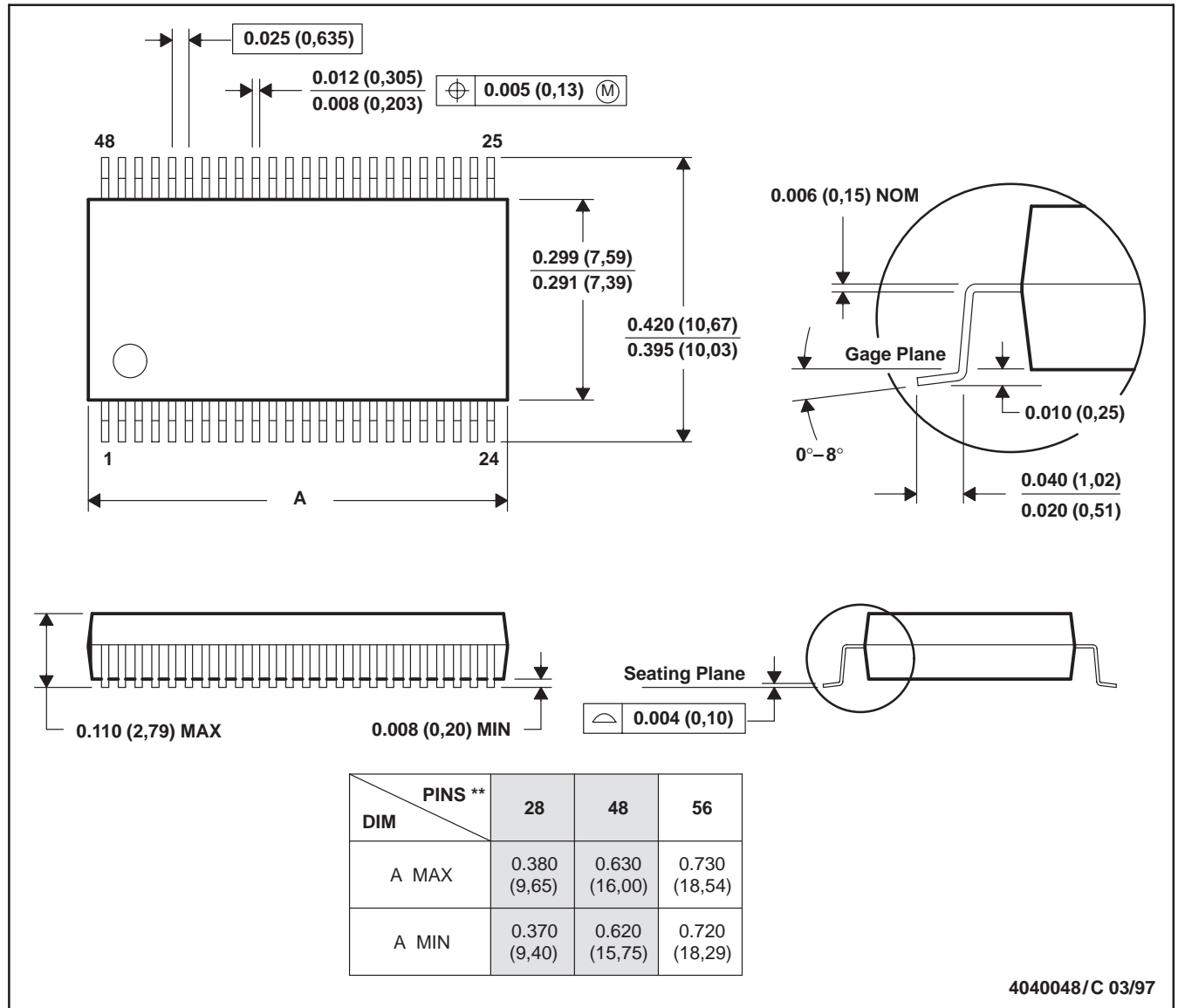H = high level   L = low level   X = irrelevant   Z = high impedance

MECHANICAL INFORMATION

DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN

0.025 (0,635)

0.012 (0,305) / 0.008 (0,203) $\oplus$ | 0.005 (0,13) (M)

48   25

0.299 (7,59) / 0.291 (7,39)

0.420 (10,67) / 0.395 (10,03)

1   24

A

0.006 (0,15) NOM

Gage Plane

0°–8°

0.010 (0,25)

0.040 (1,02) / 0.020 (0,51)

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

0.004 (0,10)

DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / C 03/97

NOTES: A. All linear dimensions are in inches (millimeters).
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
           D. Falls within JEDEC MO-118

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