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TSB12LV23/TSB41LV02 Mobile Reference Design

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TSB12LV23/TSB41LV02 Mobile Reference Design

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ABSTRACT

This application report describes the electrical connections between the Texas Instruments TSB12LV23 (400-Mbps OHCI-Lynx) and TSB41LV02 (400-Mbps PHY) for non-isolated mobile applications.

The TSB12LV23 (OHCI-Lynx) is both an open host controller interface 1.0 (OHCI) and IEEE 1394.a compliant Link-layer device that transports data between the PCI bus and PHY interface. For more information refer to the *TI Data Manual (SLLS328)*.

The TSB41LV02 is a two-port 400 Mbps physical layer device and is IEEE 1394.a compliant. The TSB41LV02 is backward-compatible with the IEEE 1394–1995 standard and can operate at 100 Mbps, 200 Mbps, and 400 Mbps. For more information on the TSB41LV02, refer to the TI data sheet, *IEEE 1394A Two-Port Cable Transceiver/Arbiter* (literature number SLLS355).

NOTE: This reference schematic does not represent an actual test board constructed or tested by Texas Instruments.

1 The Cable Interface

Figure 8 of the OHCI-LYNX/TSB41LV02 schematic shows the electrical connections for the cable interface, which includes one 1394 port connected to the PHY. The second 1394 port is not implemented to show how to correctly terminate an unused port.

If two 1394 ports are implemented, a 750-mA current-limited fuse must be connected between the 12-V supply and bus power as shown in Figure 1.

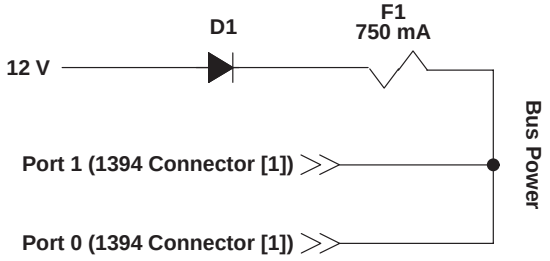


Figure 1. Fuse Placement

The cable power from each cable (terminal 1, PWR, on the 6 terminal 1394 connector) is connected to the other ports and is available as the bus power. The PHY does not operate off of bus power on the schematic. If bus power is required, then a voltage regulator is needed to regulate the bus power to 3.3 V for the PHY and is illustrated in Figure 2.

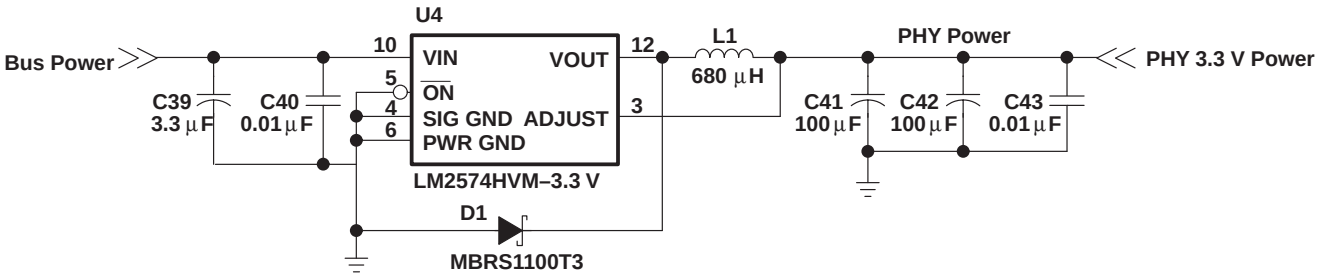


Figure 2. PHY Voltage Regulator

The cable shield from each cable (terminals 7 and 8 (SHLD) on the 6 terminal 1394 connector) is connected to chassis ground through an R-C network. This R-C network is designed to prevent current from flowing on the cable shield in case of potential differences between it and chassis ground. We suggest a combination of a 1-MΩ resistor, two 0.001-µF capacitors, and two 0.01-µF capacitors be connected to all the shield GND terminals (7 and 8) on the 1394 connectors. In addition, individual R-C networks could be set up for each connector, which would help prevent the cable shield noise on one port from coupling onto the other ports.

The cable ground (terminal 2 (GND) on the 6-terminal 1394 connector) is tied directly to PHY ground. According to the 1394 standard, all PHYs in a network must be at the same ground potential for common mode signaling.

The drivers on each port (TPA and TPB) are designed to work with an external 112-Ω termination resistor network. This is to match the 110-Ω cable impedance. One network is provided at each end of the twisted pair cable. The midpoint of the TPA resistor network is directly connected to TPBIAS; and the midpoint of the TPB resistor network is coupled to ground through a paralleled RC network. These termination resistor networks should be placed as close to the PHY as possible.

The TPBIAS lines indicate the presence of an active connection to other nodes on the bus. A 1-µF capacitor external filter is used to stabilize the TPBIAS lines.

When a 1394 port is not brought out to a connector, it must be terminated correctly. To terminate a non-implemented port, the TPB+ and TPB– terminals must be tied together and connected to ground. The TPBIAS should be tied to ground through a 1-µF capacitor filter. The TPA+ and TPA– lines can be left unconnected. Port 1 in the schematic is not brought out to a connector to illustrate a properly terminated port.

2 The Physical Layer - TSB41LV02

Figure 9 of the OHCI-LYNX/TSB41LV02 schematic shows the electrical connections for the physical layer (TSB41LV02).

All of the power terminals on the TSB41LV02 PHY should be coupled to the associated power terminals and ground through a series of high-frequency decoupling capacitors. The rules for the decoupling capacitors are:

- Place one 0.001-μF capacitor as closely as possible to each power terminal on the PHY.
- Place one 0.1-μF capacitor as closely as possible to each power terminal group (two or more adjacent power terminals) on the PHY.
- Place one 0.1-μF capacitor as closely as possible to each single power terminal (not adjacent to another) on the PHY.

A power terminal group is two or more adjacent power terminals connected to the same power supply. For example, terminals 30 and 31 are both connected to the AV_{DD} supply. These two terminals constitute a power terminal group; and a 0.1-μF capacitor should be placed as closely as possible to these terminals on the PHY. Terminal 56 ($PLLV_{DD}$) is a single power terminal, since it is not adjacent to any other power terminal; and a 0.1-μF capacitor should be placed as closely as possible to this terminal as well. Detailed information on capacitor placement is available in the TI datasheet SLLS–TBD).

The TSB41LV02 has 5-V tolerant inputs. Whenever connecting to a 5-V device, the VCC5V terminal should be tied to the 5-V supply. If the TSB41LV02 is only connected to 3.3-V devices, the VCC5V terminal should be tied to the 3.3-V supply. The 3.3-V implementation is shown in the schematic.

The $\overline{ISO}$ terminal is used to control the output differentiation on the PHY/Link interface for the Annex J method of isolation. If the IEEE 1394-1995 Annex J method of isolation is used, the $\overline{ISO}$ terminal should be tied low. If the TI bus-holder method of isolation or no isolation is used, then this terminal should be tied high. No isolation is implemented in the schematic, so $\overline{ISO}$ is tied to PHY_VCC through a 10-kΩ resistor.

Normally, the CPS terminal is connected to the cable power through a 400-kΩ resistor, which is used to detect whether or not cable power is present. A common resistor value of 390 kΩ may be used; however, for mobile designs where bus power is not needed, the CPS terminal should be tied directly to PHY ground through a 1-kΩ pull-down resistor, which is used to indicate that cable power is not available. In additions, the power class should be set to 000b.

> **NOTE:** The only instance where the CPS terminal may not be connected to cable power is in the case of a 4-terminal connector or 6-terminal connector with power class 000b. Here the CPS may be tied to PHY ground through a 1-kΩ resistor indicating cable power is not available.

The FILTER0 and FILTER1 terminals are used to provide a filter capacitor for the internal PLL. A 0.1 μF (10% or better) capacitor is the only external requirement needed to complete this filter.

The SE and SM terminals are test inputs used in the manufacturing of the TSB41LV02. For normal use, these terminals should be tied to ground separately through 1-kΩ pull-down resistors.

The R0 and R1 terminals set the internal operating currents and the cable-driver output current. A 6.3-kΩ ±0.5% resistance is required to meet the voltage limits for the IEEE 1394-1995 standard output. To achieve this, a 6.34-kΩ ±0.5% and 1-MΩ ±1% resistor are placed in parallel.

The X0 and XI terminals are the crystal oscillator inputs and connect to a 24.576 MHz parallel resonant fundamental mode crystal. There is a strict tolerance of 100 ppm on the 24.576 MHz crystal; however, it is suggested that this parameter be kept well below 100 ppm. This tolerance must be met to comply with the overall requirement of 100 ppm per the IEEE 1394-1995 standard. Loading requirements for every crystal depend on the board technology and distance from the PHY. The crystal manufacturer should be able to provide the loading requirements.

> **NOTE:** A crystal load capacitance of 15 pF or less is recommended. The external crystal terminating capacitors can be calculated as follows:
>
> $$C_{Termination} = (CL - 4) \times 2$$

The TESTM terminal is a test control input used during the manufacturing of the TSB41LV02 PHY. It should be tied directly to V_{CC}.

A node can be a power provider, power consumer, or neither. The power class terminals (PC0–PC2) are used to program the power class value into the PWR field of the transmitted self-id packet. This ensures that every node on the bus understands the power requirements of the node. These terminals are programmed according to the Power Class Descriptions in the IEEE 1394.a Standard.

In Figure 9 of the schematic the PHY is programmed as power class of 000b or 0. This indicates that the node is not capable of repeating power and does not use bus power. The power class terminals are hard-wired to their values on the schematic.

Reset is best accomplished by connecting the $\overline{\text{RESET}}$ terminal to ground through a 0.1-μF capacitor.

The PD terminal is a legacy terminal that is no longer needed to power down the PHY which is now handled via the 1394.a suspend/resume feature. The PD terminal should be tied to ground through a 1-kΩ pull-down resistor.

The CNA terminal is **not** recommended for this design. This terminal should be left unconnected.

3 The PHY-Link Interface

The PHY-Link interface electrical connection is shown on Figure 10 of the OHCI-LYNX/TSB41LV02 interface schematic. The PHY-Link interface follows the IEEE 1394-1995 and 1394.a standards. No isolation is implemented in this schematic. The PHY and Link operate with common power and ground planes.

The schematic shows no adjustment for EMI considerations. To help minimize EMI, we suggest including a 0-Ω resistor on the SCLK signal as close as possible to the PHY. If EMI issues are a concern, the value of this resistor can be adjusted to reduce emissions. This will also reduce reflections that may occur when the distance between the PHY and Link is large (greater than 4 inches.)

The SCLK is a 49.152-MHz clock provided by the PHY to the Link. SCLK is essential for transactions on the PHY-Link interface as well as transactions within the Link.

The LREQ, or Link Request, signal is an input to the PHY from the Link. The Link uses this to initiate a service request to the PHY. CTL0 and CTL1 are bidirectional signals used to control communication between the PHY and the Link. These terminals should be directly connected between the PHY and Link.

Both the TSB12LV23 (Link layer) and the TSB41LV02 (Phy) are 400-Mbps devices, which use terminals D0–D7 to transport data bidirectionally, and should be connected directly to each other respectively (i.e., D0 ↔ D0 . . . D7 ↔ D7).

The Link's PHY_LPS (Link Power Status) terminal is asserted to indicate that the Link is powered on. The LPS input on the PHY can be tied to either the Link layer's PHY_LPS terminal or the Link layer's V_{CC}. In addition, the line connecting the Link's PHY_LPS terminal with the PHY's LPS terminal should be pulled down to ground through a 4.7-kΩ resistor.

As is shown in Figure 3, the BMC/PHY_LINKON terminal on the TSB12LV23 is connected the TSB41LV02 C/LKON terminal through a 1-kΩ series resistor and 10-kΩ pulldown resistor on the TSB41LV02 side. The PHY's LKON signal is used to activate (wake) the Link when the Link is not active. This signal is driven low as long as the Link is not active.

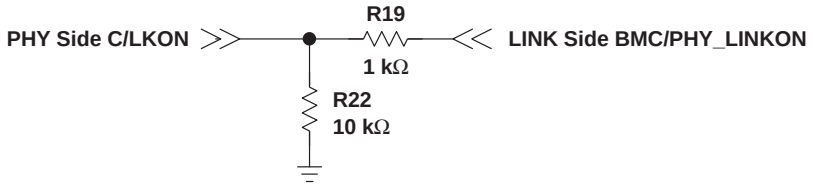


Figure 3. Link On

All of the above PHY-Link interface signals could also be connected to a test header that would provide test points for new prototype designs, as is shown on Figure 10 of the schematic.

4 The Link Layer - TSB12LV23 OHCI-Lynx

The TSB12LV23 is a 400 Mbps Link-layer specifically designed with power management and $\overline{\text{CARDBUS}}$ features.

All of the power 3.3-V V_{CC} terminals on the TSB12LV23 should be coupled together and ground through a series of high-frequency decoupling capacitors as is shown on Figure 8 of the schematic.

- Place one 0.01-µF and one 0.1-µF capacitor as closely as possible to each power terminal on the Link. This will help minimize switching noise.
- Also use a single 47-µF capacitor to reduce dc ripple.

The VCCP power terminals provide a voltage clamping rail for 5-V tolerant inputs. The VCCP voltage is determine by the PCI bus voltage. Figure 4 illustrates the voltage clamping rail.

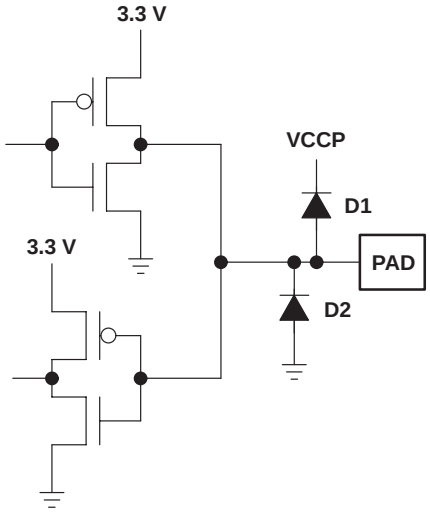


Figure 4. Clamping Voltage

When implementing the TSB12LV23 in a mobile design, the VCCP terminals should be connected the Link's 3.3-V supply.

The $\overline{\text{ISOLATED}}$ terminal is used to enable the bus holders for isolated designs. However, for most designs this is not required.

- To disable the bus-holders connect the $\overline{\text{ISOLATED}}$ terminal to 3.3 V through a 4.7-kΩ pullup resistor.
- To enable the bus-holders connect the $\overline{\text{ISOLATED}}$ terminal to GND through a 220-Ω pulldown resistor.

The $\overline{\text{CARDBUS}}$/CYCLEOUT terminal is sampled when $\overline{\text{G\_RST}}$ is asserted, and it selects between the PCI buffers and CardBus buffers. After reset, this terminal may also function as CYCLEOUT which provides an 8-kHz cycle timer synchronization signal.

- To use the PCI bus buffers, this terminal should be left unconnected, and an internal pullup resistor will enable the PCI buffers.
- To enable the CardBus buffers this terminal should be pulled down with 220-Ω resistor. It is important that a weak pulldown resistor be used if the design is going to use the CYCLEOUT feature.

The CYCLEIN terminal can be used to receive an optional external 8-kHz clock used as a cycle timer, which provides synchronization with other system devices. If not implemented, a 4.7-kΩ pullup resistor should be used to tie this terminal to 3.3 V.

The TSB12LV23's $\overline{\text{G\_RST}}$ terminal allows for retaining context from a D3 to D0 transition when the PCI interface may transition from B3 to B0 and issue a PCI reset. The TSB12LV23 resets are illustrated in Figure 5.

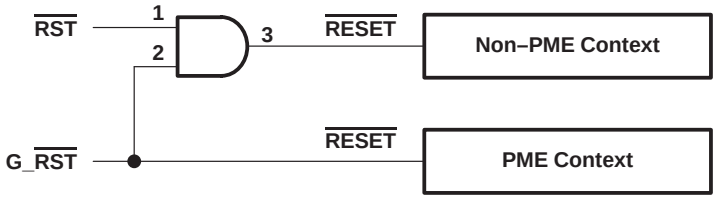
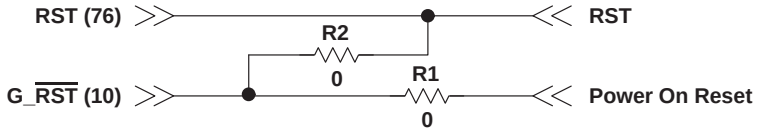


Figure 5. TSB12LV23 Reset Illustration

If the design supports D3 Wake, then the $\overline{\text{G\_RST}}$ terminal provides the hardware reset at power on, while the $\overline{\text{RST}}$ terminal should be connected to the PCI Bus $\overline{\text{RST}}$, which will provides resets that retain the PME context.

For designs that will not support D3 Wake, the $\overline{\text{RST}}$ terminal can either be pulled up to 3.3 V through a 4.7-kΩ resistor or tied together with the $\overline{\text{G\_RST}}$ terminal. An example implementation is shown in Figure 6.



NOTE: For normal operation populate R2 and do not populate R1
For Mobile or D3_Wake operation populate R1 and do not populate R2

Figure 6. Reset

The $\overline{\text{CLKRUN}}$ terminal is used to turn the clock on and off. This is useful in mobile design where conserving power is important. When implementing $\overline{\text{CLKRUN}}$, this terminal is connected to external circuitry that provides a common $\overline{\text{CLKRUN}}$ control signal. If the clock is never turned off, then this terminal should be left unconnected and an internal pulldown resistor will keep the clock active.

The GPIO2 and GPIO3 are general-purpose I/O terminals that should each be pulled down to GND through a 220-Ω resistors.

For more information on the TSB12LV23, consult the TI data manual, *TSB12LV23 (OHCI-LYNX) IEEE 1394-1995 Link-Layer Controller* (literature number SLLS328).

5 The Link Layer - Serial EEPROM

The Serial EEPROM provides a convenient mechanism to load system specific data and is detected at reset via SDA and SCL terminals.

The following are the types of data stored in the EEPROM:

- PCI: Max latency, min grant, subsystem VID, subsystem ID, Link enhancements, miscellaneous control, and CIS offset
- OHCI: GUID, HCControl.programPhyEnable

The serial EEPROM is required for adapter cards, but it is optional for implementations where the BIOS could load GUID and other system specific registers.

NOTE: SDA and SCL should each be pulled up to 3.3 V through 2.7-kΩ resistors, and then connected to the EPROM's SDA and SCL terminals respectively (as is illustrated in Figure 7). If no serial EEPROM is used, then both the SDA and SCL terminals should be connected to ground through 220-Ω pulldown resistors.

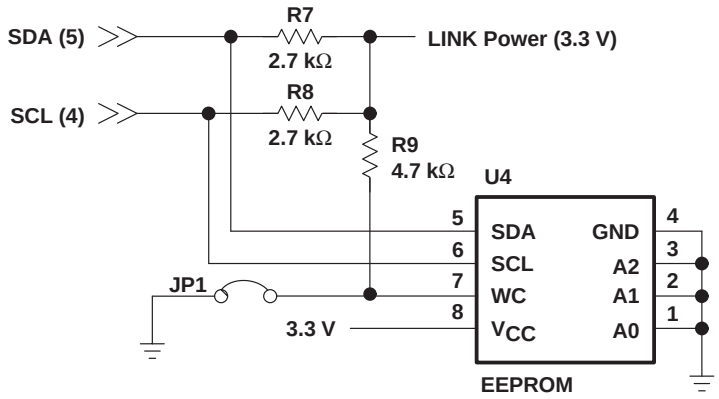


Figure 7. Serial EEPROM

If the EEPROM has a write enable terminal, it should be connected to 3.3 V with a pullup resistor. In addition, a jumper to GND should be connected in series with the pull up, as is illustrated in Figure 7. This allows the EEPROM to be write-enabled and write-disabled.

5.1 Serial Bus Interface

The TSB12LV23 provides a serial bus interface to initialize the 1394 global unique ID register and a few PCI configuration registers through a serial EEPROM. The TSB12LV23 communicates with the serial EEPROM via the 2-wire serial interface.

After power up the serial interface initializes the locations listed in Table 1. While the TSB12LV23 is accessing the serial ROM, all incoming PCI slave accesses are terminated with retry status. Table 2 shows the serial ROM memory map required for initializing the TSB12LV23 registers.

Table 1. Registers and Bits Loadable Through Serial EEPROM

OFFSET	REGISTER	BITS LOADED FROM EEPROM
OHCI register (24h)	1394 GlobalUniqueIDHi	31-0
OHCI register(28h)	1394 GlobalUniqueIDLo	31-0
OHCI register (50h)	Host control register	23
PCI register (2Ch)	PCI subsytem ID	15-0
PCI register (2Dh)	PCI vendor ID	15-0
PCI register (3Eh)	PCI maximum latency, PCI minimum grant	15-0
PCI register (F4h)	Link enhancements control register	13, 12, 9, 8, 7, 2, 1
PCI register (F0h)	PCI miscellaneous register	15, 13, 10, 5-0
PCI register (40h)	PCI OHCI register	0

Table 2. Serial EEPROM Map

BYTE ADDRESS	BYTE DESCRIPTION							
00	PCI maximum latency (0h)				PCI_minimum grant (0h)			
01	PCI vendor ID							
02	PCI vendor ID (msbyte)							
03	PCI subsystem ID (lsbyte)							
04	PCI subsystem ID							
05	[7] Link_enhancement-Control.enab_unfair	[6] HCControl. ProgramPhy Enable	[5] RSVD	[4] RSVD	[3] RSVD	[2] Link_enhancement-Control.enab_ insert_idle	[1] Link_enhancement-Control.enab_accel	[0] RSVD
06	Mini ROM address							
07	1394 GlobalUniqueIDHi (lsbyte 0)							
08	1394 GlobalUniqueIDHi (byte 1)							
09	1394 GlobalUniqueIDHi (byte 2)							
0A	1394 GlobalUniqueIDHi (msbyte 3)							
0B	1394 GlobalUniqueIDLo (lsbyte 0)							
0C	1394 GlobalUniqueIDLo (byte 1)							
0D	1394 GlobalUniqueIDLo (byte 2)							
0E	1394 GlobalUniqueIDLo (msbyte 3)							
0F	Checksum							
10	[15] RSVD	[14] RSVD	[13-12] AT threshold		[11] RSVD	[10] RSVD	[9] Enable audio timestamp	[8] Enable DV CIP timestamp
11	[7] RSVD	[6] RSVD	[5] Select D3 STAT	[4] Disable Tar-get Abort	[3] GP2IIC	[2] Disable SCLK gate	[1] Disable PCI gate	[0] Keep PCI
12	[15] PME D3 Cold	[14] RSVD	[13] PME Sup-port D2	[12] RSVD	[11] RSVD	[10] D2 support	[9] RSVD	[8] RSVD
13	[7] RSVD	[6] RSVD	[5] RSVD	[4] RSVD	[3] RSVD	[2] RSVD	[1] RSVD	[0] Global swap
14	CIS offset address							
15-1E	RSVD							
1F	RSVD							

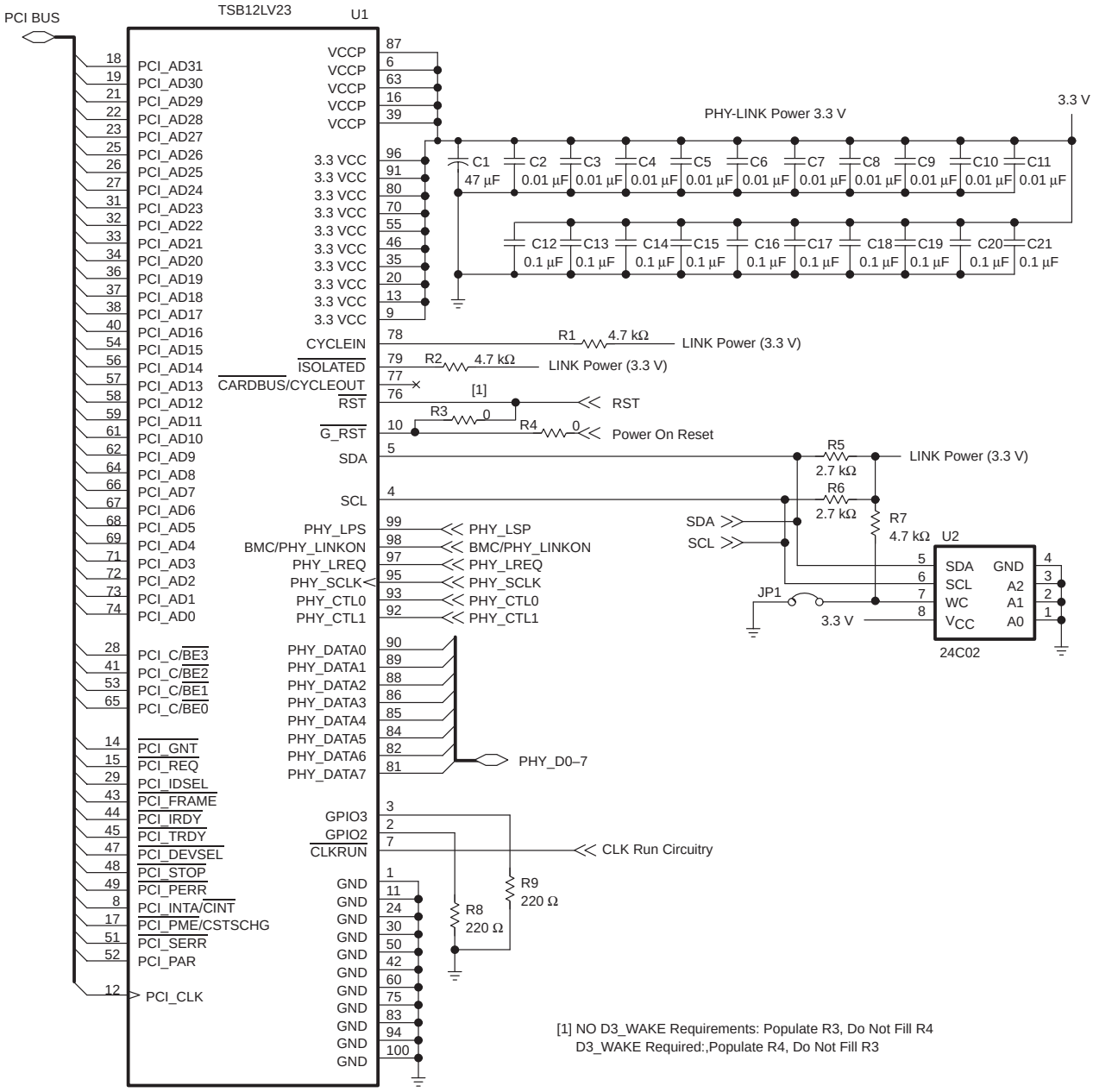


Figure 8. TSB12LV23 Schematic

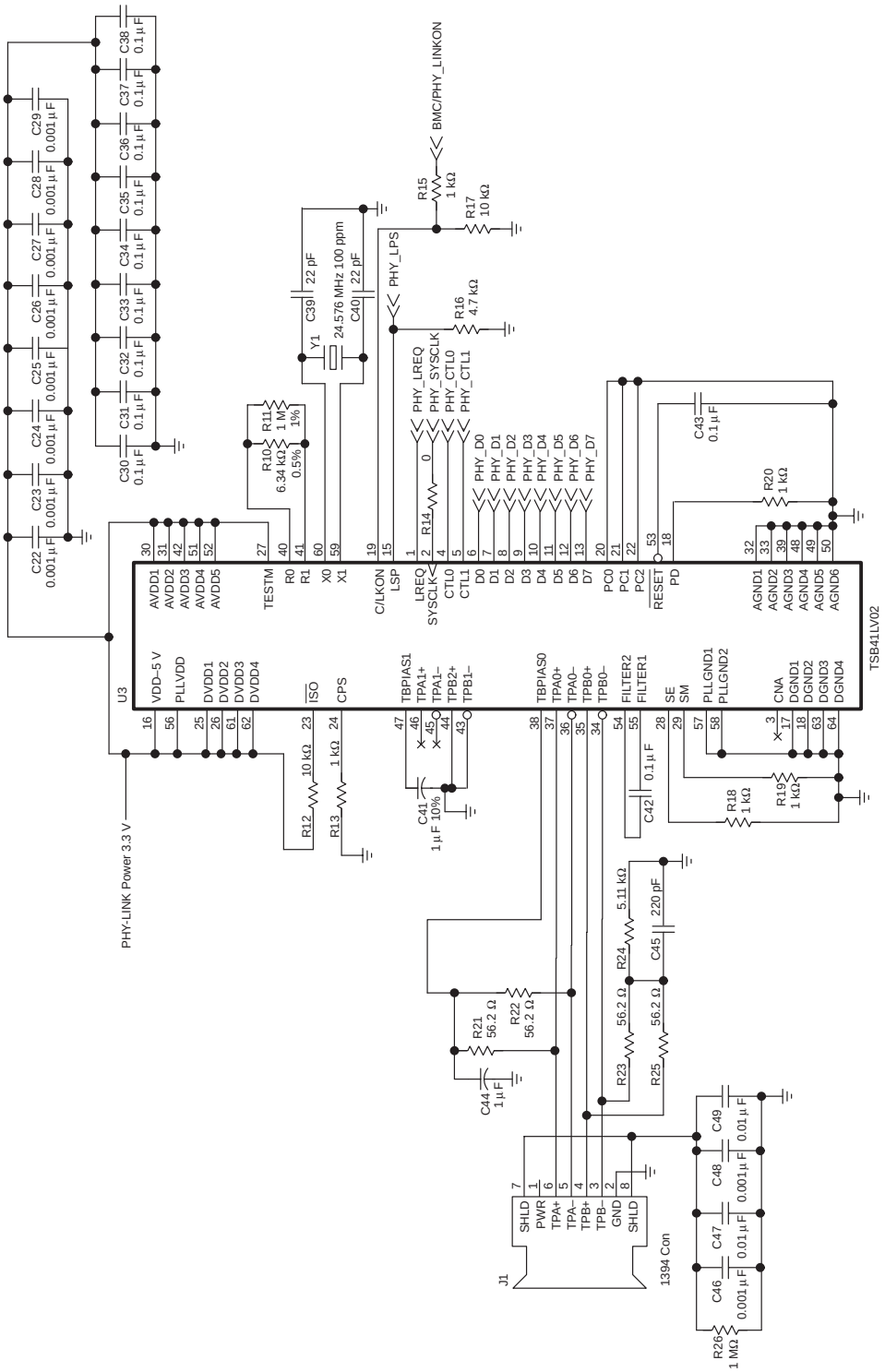


Figure 9. TSB12LV02 Schematic

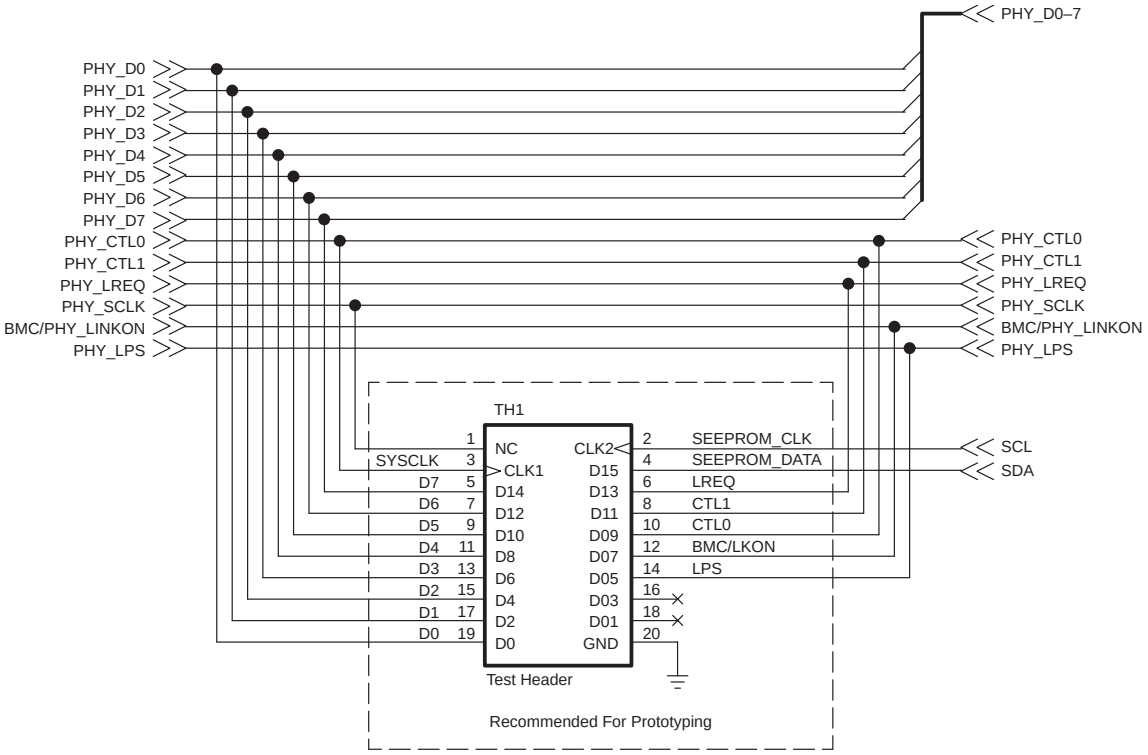


Figure 10. TSB12LV23/TSB41LV02 Interface Schematic

5.2 Parts List for Schematics

The following parts are represented on the schematic pages. Other parts may be used as long as their function meets the IEEE 1394-1995 and IEEE 1394.a requirements.

Table 3. Link Part List

	DESCRIPTION	SUPPLIER	PART NUMBER	PACKAGE	QUANTITY	REFERENCE DESIGNATOR
Capacitors	0.01 μF 10%	KEMET	C0805C103K5RAC	0805	10	C2-C11
	0.1 μF 10%	KEMET	C0805C104K5RAC	0805	10	C12-C21
	47 μF 50 V	KEMET	T491A476K050AS	2816	1	C1
Resistors	0 Ω	KOA	RM73B2AT000J	0805	2	R3-R4
	220 Ω	KOA	RM73B2AT221J	0805	2	R8-R9
	2.7 kΩ	KOA	RM73B2AT272J	0805	2	R5-R6
	4.7 kΩ	KOA	RM73B2AT472J	0805	3	R1-R2,R7
Chips	1394 400-Mbps Link	TI	TSB12LV23	100 TERMINAL TQFP	1	U1
	3.3-V EEPROM	SGS Thomson	M24C02R	S08	1	U2

Table 4. PHY Part List

	DESCRIPTION	SUPPLIER	PART NUMBER	PACKAGE	QUANTITY	REFERENCE DESIGNATOR
Capacitors	0.001 µF	KEMET	C0805C102K5RAC	0805	10	C22-C29, C46, C48
	0.01 µF 10%	KEMET	C0805C103K5RAC	0805	2	C47, C49
	0.1 µF 10%	KEMET	C0805C104K5RAC	0805	10	C30-C38, C42-C43
	1 µF 50 V	KEMET	T491A105M016AS	0805	2	C41, C44
	22 pF	KEMET	C0805C220K5RAC	0805	2	C39-C40
	220 pF	KEMET	C0805C221K5RAC	0805	1	C45
Headers	1394 R/A Flat Header	MOLEX	53462-0611	Socket_6	1	J1
Resistors	0 Ω	KOA	RM73B2AT000J	0805	1	R14
	56.2 Ω 1%	KOA	RK73H2AT56R2F	0805	4	R21-23, R25
	1 kΩ 5%	KOA	RM73B2AT102J	0805	6	R13, R15, R18-R20
	5.11 kΩ	KOA	RM73H2AT5111F	0805	1	R24
	6.34 kΩ 0.5%	KOA	RM73H2AT6341D	0805	1	R10
	10 kΩ	KOA	RM73B2AT103J	0805	2	R12, R17
	1 MΩ 1%	KOA	RK73H2AT105F	0805	2	R11, R26
Chips	1394 3-Port 400-Mbps PHY	TI	TSB41LV02	80 TERMINAL TQFP	1	U3
Crystal	XTAL, 24.576 MHz	FOX	FE 24.576 20PF	XTAL_ FE	1	Y1