TPIC3322L 3-CHANNEL COMMON-DRAIN LOGIC-LEVEL POWER DMOS ARRAY

SLIS035B - JUNE 1994 - REVISED SEPTEMBER 1995

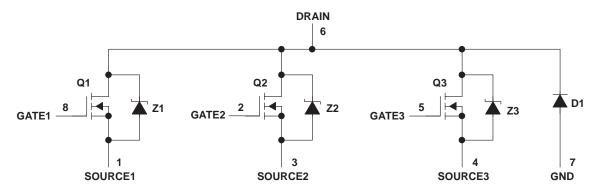
 Low r_{DS(on)} 0.6 Ω Typ High-Voltage Outputs 60 V 	D PACKAGE (TOP VIEW)
 Pulsed Current 2.25 A Per Channel Fast Commutation Speed 	SOURCE1 [1 8] GATE1 GATE2 [2 7] GND
Direct Logic-Level Interface	SOURCE2 3 6 DRAIN SOURCE3 4 5 GATE3

description

The TPIC3322L is a monolithic logic-level power DMOS transistor array that consists of three isolated N-channel enhancement-mode DMOS transistors configured with a common drain and open sources.

The TPIC3322L is offered in a standard 8-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of -40° C to 125° C.

schematic diagram



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V _{DS}	
Drain-to-GND voltage	
Gate-to-source voltage, V _{GS}	
Continuous drain current, each output, all outputs on, T _C = 25°C	0.75 A
Continuous source-to-drain diode current, T _C = 25°C	0.75 A
Pulsed drain current, each output, I _{max} , T _C = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E _{AS} , T _C = 25°C (see Figure 4)	19 mJ
Continuous total power dissipation at (or below) $T_C = 25^{\circ}C$ (see Figure 15)	0.95 W
Operating virtual junction temperature range, T _J	
Operating case temperature range, T _C	-40°C to 125°C
Storage temperature range, T _{stq}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.



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electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-to-source breakdown voltage	I _D = 250 μA,	V _{GS} = 0	60			V
VGS(th)	Gate-to-source threshold voltage	$I_D = 1 \text{ mA},$	$V_{DS} = V_{GS}$	1.5	1.85	2.2	V
V _(BR)	Reverse drain-to-GND breakdown voltage (across D1)	Drain-to-GND curren	t = 250 μA	100			V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 0.75 A, See Notes 2 and 3	$V_{GS} = 5 V$,		0.45	0.53	V
VF	Forward on-state voltage, GND-to-drain	I _D = 0.75 A, See Notes 2 and 3			1.8		V
V _F (SD)	Forward on-state voltage, source-to-drain	Is = 0.75 A, See Notes 2 and 3 a	VGS = 0, nd Figure 12		0.85	1	V
l	Zana mata walta na duain awanat	V _{DS} = 48 V,	T _C = 25°C		0.05	1	^
IDSS	Zero-gate-voltage drain current	V _{GS} = 0	T _C = 125°C		0.5	10	μΑ
IGSSF	Forward gate current, drain short circuited to source	V _{GS} = 16 V,	$V_{DS} = 0$		10	100	nA
I _{GSSR}	Reverse gate current, drain short circuited to source	V _{SG} = 16 V,	$V_{DS} = 0$		10	100	nA
lu.	Leakage current, drain-to-GND	V _{DGND} = 48 V	T _C = 25°C		0.05	1	μΑ
likg	Leakage current, drain-to-GND		T _C = 125°C		0.5	10	
rno()	Static drain-to-source on-state resistance	$V_{GS} = 5 \text{ V},$ $I_{D} = 0.75 \text{ A},$	T _C = 25°C		0.6	0.7	Ω
rDS(on)	Static drain-to-source on-state resistance	See Notes 2 and 3 and Figures 6 and 7	T _C = 125°C		0.94	1	22
9fs	Forward transconductance	V _{DS} = 10 V, See Notes 2 and 3 ar	I _D = 0.5 A, nd Figure 9	0.75	0.9		S
C _{iss}	Short-circuit input capacitance, common source				115	145	
C _{oss}	Short-circuit output capacitance, common source		$V_{GS} = 0$,		60	75	pF
C _{rss}	Short-circuit reverse transfer capacitance, common source		See Figure 11		30	40	Pi

NOTES: 2. Technique should limit $T_J - T_C$ to $10^{\circ}C$ maximum.

source-to-drain and GND-to-drain diode characteristics, $T_{\mbox{\scriptsize C}}$ = 25 $^{\circ}\mbox{\scriptsize C}$

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
1 ' '		V _{GS} = 0, V _{DS} = 48 V,	Z1, Z2, Z3		30			
	$I_S = 0.375 \text{ A},$ di/dt = 100 A/µs,		D1		85		ns	
Q _{RR} Total diode charge See Figures 1 and 14	v _D S = 40 v,	Z1, Z2, Z3		0.03		μC		
		D1		0.19		μΟ		

^{3.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

resistive-load switching characteristics, T_C = 25°C

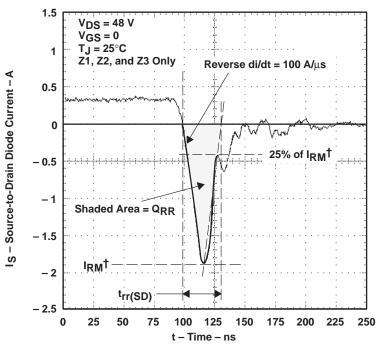
	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT																																												
t _d (on)	Turn-on delay time					8	16																																													
t _d (off)	Turn-off delay time	$V_{DD} = 25 \text{ V},$ $t_{f1} = 10 \text{ ns},$	$V_{DD} = 25 \text{ V}, \qquad R_{L} = 67 \Omega,$	$t_{r1} = 10 \text{ ns},$		12	24	no																																												
t _{r2}	Rise time					14	28	ns																																												
t _{f2}	Fall time					13	26																																													
Qg	Total gate charge					1.8	2.3																																													
Q _{gs(th)}	Threshold gate-to-source charge	V _{DS} = 48 V, See Figure 3		V _{DS} = 48 V, See Figure 3																																											$I_D = 0.375 A,$	$V_{GS} = 5 V$,		0.4	0.5	nC
Q _{gd}	Gate-to-drain charge					1.1	1.4																																													
L _D	Internal drain inductance					5		-11																																												
LS	Internal source inductance					5		nH																																												
Rg	Internal gate resistance					0.25		Ω																																												

thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			44		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

PARAMETER MEASUREMENT INFORMATION

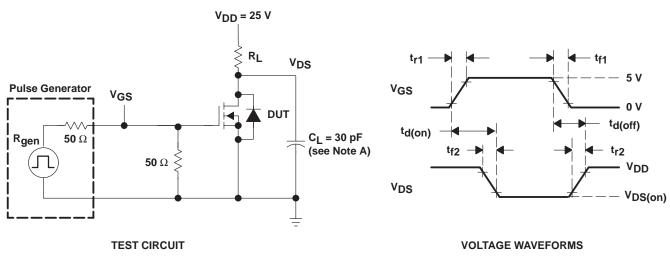


† I_{RM} = maximum recovery current NOTE A. The above waveform represents D1 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

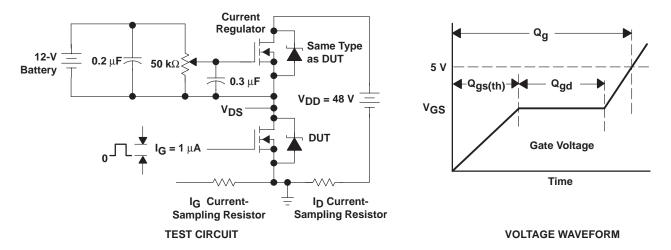
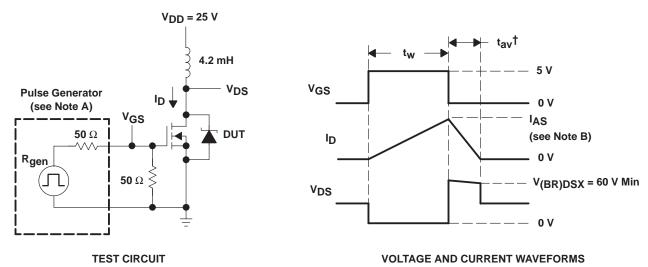


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



† Non-JEDEC symbol for avalanche time

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $z_0 = 50 \Omega$.

B. Input pulse duration (t_W) is increased until peak current IAS = 2.25 A.

Energy test level is defined as
$$E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 19$$
 mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE **JUNCTION TEMPERATURE JUNCTION TEMPERATURE** 2.5 1.5 VGS (th) - Gate-to-Source Threshold Voltage - V $I_D = 0.75 A$ $V_{DS} = V_{GS}$ ' DS(on) - Static Drain-to-Source On-State 2 1.2 $I_D = 1 \text{ mA}$ Resistance - D 1.5 0.9 $I_D = 100 \, \mu A$ VGS = 4.5 V $V_{GS} = 5 V$ 0.6 0.5 0.3 20 40 60 80 100 120 140 160 -40 -20 40 60 80 100 120 140 160 -40 - 2020 T_J - Junction Temperature - °C T_J - Junction Temperature - °C Figure 5 Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

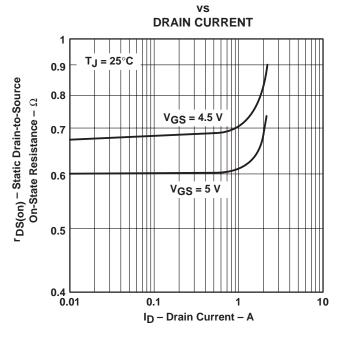


Figure 7

DRAIN CURRENT DRAIN-TO-SOURCE VOLTAGE 2.25 2 $V_{GS} = 4 V$ 1.75 D- Drain Current - A 1.50 $V_{GS} = 3.6 V$ 1.25 0.75 $V_{GS} = 3 V$ 0.50 T_J = 25°C 0.25 $\triangle V_{GS} = 0.2 V$ 0 0 2 V_{DS} - Drain-to-Source Voltage - V

Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

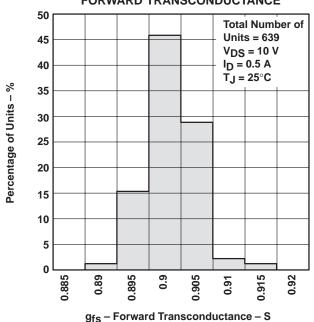


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

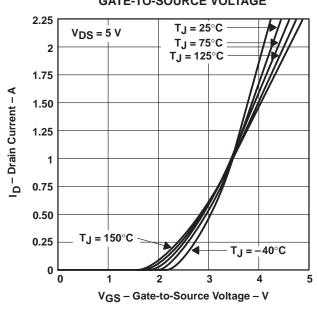


Figure 10



TYPICAL CHARACTERISTICS

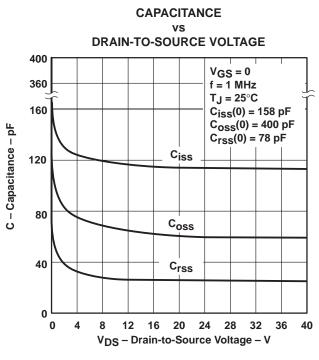


Figure 11

DRAIN-TO-SOURCE AND GATE-TO-SOURCE VOLTAGE

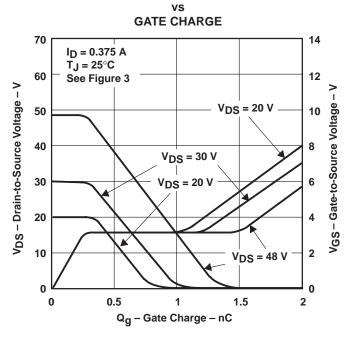


Figure 13

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

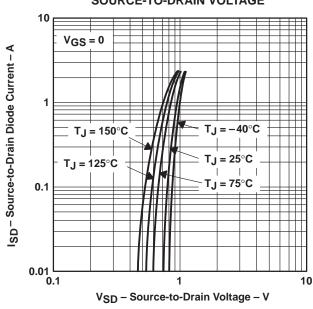


Figure 12

REVERSE-RECOVERY TIME

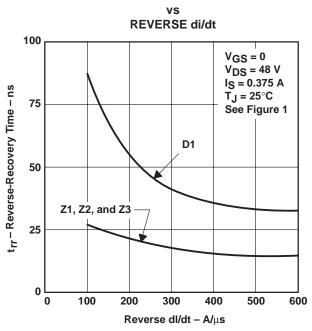
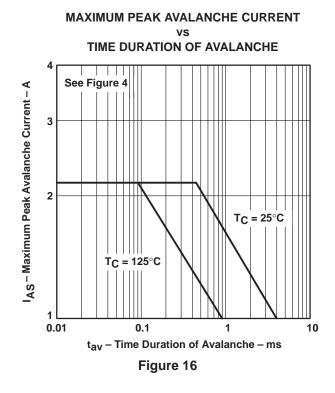


Figure 14

THERMAL INFORMATION

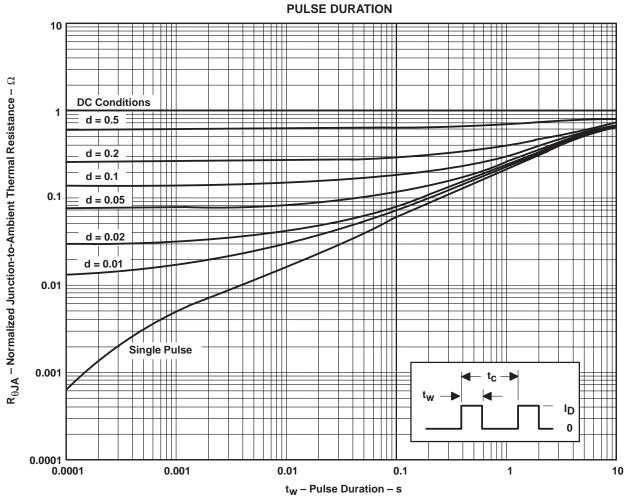
†Less than 2% duty cycle

Figure 15



THERMAL INFORMATION

NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE[†]



† Device mounted on FR4 printed-circuit board with no heat sink.

NOTE A: $Z_{\theta A}(t) = r(t) R_{\theta JA}$ $t_W = \text{pulse duration}$ $t_C = \text{cycle time}$ $d = \text{duty cycle} = t_W/t_C$

Figure 17

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