SLDS011B – OCTOBER 1985 – REVISED MAY 1993

- **Drives up to 20 Lines**
- **70-V Output Voltage Swing Capability**
- **40-mA Output Source Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **CMOS-Compatible Inputs**
- **Direct Replacement for Sprague UCN5812A**

description

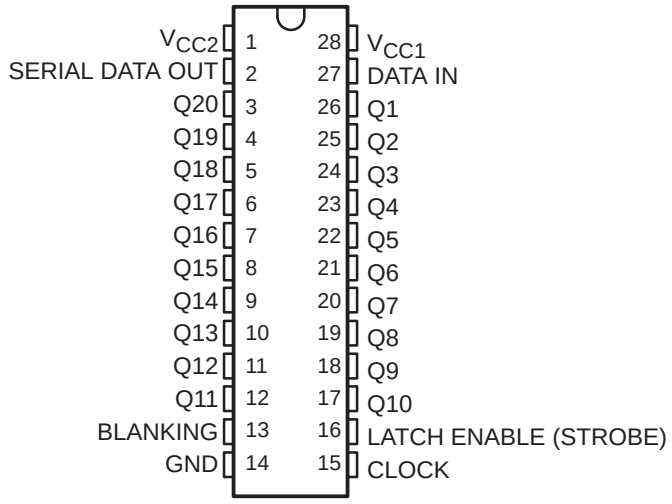
The TL5812 and TL5812I are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). Each device features a serial data output to cascade additional devices for large display arrays.

A 20-bit data word is serially loaded into the shift register on the low-to-high transition of CLOCK. Parallel data is transferred to the output buffers through a 20-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

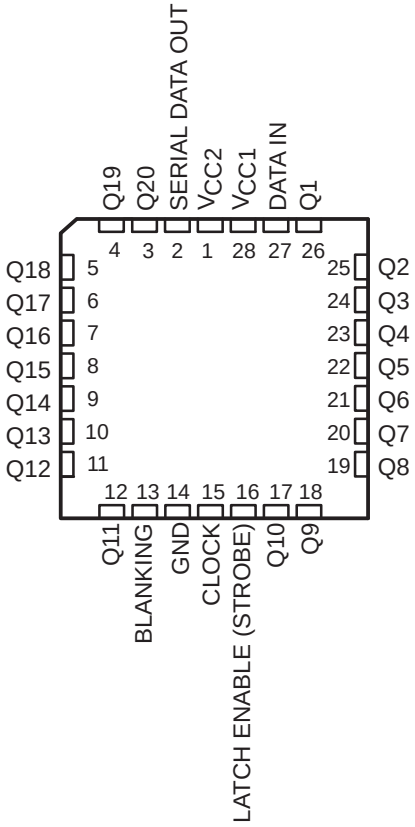
The outputs are totem-pole structures formed by npn emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and a source-current capability of 40 mA. All inputs are CMOS compatible.

The TL5812 is characterized for operation from 0°C to 70°C. The TL5812I is characterized for operation from –40°C to 85°C.

N PACKAGE
(TOP VIEW)

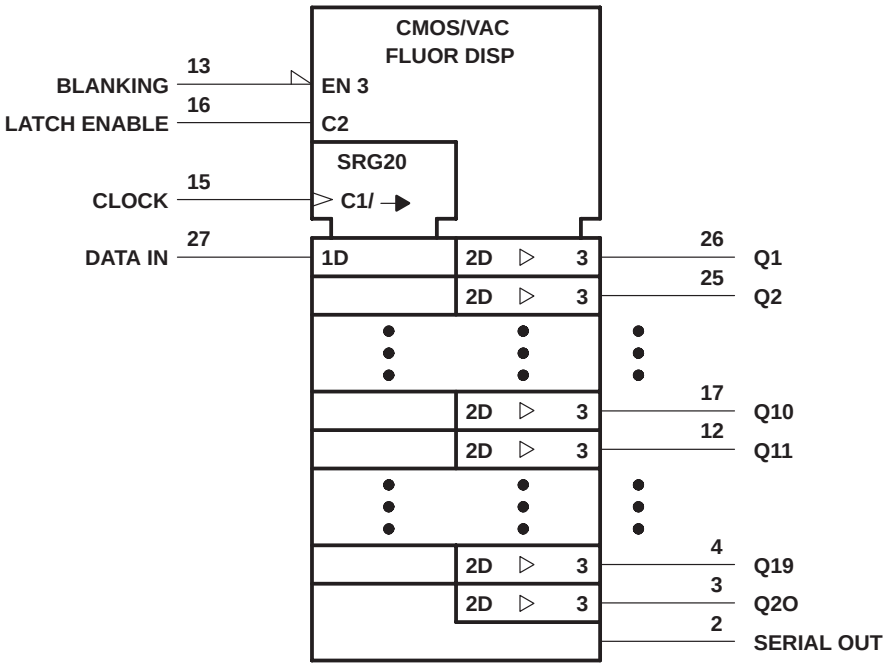


FN PACKAGE
(TOP VIEW)



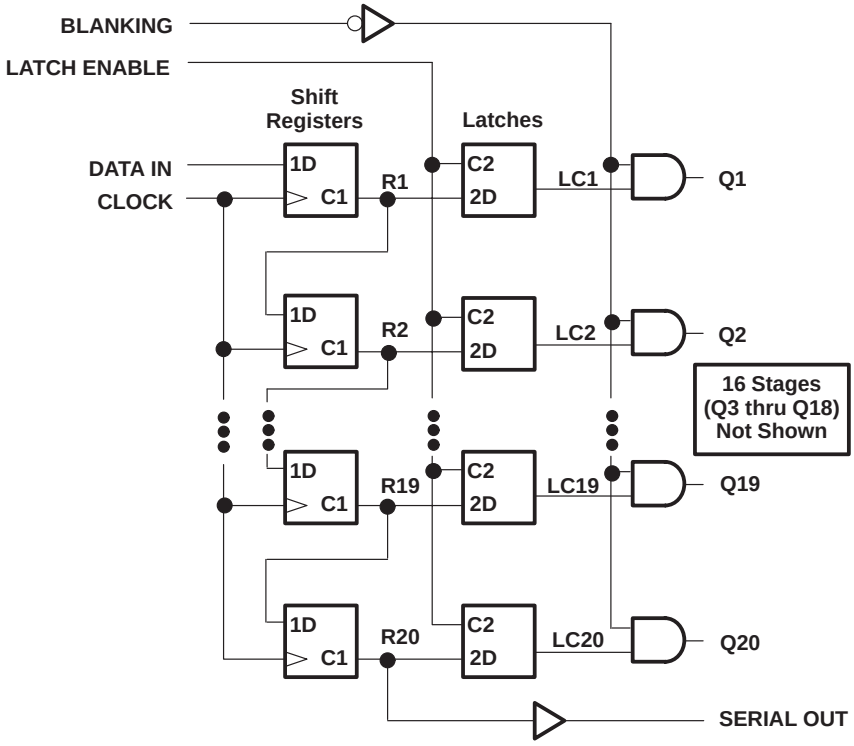
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

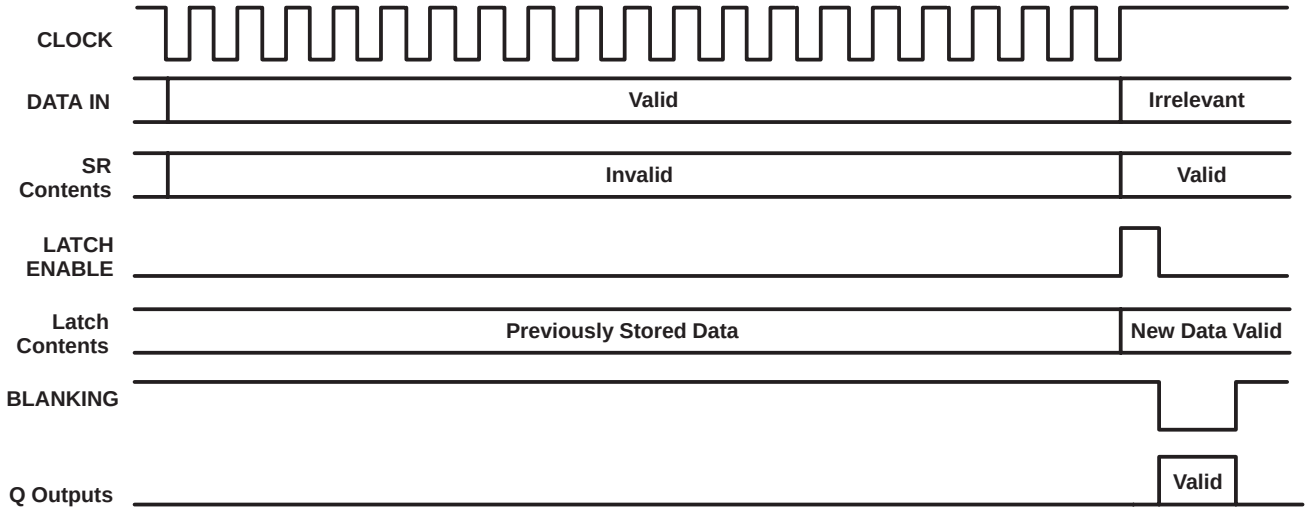


FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R20	LATCHES LC1 THRU LC20	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANKING			SERIAL	Q1 THRU Q20
Load	↑ No↑	X X	X X	Load and shift† No change	Determined by LATCH ENABLE‡	R20 R20	Determined by BLANKING
Latch	X X	L H	X X	As determined above	Stored data New data	R20 R20	Determined by BLANKING
Blank	X X	X X	H L	As determined above	Determined by LATCH ENABLE‡	R20 R20	All L LC1 thru LC10, respectively

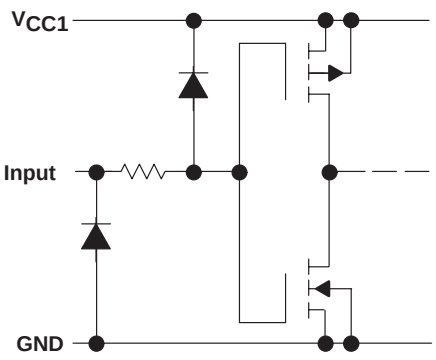
H = high level, L = low level, X = irrelevant, ↑= low-to-high-level transition.
† R20 takes on the state of R19, R19 takes on the state of R18, ... R2 takes on the state of R1, and R1 takes on the state of the data input.
‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence

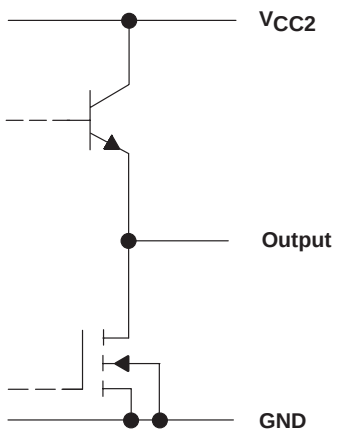


schematics of inputs and outputs

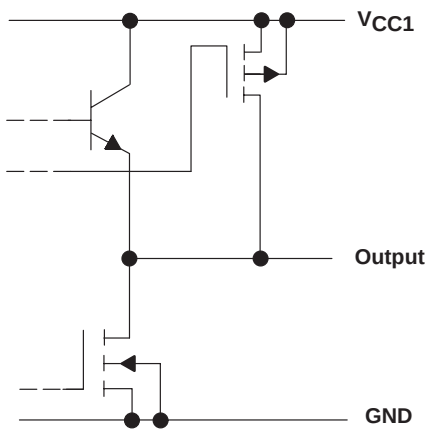
EQUIVALENT OF EACH INPUT



TYPICAL OF ALL Q OUTPUTS



TYPICAL OF SERIAL OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Output voltage, V_O . . . . . 70 V
Input voltage range, V_I . . . . . –0.3 V to V_{CC1} +0.3 V
Output current, I_O . . . . . –40 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL5812 . . . . . 0°C to 70°C
TL5812I . . . . . –40°C to 85°C
Storage temperature range, ... –65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1400 mW	11.2 mW/°C	896 mW	728 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		4.5		15	V
Supply voltage, V_{CC2}		0		60	V
High-level input voltage, V_{IH}		V_{CC1}–1.5		V_{CC1}+0.3	V
Low-level input voltage, V_{IL}		–0.3†		0.8	V
High-level output current, I_{OH}				–40	mV
Operating free-air temperature, T_A	TL5812	0		70	°C
	TL5812I	–40		85	

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over operating free-air temperature range, V_{DD} = 5 V to 15 V, V_{BB} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output	Q outputs	I_{OH} = –25 mA		57.5	58.2		V
		SERIAL DATA OUT	V_{CC1} = 5 V,	I_{OH} = –20 µA	4.5	4.9		
			V_{CC1} = 15 V,	I_{OH} = –20 µA	14.5	14.9		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA,	BLANKING at V_{CC1}		0.7	1.5	V
		SERIAL DATA OUT	V_{CC1} = 5 V,	I_{OL} = 20 µA		0.06	0.3	
			V_{CC1} = 15 V,	I_{OL} = 20 µA		0.03	0.3	
I_{IH}	High-level input current		$V_I = V_{CC1}$			0.3	1	µA
I_{IL}	Low-level input current		V_I = 0			–0.3	–1	µA
I_{OL}	Low-level output current (pulldown current)		V_O = 60 V,	BLANKING at V_{CC1}	2.5	3.2		µA
$I_{O(off)}$	Off-state output current		V_O = 0,	BLANKING at V_{CC1}		< – 1	–15	µA
I_{CC2}	Supply current from V_{CC2}		Outputs high			3.5	8	mA
			Outputs low			0.02	0.5	
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 5 V			1.5	3	mA
			V_{CC1}= 15 V			1.7	4	

‡ All typical characteristics are at T_A= 25°C.

timing requirements over operating free-air temperature range

			MIN	MAX	UNIT
$t_{w(CKH)}$	Pulse duration, CLOCK high	V_{CC1} = 5 V	500		ns
		V_{CC1} = 15 V	100		
$t_{w(LEH)}$	Pulse duration, LATCH ENABLE high	V_{CC1} = 5 V	500		ns
		V_{CC1} = 15 V	100		
$t_{su(D)}$	Setup time, DATA IN before CLOCK↑	V_{CC1} = 5 V	150		ns
		V_{CC1} = 15 V	75		
$t_{h(D)}$	Hold time, DATA IN after CLOCK↑	V_{CC1} = 5 V	150		ns
		V_{CC1} = 15 V	75		
$t_{d(CKH-LEH)}$	Delay time, CLOCK↑ to LATCH ENABLE high	V_{CC1} = 5 V	150		ns
		V_{CC1} = 15 V	75		

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, LATCH ENABLE to Q outputs	V_{CC1} = 5 V		2.2		µs
		V_{CC1} = 15 V		0.8		

PARAMETER MEASUREMENT INFORMATION

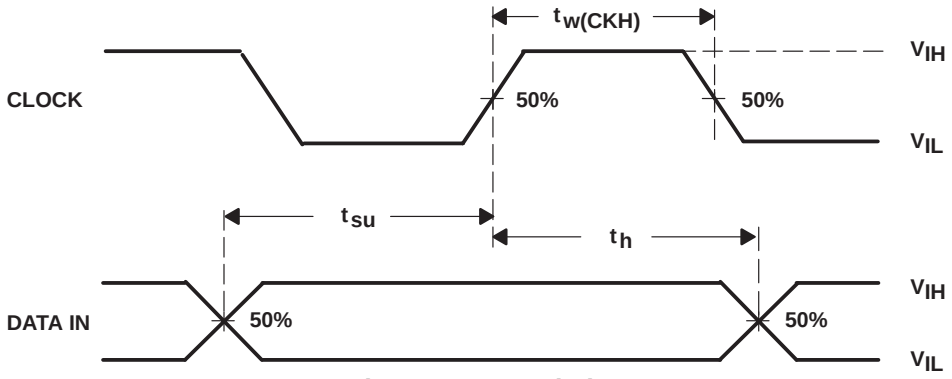


Figure 1. Input Timing

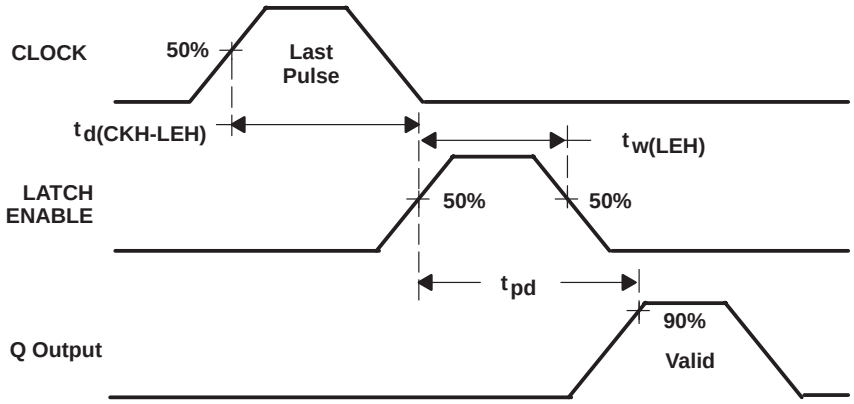


Figure 2. Output Switching Times

THERMAL INFORMATION

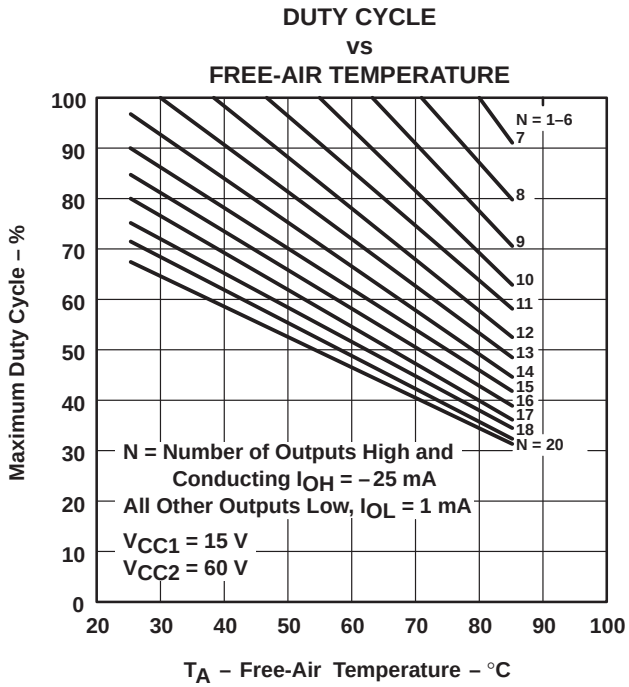


Figure 3

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